# HEF4053B

## Triple single-pole double-throw analog switch

**Rev. 10 — 17 November 2011** **Product data sheet**

## 1. General description

The HEF4053B is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input ($\overline{E}$). A HIGH on $\overline{E}$ causes all switches into the high-impedance OFF-state, independent of Sn.

$V_{DD}$ and $V_{SS}$ are the supply voltage connections for the digital control inputs (Sn and $\overline{E}$). The $V_{DD}$ to $V_{SS}$ range is 3 V to 15 V. The analog inputs/outputs (nY0, nY1 and nZ) can swing between $V_{DD}$ as a positive limit and $V_{EE}$ as a negative limit. $V_{DD} – V_{EE}$ may not exceed 15 V. Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input. For operation as a digital multiplexer/demultiplexer, $V_{EE}$ is connected to $V_{SS}$ (typically ground). $V_{EE}$ and $V_{SS}$ are the supply voltage connections for the switches.

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## 4. Ordering information

**Table 1. Ordering information**
*All types operate from –40 °C to +125 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4053BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4053BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| HEF4053BTT | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

## 5. Functional diagram

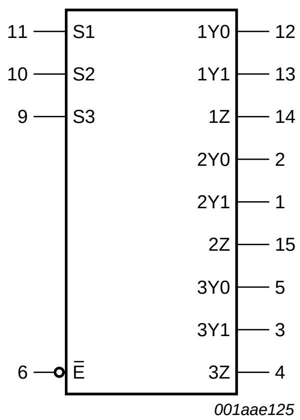



**Fig 1. Logic symbol**

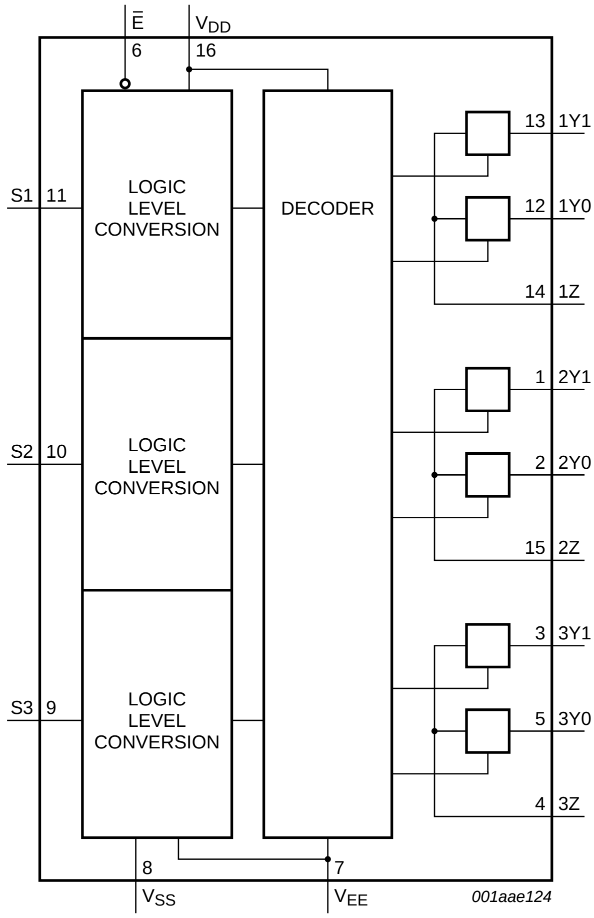



**Fig 2. Functional diagram**

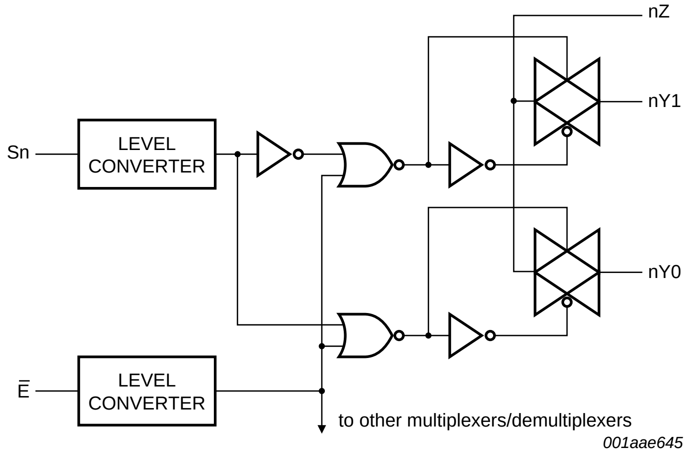



**Fig 3. Logic diagram (one multiplexer/demultiplexer)**

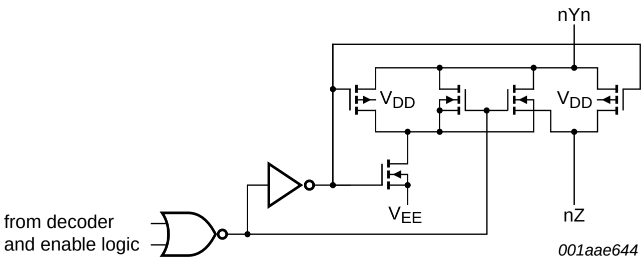



**Fig 4. Schematic diagram (one switch)**

# 6. Pinning information

## 6.1 Pinning

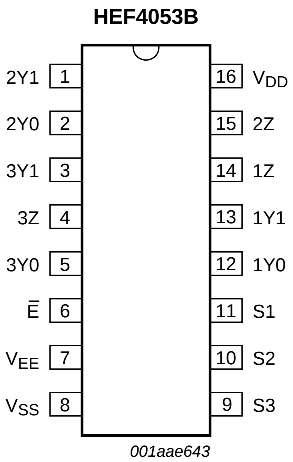



**Fig 5. Pin configuration for SOT38-4 (DIP16) and SOT109-1 (SO16)**

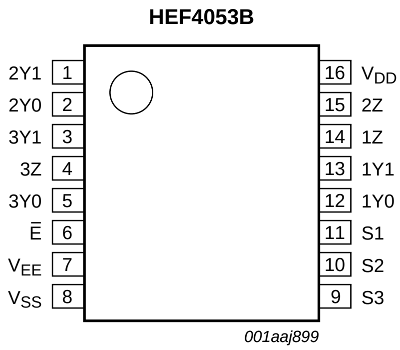



**Fig 6. Pin configuration for SOT403-1 (TSSOP16)**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{E}$ | 6 | enable input (active LOW) |
| $V_{EE}$ | 7 | supply voltage |
| $V_{SS}$ | 8 | ground supply voltage |
| S1, S2, S3 | 11, 10, 9 | select input |
| 1Y0, 2Y0, 3Y0 | 12, 2, 5 | independent input or output |
| 1Y1, 2Y1, 3Y1 | 13, 1, 3 | independent input or output |
| 1Z, 2Z, 3Z | 14, 15, 4 | independent output or input |
| $V_{DD}$ | 16 | supply voltage |

# 7. Functional description

**Table 3. Function table [1]**

| Inputs | | Channel on |
|---|---|---|
| $\overline{E}$ | Sn | |
| L | L | nY0 to nZ |
| L | H | nY1 to nZ |
| H | X | switches OFF |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS}$ = 0 V (ground).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.5 | +18 | V |
| $V_{EE}$ | supply voltage | referenced to $V_{DD}$ | [1] | –18 | +0.5 | V |
| $I_{IK}$ | input clamping current | pins Sn and $\overline{E}$; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | –0.5 | $V_{DD}$ + 0.5 | V |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | –40 | +125 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | [2] | | | |
| | | DIP16 package | | - | 750 | mW |
| | | SO16 package | | - | 500 | mW |
| | | TSSOP16 package | | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1] To avoid drawing $V_{DD}$ current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no $V_{DD}$ current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed $V_{DD}$ or $V_{EE}$.

[2] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.
For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

# 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | see Figure 7 | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +125 | °C |

**Table 5. Recommended operating conditions** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | μs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | μs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | μs/V |

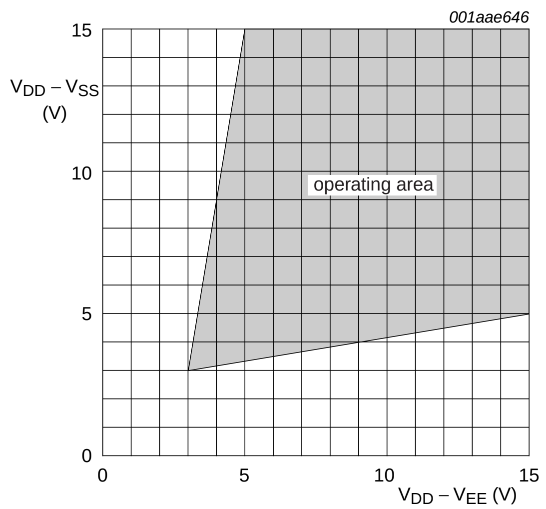



**Fig 7. Operating area as a function of the supply voltages**

## 10. Static characteristics

**Table 6. Static characteristics**

*$V_{SS} = V_{EE} = 0$ V; $V_I = V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | $T_{amb}$ = 125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\lvert I_O \rvert < 1$ μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\lvert I_O \rvert < 1$ μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $I_I$ | input leakage current | | 15 V | - | ±0.1 | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | Z port; all channels OFF; see Figure 8 | 15 V | - | - | - | 1000 | - | - | - | - | nA |
| | | Y port; per channel; see Figure 9 | 15 V | - | - | - | 200 | - | - | - | - | nA |

**Table 6. Static characteristics** *...continued*

*$V_{SS} = V_{EE} = 0$ V; $V_I = V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | $T_{amb}$ = 125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 5 | - | 5 | - | 150 | - | 150 | µA |
| | | | 10 V | - | 10 | - | 10 | - | 300 | - | 300 | µA |
| | | | 15 V | - | 20 | - | 20 | - | 600 | - | 600 | µA |
| $C_I$ | input capacitance | Sn, $\overline{E}$ inputs | - | - | - | - | 7.5 | - | - | - | - | pF |

## 10.1 Test circuits

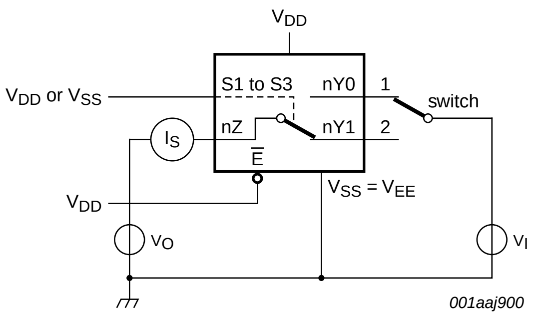



**Fig 8. Test circuit for measuring OFF-state leakage current Z port**

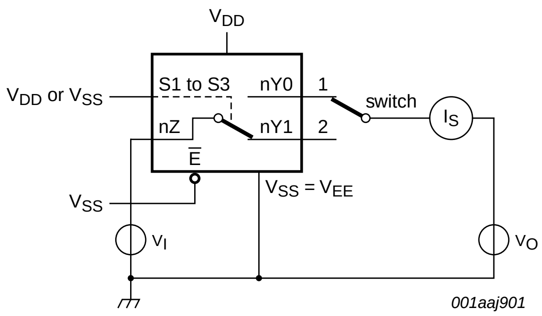



**Fig 9. Test circuit for measuring OFF-state leakage current nYn port**

## 10.2 ON resistance

**Table 7. ON resistance**

*$T_{amb}$ = 25 °C; $I_{SW}$ = 200 µA; $V_{SS} = V_{EE} = 0$ V.*

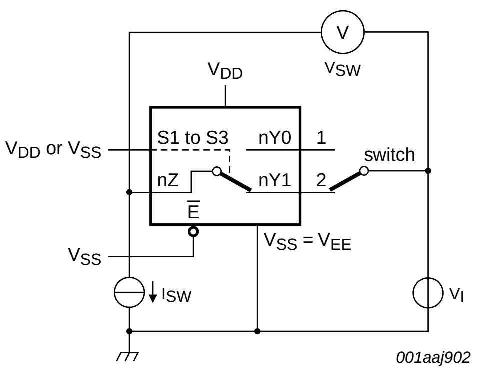
| Symbol | Parameter | Conditions | $V_{DD} - V_{EE}$ | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{ON(peak)}$ | ON resistance (peak) | $V_I$ = 0 V to $V_{DD} - V_{EE}$; see Figure 10 and Figure 11 | 5 V | 350 | 2500 | Ω |
| | | | 10 V | 80 | 245 | Ω |
| | | | 15 V | 60 | 175 | Ω |

**Table 7. ON resistance** *...continued*

*$T_{amb}$ = 25 °C; $I_{SW}$ = 200 μA; $V_{SS}$ = $V_{EE}$ = 0 V.*

| Symbol | Parameter | Conditions | $V_{DD} - V_{EE}$ | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{ON(rail)}$ | ON resistance (rail) | $V_I$ = 0 V; see Figure 10 and Figure 11 | 5 V | 115 | 340 | Ω |
| | | | 10 V | 50 | 160 | Ω |
| | | | 15 V | 40 | 115 | Ω |
| | | $V_I = V_{DD} - V_{EE}$; see Figure 10 and Figure 11 | 5 V | 120 | 365 | Ω |
| | | | 10 V | 65 | 200 | Ω |
| | | | 15 V | 50 | 155 | Ω |
| $\Delta R_{ON}$ | ON resistance mismatch between channels | $V_I$ = 0 V to $V_{DD} - V_{EE}$; see Figure 10 | 5 V | 25 | - | Ω |
| | | | 10 V | 10 | - | Ω |
| | | | 15 V | 5 | - | Ω |

### 10.2.1 ON resistance waveform and test circuit




$R_{ON} = V_{SW} / I_{SW}$.

**Fig 10. Test circuit for measuring $R_{ON}$**

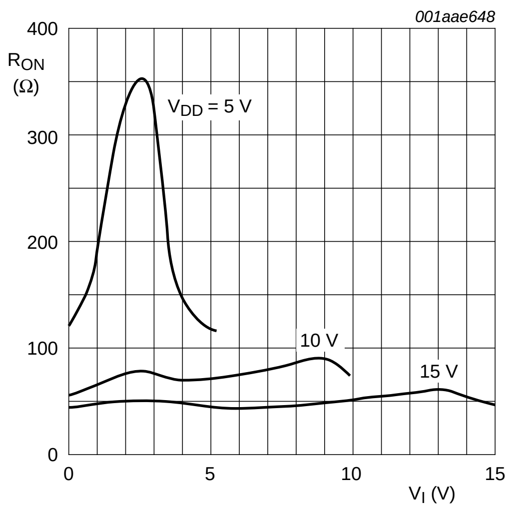



**Fig 11. Typical $R_{ON}$ as a function of input voltage**

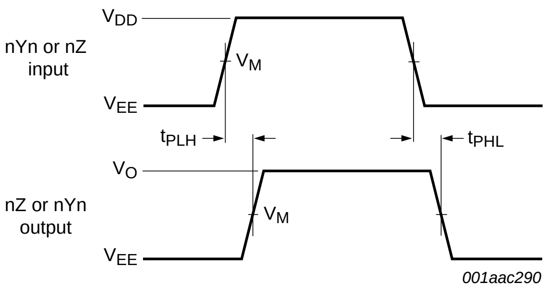
# 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*$T_{amb}$ = 25 °C; $V_{SS}$ = $V_{EE}$ = 0 V; for test circuit see Figure 15.*

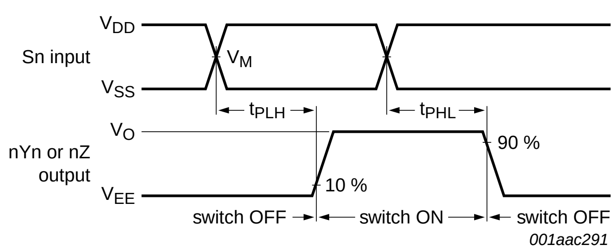
| Symbol | Parameter | Conditions | $V_{DD}$ | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | nYn, nZ to nZ, nYn; see Figure 12 | 5 V | 10 | 20 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 13 | 5 V | 200 | 400 | ns |
| | | | 10 V | 85 | 170 | ns |
| | | | 15 V | 65 | 130 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | nYn, nZ to nZ, nYn; see Figure 12 | 5 V | 15 | 30 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 13 | 5 V | 275 | 555 | ns |
| | | | 10 V | 100 | 200 | ns |
| | | | 15 V | 65 | 130 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $\overline{E}$ to nYn, nZ; see Figure 14 | 5 V | 200 | 400 | ns |
| | | | 10 V | 115 | 230 | ns |
| | | | 15 V | 110 | 220 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $\overline{E}$ to nYn, nZ; see Figure 14 | 5 V | 260 | 525 | ns |
| | | | 10 V | 95 | 190 | ns |
| | | | 15 V | 65 | 130 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $\overline{E}$ to nYn, nZ; see Figure 14 | 5 V | 200 | 400 | ns |
| | | | 10 V | 120 | 245 | ns |
| | | | 15 V | 110 | 215 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | $\overline{E}$ to nYn, nZ; see Figure 14 | 5 V | 280 | 565 | ns |
| | | | 10 V | 105 | 205 | ns |
| | | | 15 V | 70 | 140 | ns |

## 11.1 Waveforms and test circuit



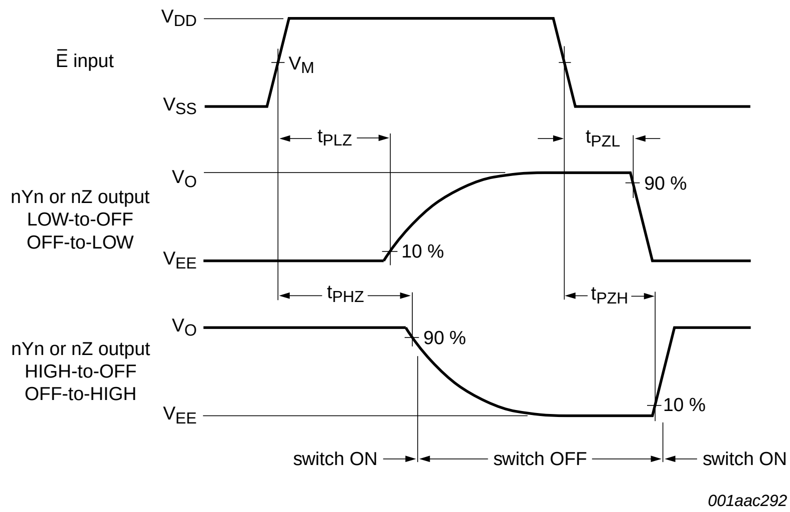

Measurement points are given in Table 9.

**Fig 12. nYn, nZ to nZ, nYn propagation delays**




Measurement points are given in Table 9.

**Fig 13. Sn to nYn, nZ propagation delays**

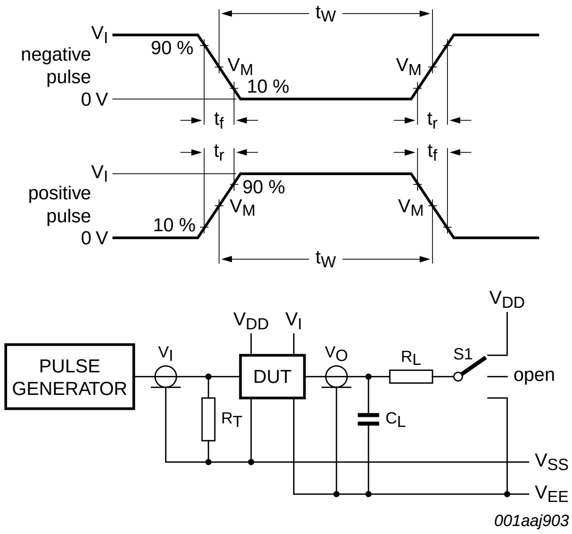



Measurement points are given in Table 9.

**Fig 14. Enable and disable times**

### Table 9. Measurement points

| Supply voltage | Input | Output |
|---|---|---|
| **$V_{DD}$** | **$V_M$** | **$V_M$** |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |




Test data is given in Table 10.

Definitions:

DUT = Device Under Test.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including test jig and probe.

$R_L$ = Load resistance.

**Fig 15. Test circuit for measuring switching times**

**Table 10. Test data**

| Input | | | | Load | | S1 position | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| nYn, nZ | Sn and $\overline{E}$ | $t_r$, $t_f$ | $V_M$ | $C_L$ | $R_L$ | $t_{PHL}$ [1] | $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ | other |
| $V_{DD}$ or $V_{EE}$ | $V_{DD}$ or $V_{SS}$ | $\leq$ 20 ns | $0.5V_{DD}$ | 50 pF | 10 k$\Omega$ | $V_{DD}$ or $V_{EE}$ | $V_{EE}$ | $V_{EE}$ | $V_{DD}$ | $V_{EE}$ |

[1] For nYn to nZ or nZ to nYn propagation delays use $V_{EE}$. For Sn to nYn or nZ propagation delays use $V_{DD}$.

## 11.2 Additional dynamic parameters

**Table 11. Additional dynamic characteristics**
*$V_{SS} = V_{EE} = 0$ V; $T_{amb} = 25$ °C.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| THD | total harmonic distortion | see Figure 16; $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1$ kHz | 5 V | [1] | 0.25 | - | % |
| | | | 10 V | [1] | 0.04 | - | % |
| | | | 15 V | [1] | 0.04 | - | % |
| $f_{(-3dB)}$ | −3 dB frequency response | see Figure 17; $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_I = 0.5V_{DD}$ (p-p) | 5 V | [1] | 13 | - | MHz |
| | | | 10 V | [1] | 40 | - | MHz |
| | | | 15 V | [1] | 70 | - | MHz |
| $\alpha_{iso}$ | isolation (OFF-state) | see Figure 18; $f_i = 1$ MHz; $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_I = 0.5V_{DD}$ (p-p) | 10 V | [1] | −50 | - | dB |
| $V_{ct}$ | crosstalk voltage | digital inputs to switch; see Figure 19; $R_L = 10$ kΩ; $C_L = 15$ pF; $\overline{E}$ or Sn = $V_{DD}$ (square-wave) | 10 V | | 50 | - | mV |
| Xtalk | crosstalk | between switches; see Figure 20; $f_i = 1$ MHz; $R_L = 1$ kΩ; $V_I = 0.5V_{DD}$ (p-p) | 10 V | [1] | −50 | - | dB |

[1] $f_i$ is biased at 0.5 $V_{DD}$; $V_I = 0.5V_{DD}$ (p-p).

**Table 12. Dynamic power dissipation $P_D$**
*$P_D$ can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25$ °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (μW) | where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz; |
| | | 10 V | $P_D = 11500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_o$ = output frequency in MHz; |
| | | 15 V | $P_D = 29000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $C_L$ = output load capacitance in pF; |
| | | | | $V_{DD}$ = supply voltage in V; |
| | | | | $\Sigma(C_L \times f_o)$ = sum of the outputs. |

### 11.2.1 Test circuits

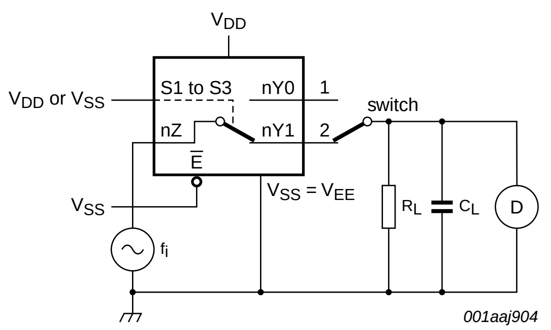



**Fig 16. Test circuit for measuring total harmonic distortion**

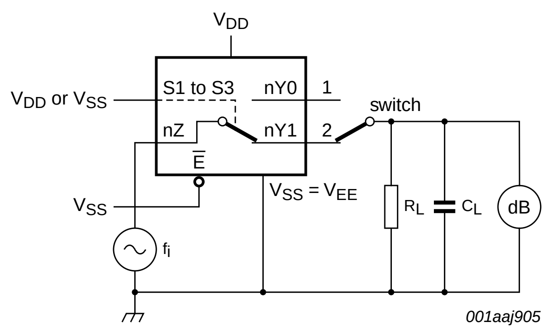



**Fig 17. Test circuit for measuring frequency response**

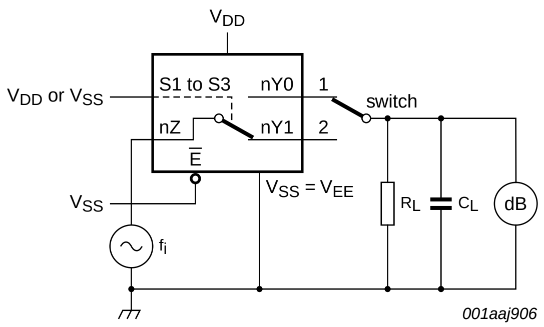
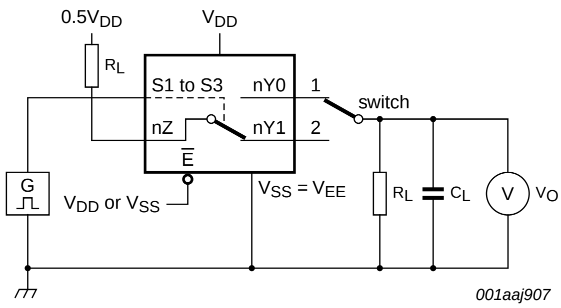
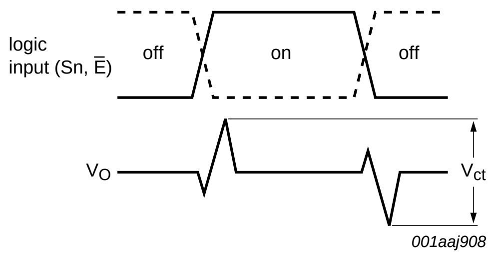



**Fig 18. Test circuit for measuring isolation (OFF-state)**

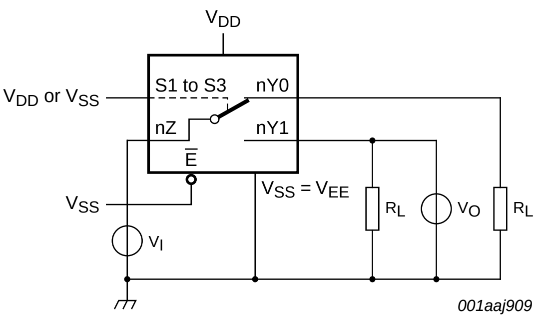



a. Test circuit

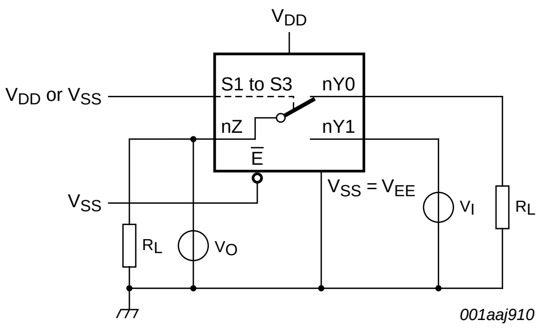



b. Input and output pulse definitions

**Fig 19. Test circuit for measuring crosstalk voltage between digital inputs and switch**




a. Switch closed condition

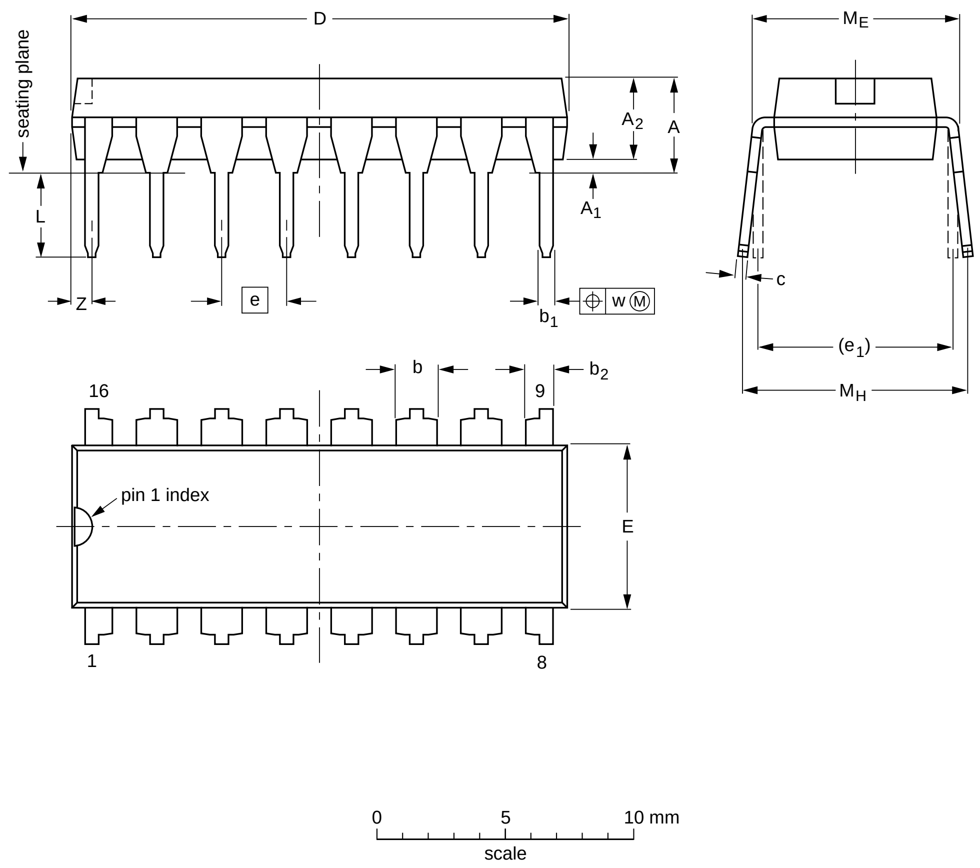



b. Switch open condition

**Fig 20. Test circuit for measuring crosstalk between switches**

## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

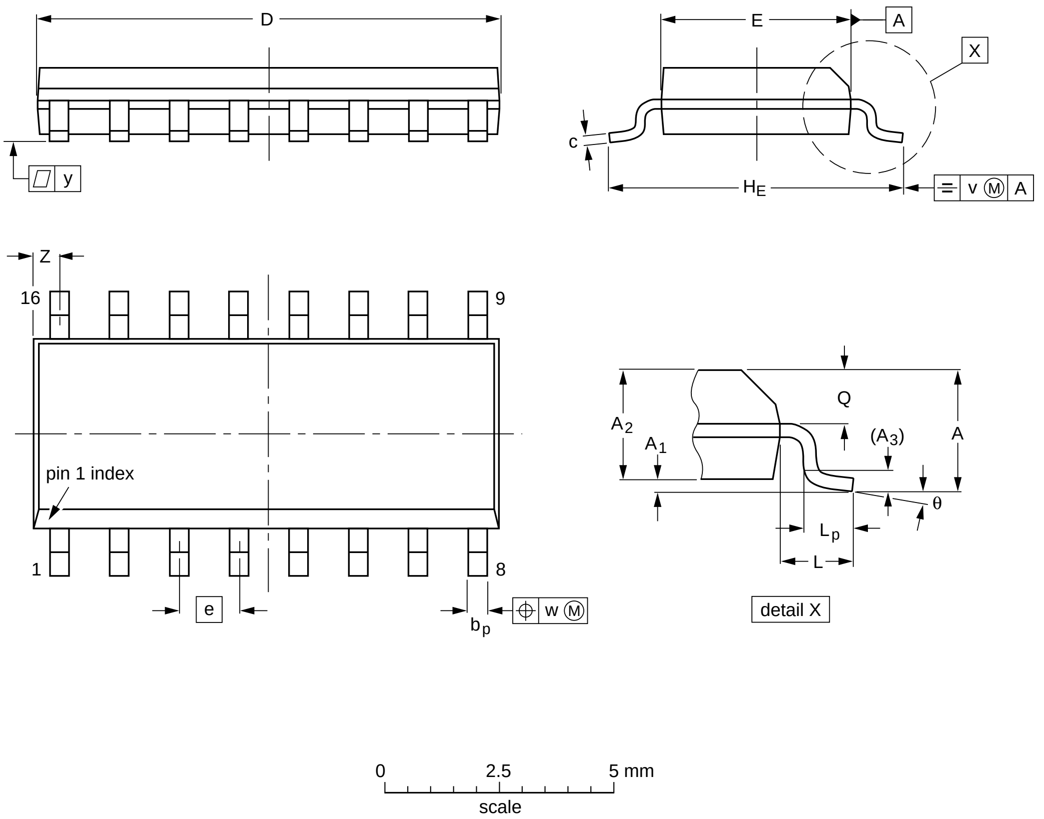
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 21. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

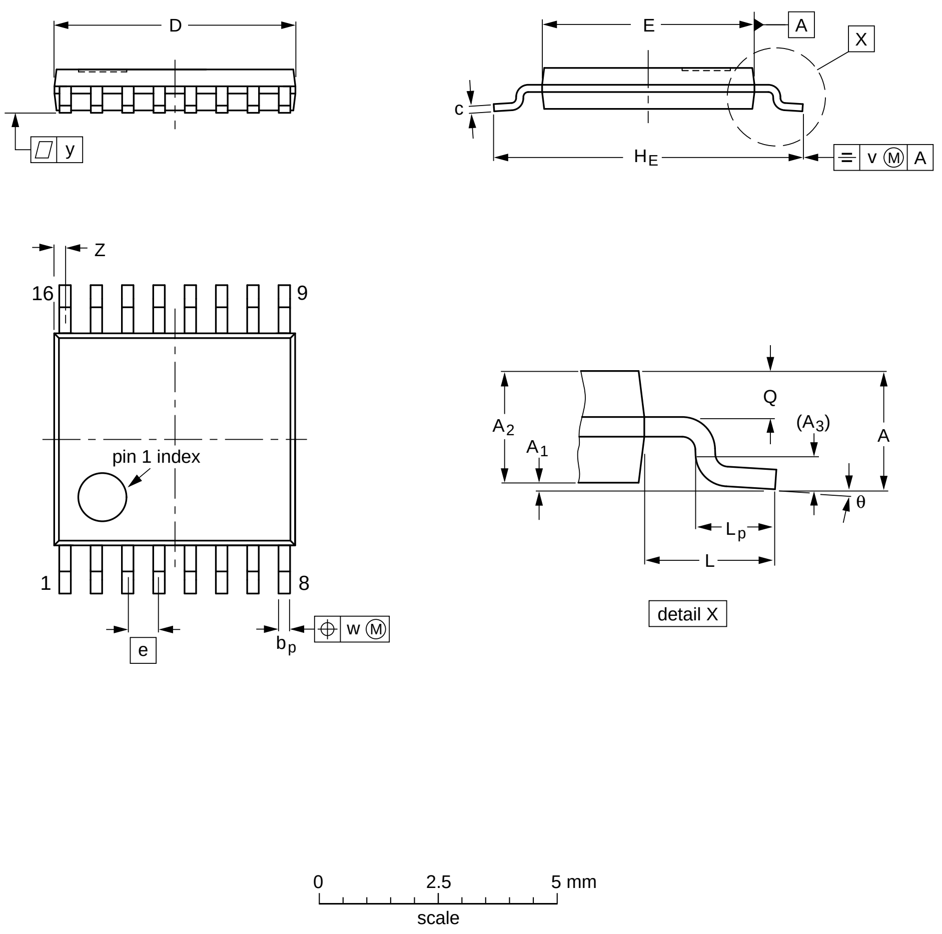
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 22. Package outline SOT109-1 (SO16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 23. Package outline SOT403-1 (TSSOP16)**

## 13. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4053B v.10 | 20111117 | Product data sheet | - | HEF4053B v.9 |
| Modifications: | • Legal pages updated.<br>• Changes in “General description”, “Features and benefits” and “Applications”. | | | |
| HEF4053B v.9 | 20100325 | Product data sheet | - | HEF4053B v.8 |
| HEF4053B v.8 | 20100224 | Product data sheet | - | HEF4053B v.7 |
| HEF4053B v.7 | 20091127 | Product data sheet | - | HEF4053B v.6 |
| HEF4053B v.6 | 20090924 | Product data sheet | - | HEF4053B v.5 |
| HEF4053B v.5 | 20090825 | Product data sheet | - | HEF4053B v.4 |
| HEF4053B v.4 | 20090713 | Product data sheet | - | HEF4053B_CNV v.3 |
| HEF4053B_CNV v.3 | 19950101 | Product specification | - | HEF4053B_CNV v.2 |
| HEF4053B_CNV v.2 | 19950101 | Product specification | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 16. Contents





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