850MHz, Low Distortion Programmable Gain Buffer Amplifiers

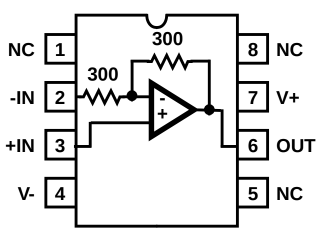
The HFA1112/12A are closed loop Buffers featuring user programmable gain and ultra high speed performance. Manufactured on Intersil's proprietary complementary bipolar UHF-1 process, these devices offer a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current. The HFA1112A is a more stable version optimized for unity gain applications.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

This amplifier is available with programmable output limiting as the HFA1113. For applications requiring a standard buffer pinout, please refer to the HFA1110 data sheet.

HFA1112 (PDIP, SOIC)
HFA1112A (SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 5, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
OUT	6	Output
V+	7	Positive Supply

Features

- User Programmable for Closed-Loop Gains of +1, -1 or +2 without Use of External Resistors
- HFA1112A Optimized for A_V = 1 Applications
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- Overdrive Recovery . . . . <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems
- Related Literature
  - AN9507, Video Cable Drivers Save Board Space

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1112IP	-40 to 85	8 Ld PDIP	E8.3
HFA1112IB (1112I)	-40 to 85	8 Ld SOIC	M8.15
HFA1112AIB (1112AIB)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	High Speed Op Amp DIP Evaluation Board		

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage . . . . V_{SUPPLY}
Output Current 60mA

Operating Conditions

Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	125	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Plastic Package) . . . . .150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage (Note 3)	100kHz	25	-	9	-	nV/√Hz
Non-Inverting Input Noise Current (Note 3)	100kHz	25	-	37	-	pA/√Hz
Non-Inverting Input Bias Current		25	-	25	40	µA
		Full	-	-	65	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance (Note 2)		25	240	300	360	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS						
Gain	A_V = +1, V_{IN} = +2V	25	0.980	0.990	1.02	V/V
		Full	0.975	-	1.025	V/V
Gain	A_V = +2, V_{IN} = +1V	25	1.96	1.98	2.04	V/V
		Full	1.95	-	2.05	V/V
DC Non-Linearity (Note 3)	A_V = +2, ±2V Full Scale	25	-	0.02	-	%
OUTPUT CHARACTERISTICS						
Output Voltage (Note 3)	A_V = -1	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (Note 3)	R_L = 50Ω	25, 85	50	60	-	mA
		-40	35	50	-	mA
Closed Loop Output Impedance	DC, A_V = +2	25	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (Note 3)		25	-	21	26	mA
		Full	-	-	33	mA
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 2, 3)	A_V = -1	25	450	800	-	MHz
	A_V = +1	25	500	850	-	MHz
	A_V = +2	25	350	550	-	MHz

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = $5V_{P-P}$, Note 2)	A_V = -1	25	1500	2400	-	V/µs
	A_V = +1	25	800	1500	-	V/µs
	A_V = +2	25	1100	1900	-	V/µs
Full Power Bandwidth (V_{OUT} = $5V_{P-P}$, Note 3)	A_V = -1	25	-	300	-	MHz
	A_V = +1	25	-	150	-	MHz
	A_V = +2	25	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 2, 3)	A_V = -1	25	-	±0.02	-	dB
	A_V = +1	25	-	±0.1	-	dB
	A_V = +2	25	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 2, 3)	A_V = -1	25	-	±0.05	-	dB
	A_V = +1	25	-	±0.2	-	dB
	A_V = +2	25	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 2, 3)	A_V = -1	25	-	±0.10	-	dB
	A_V = +2	25	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 3)	A_V = -1	25	-	±0.13	-	Degrees
	A_V = +1	25	-	±0.83	-	Degrees
	A_V = +2	25	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-52	-	dBc
	A_V = +1	25	-	-57	-	dBc
	A_V = +2	25	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-71	-	dBc
	A_V = +1	25	-	-73	-	dBc
	A_V = +2	25	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-47	-	dBc
	A_V = +1	25	-	-53	-	dBc
	A_V = +2	25	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-63	-	dBc
	A_V = +1	25	-	-68	-	dBc
	A_V = +2	25	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-41	-	dBc
	A_V = +1	25	-	-50	-	dBc
	A_V = +2	25	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = $2V_{P-P}$, Notes 2, 3)	A_V = -1	25	-	-55	-	dBc
	A_V = +1	25	-	-49	-	dBc
	A_V = +2	25	-	-62	-45	dBc
3rd Order Intercept (A_V = +2, Note 3)	100MHz	25	-	28	-	dBm
	300MHz	25	-	13	-	dBm
1dB Compression (A_V = +2, Note 3)	100MHz	25	-	19	-	dBm
	300MHz	25	-	12	-	dBm
Reverse Isolation (S_{12}, Note 3)	40MHz	25	-	-70	-	dB
	100MHz	25	-	-60	-	dB
	600MHz	25	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 2)	A_V = -1	25	-	500	800	ps
	A_V = +1	25	-	480	750	ps
	A_V = +2	25	-	700	1000	ps

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Rise Time (V_{OUT} = 2V Step)	A_V = -1	25	-	0.82	-	ns
	A_V = +1	25	-	1.06	-	ns
	A_V = +2	25	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 2, 3, 4)	A_V = -1	25	-	12	30	%
	A_V = +1	25	-	45	65	%
	A_V = +2	25	-	6	20	%
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	25	-	11	-	ns
0.05% Settling Time	V_{OUT} = 2V to 0V	25	-	15	-	ns
Overdrive Recovery Time	V_{IN} = $5V_{P-P}$	25	-	8.5	-	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.04	-	Degrees

NOTES:

2. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
3. See Typical Performance Curves for more information.
4. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Typical Performance Curves.

Application Information

Closed Loop Gain Selection

The HFA1112 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This “buffer” operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1 (Note)	Input	NC (Floating)
+2	Input	GND

NOTE: Use HFA1112A For Maximum Stability.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier’s inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier’s phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

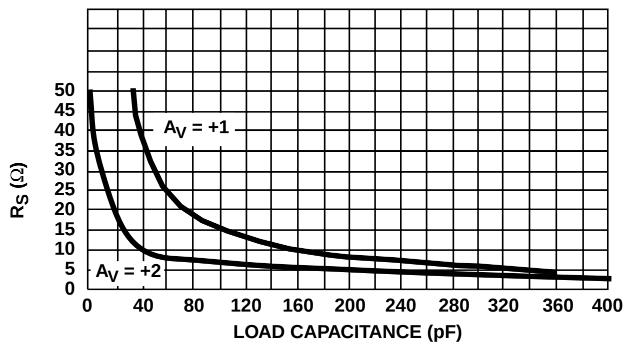


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1112 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

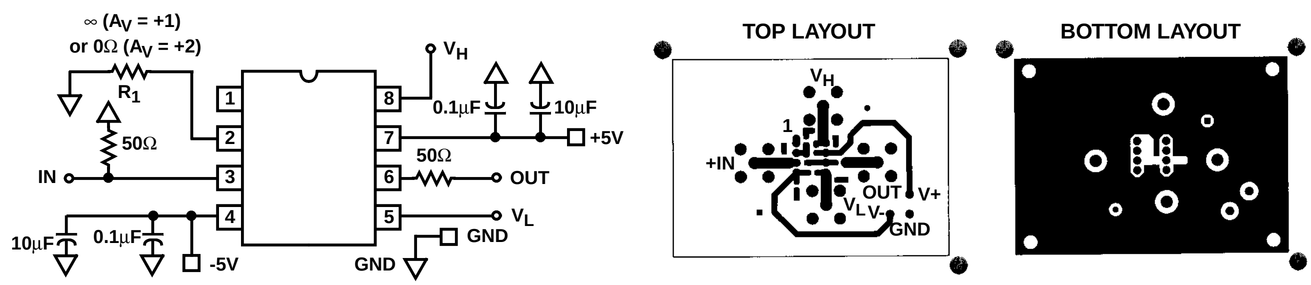


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves
$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

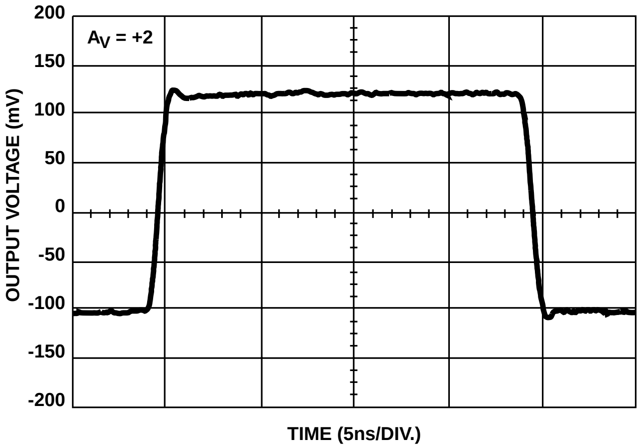


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

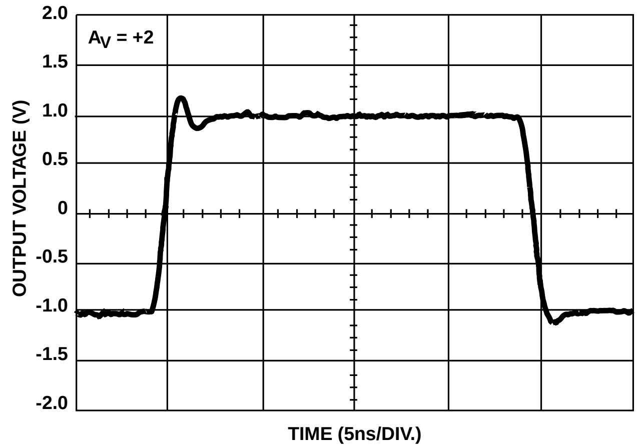


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

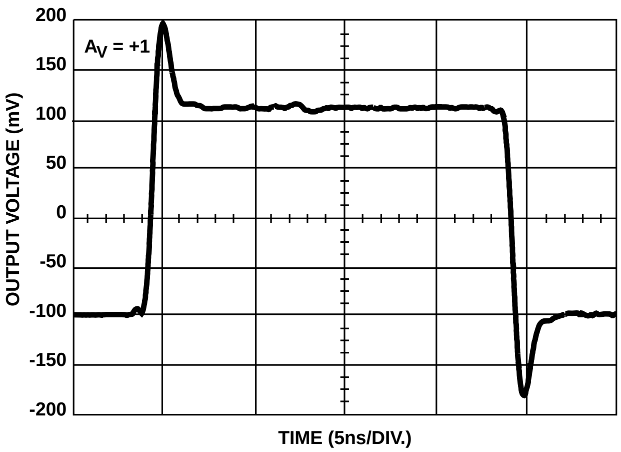


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

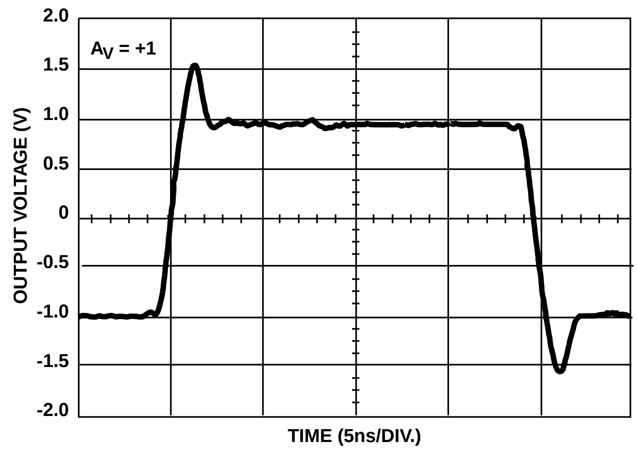


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

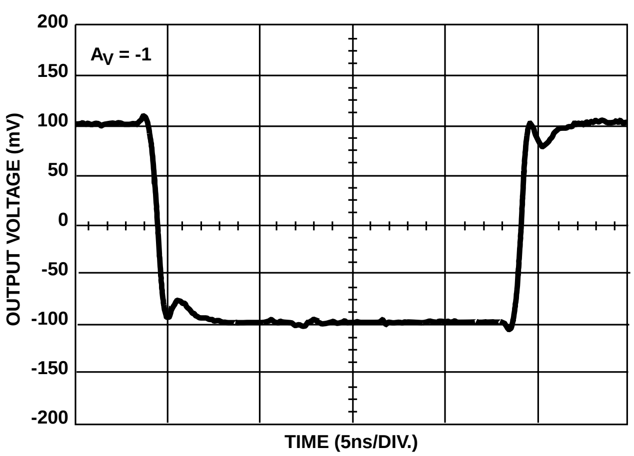


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

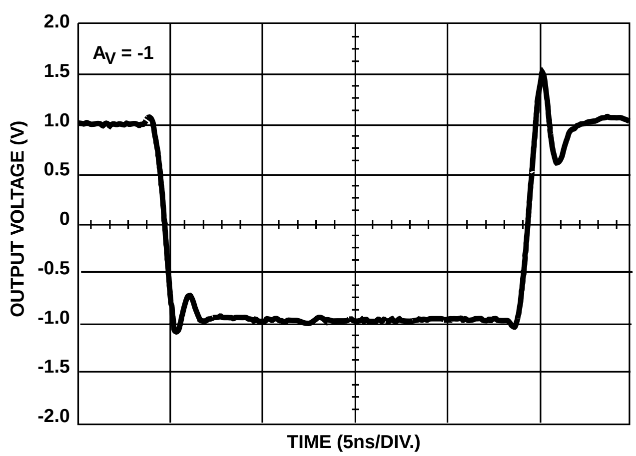


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

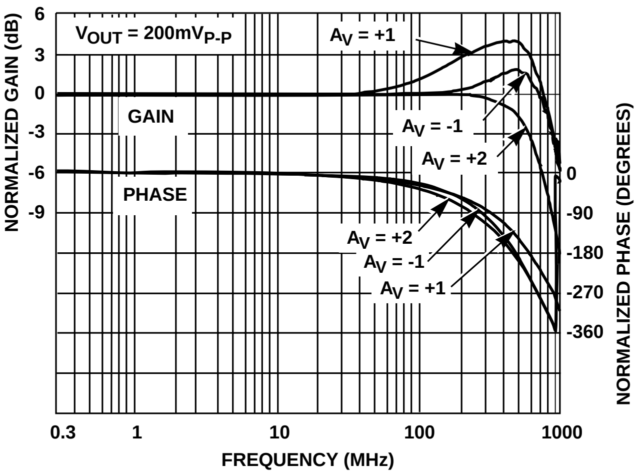


FIGURE 9. FREQUENCY RESPONSE

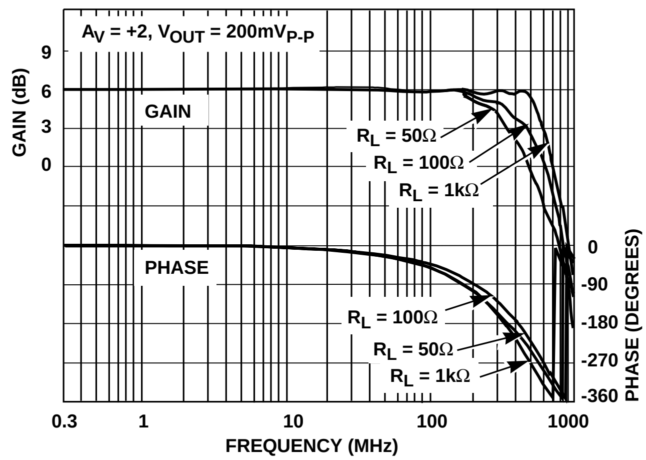


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

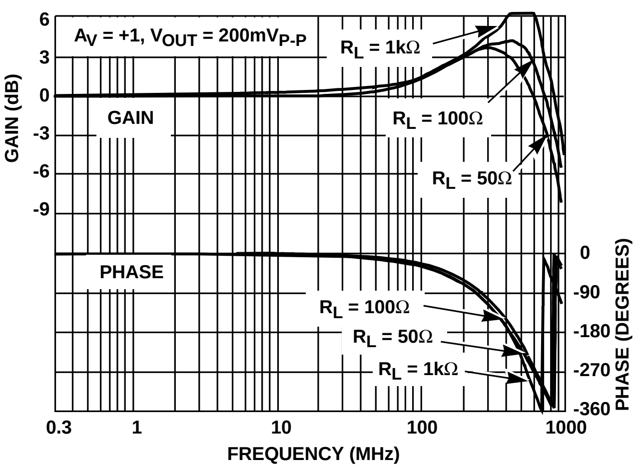


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

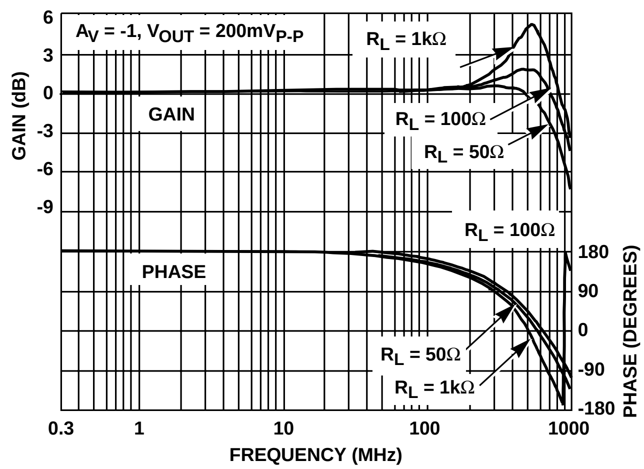


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

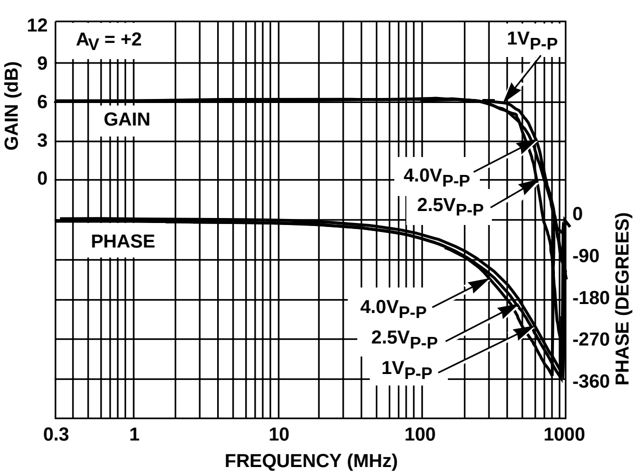


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

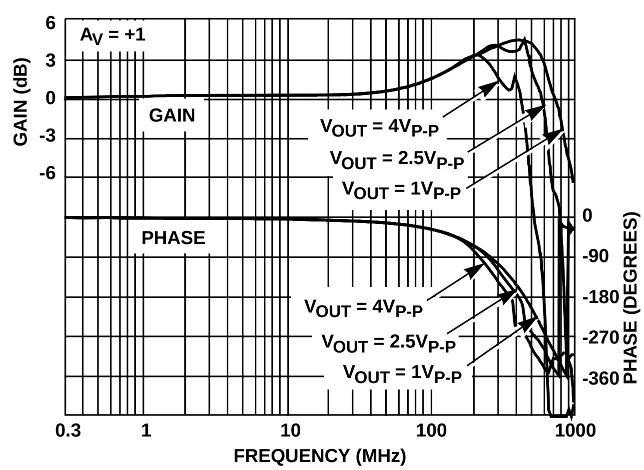


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

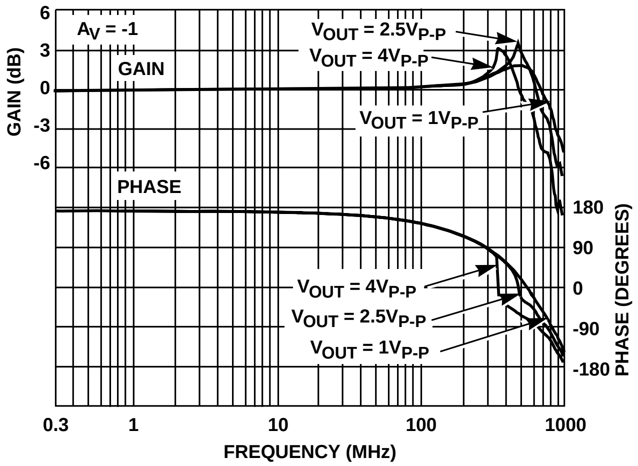


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

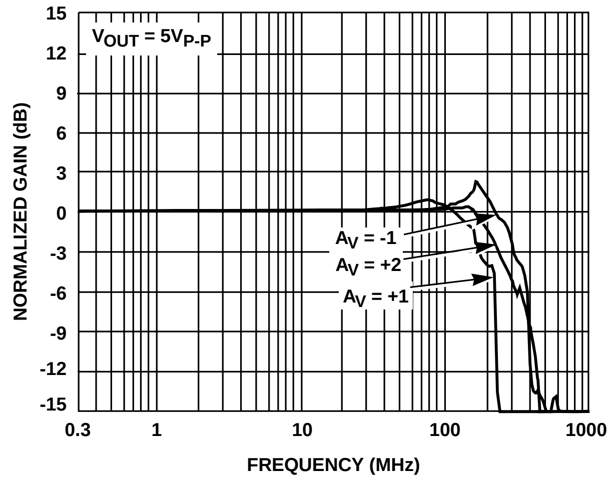


FIGURE 16. FULL POWER BANDWIDTH

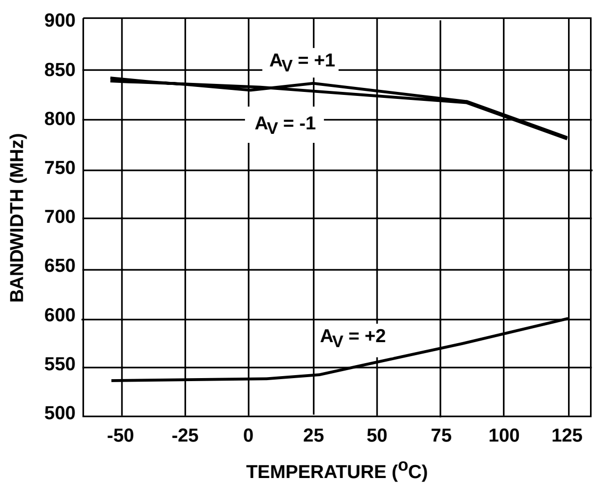


FIGURE 17. -3dB BANDWIDTH vs TEMPERATURE

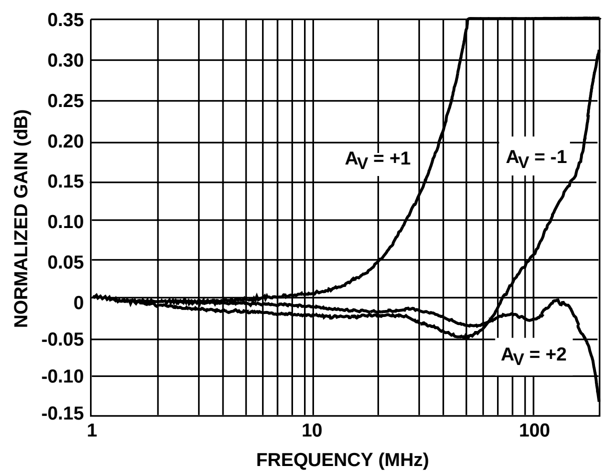


FIGURE 18. GAIN FLATNESS

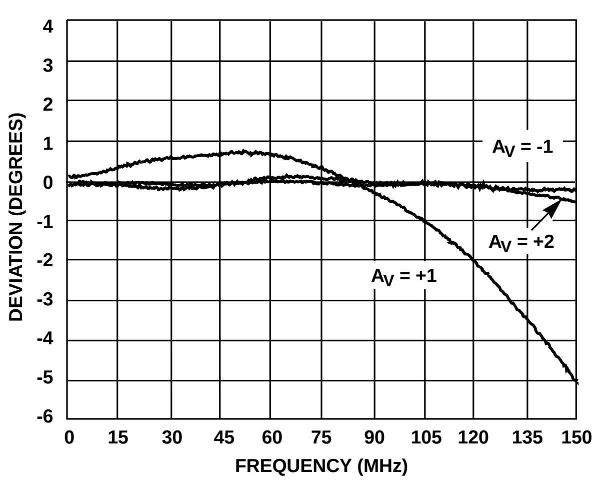


FIGURE 19. DEVIATION FROM LINEAR PHASE

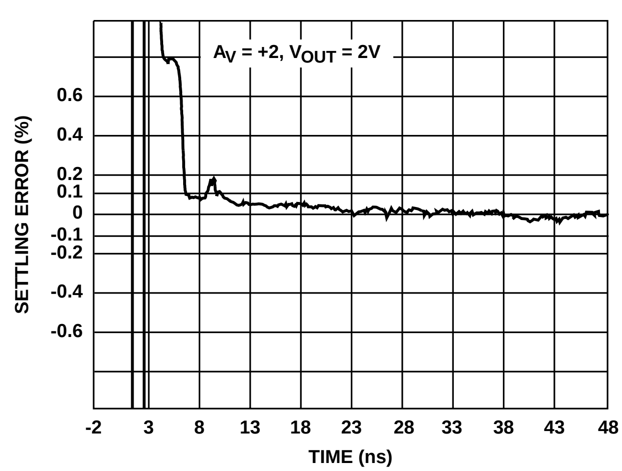


FIGURE 20. SETTLING RESPONSE

Typical Performance Curves
V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

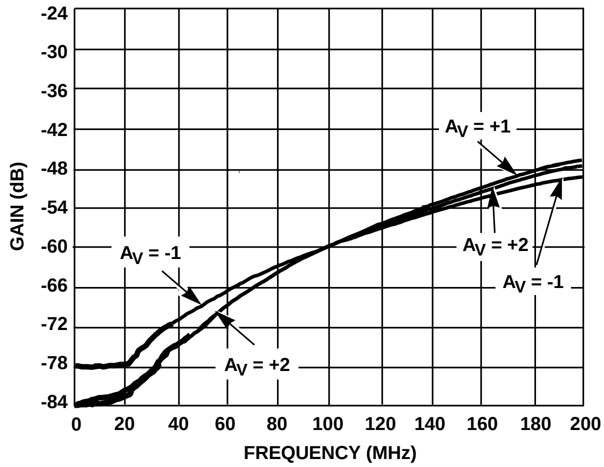


FIGURE 21. LOW FREQUENCY REVERSE ISOLATION (S_{12})

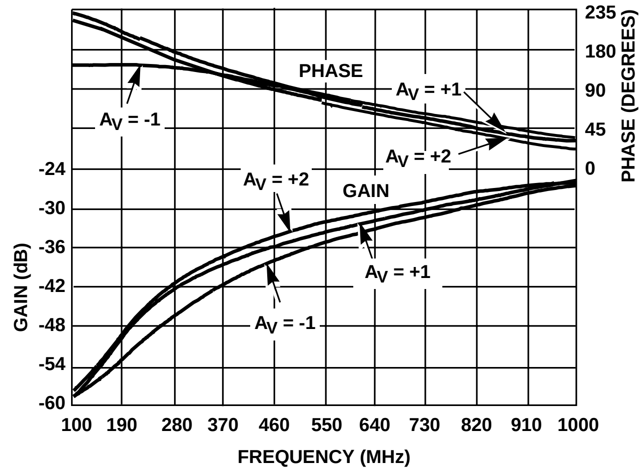


FIGURE 22. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

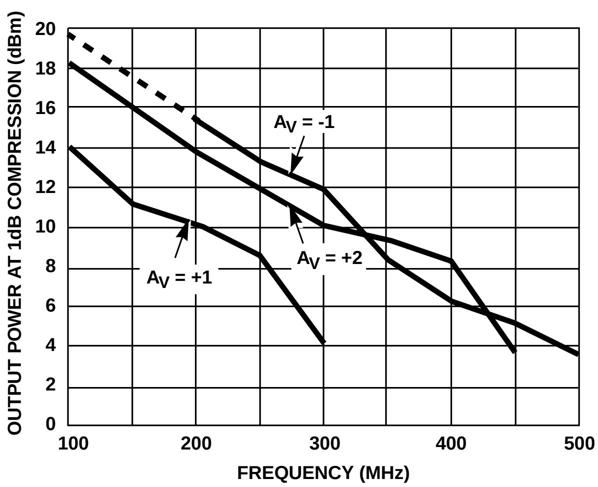


FIGURE 23. 1dB GAIN COMPRESSION vs FREQUENCY

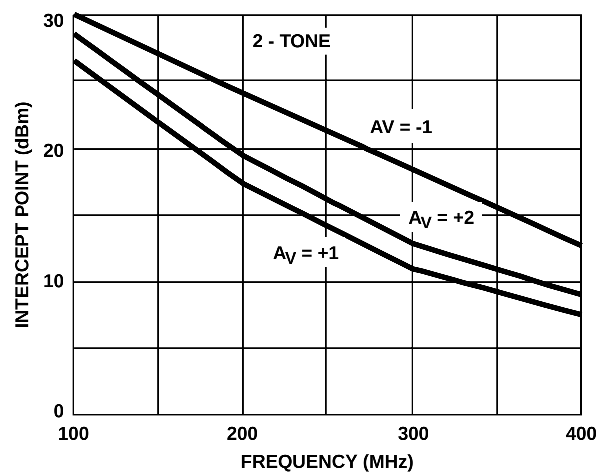


FIGURE 24. 3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY

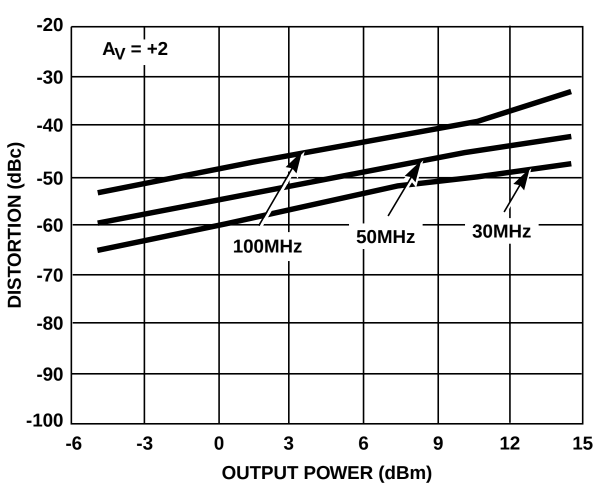


FIGURE 25. 2nd HARMONIC DISTORTION vs P_{OUT}

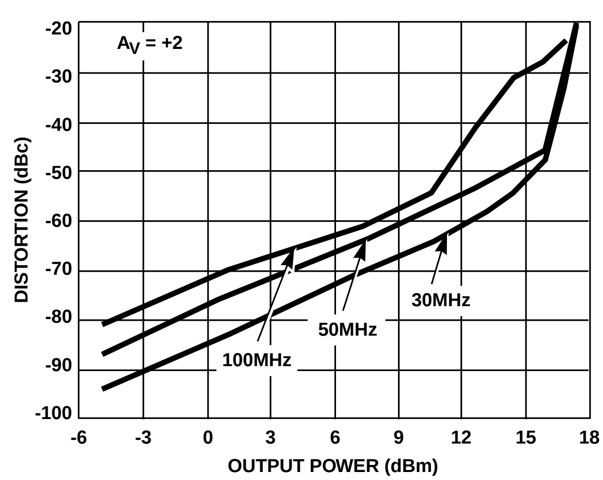


FIGURE 26. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

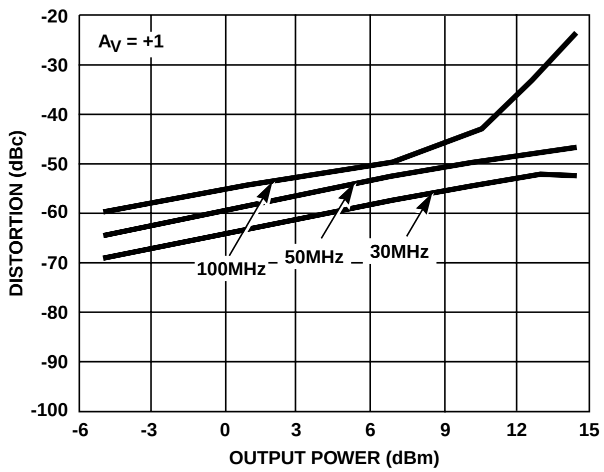


FIGURE 27. 2nd HARMONIC DISTORTION vs P_{OUT}

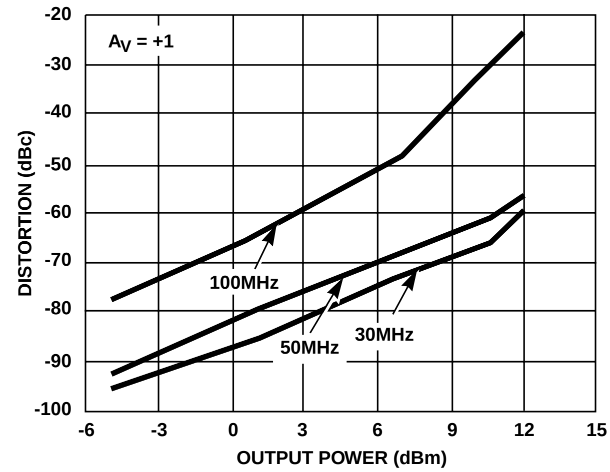


FIGURE 28. 3rd HARMONIC DISTORTION vs P_{OUT}

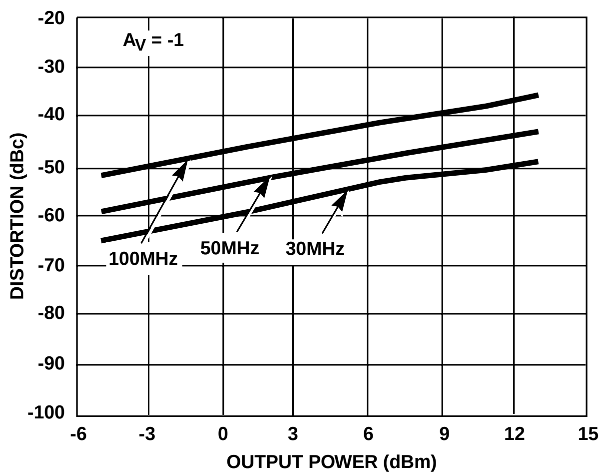


FIGURE 29. 2nd HARMONIC DISTORTION vs P_{OUT}

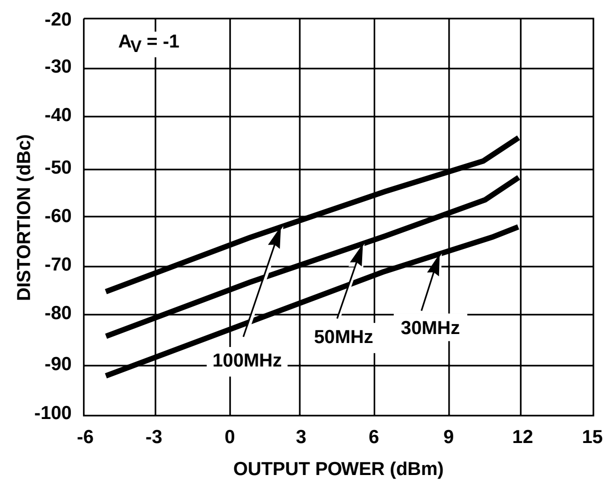


FIGURE 30. 3rd HARMONIC DISTORTION vs P_{OUT}

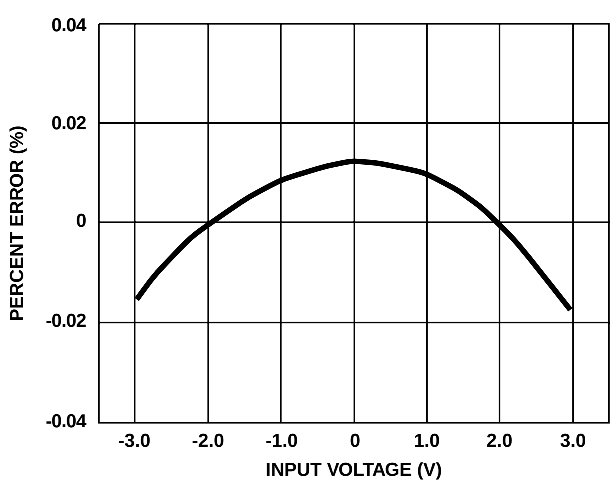


FIGURE 31. INTEGRAL LINEARITY ERROR

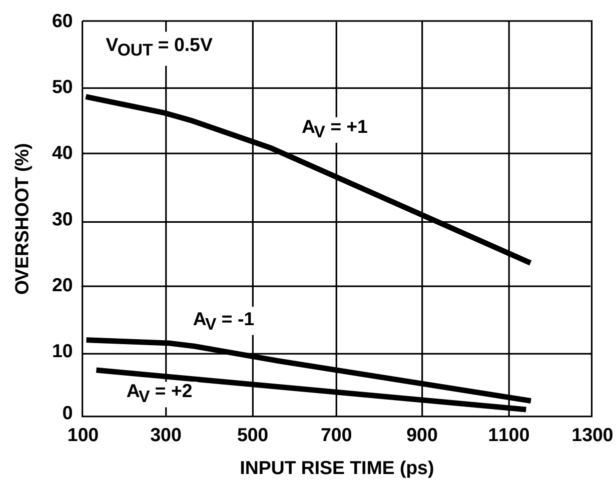


FIGURE 32. OVERSHOOT vs INPUT RISE TIME

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

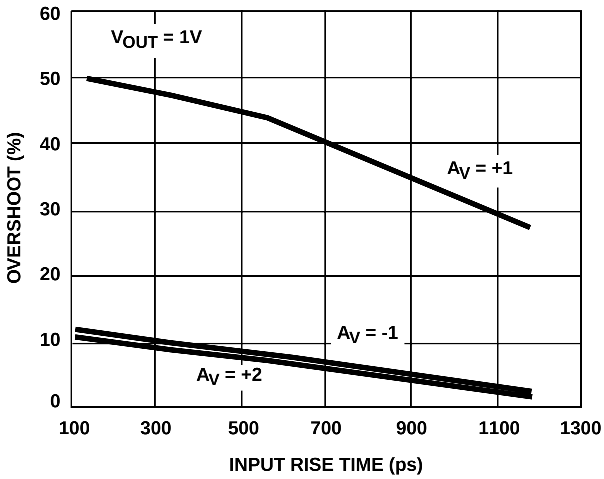


FIGURE 33. OVERSHOOT vs INPUT RISE TIME

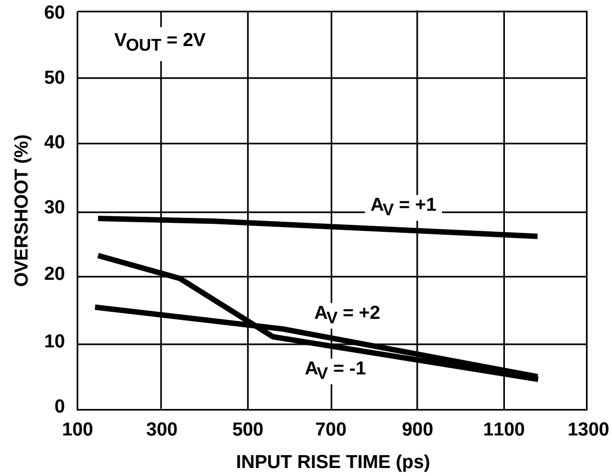


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

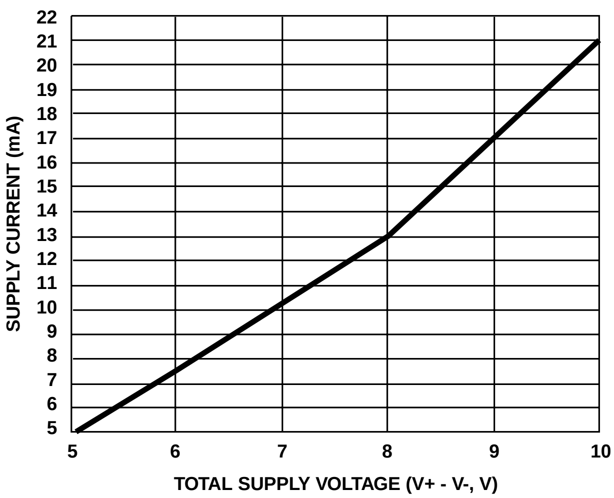


FIGURE 35. SUPPLY CURRENT vs SUPPLY VOLTAGE

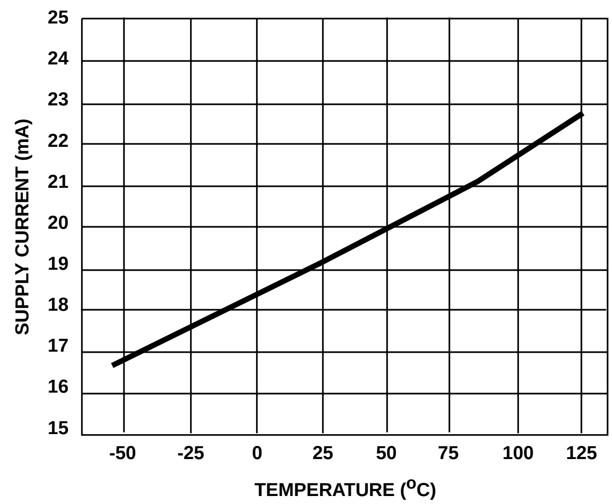


FIGURE 36. SUPPLY CURRENT vs TEMPERATURE

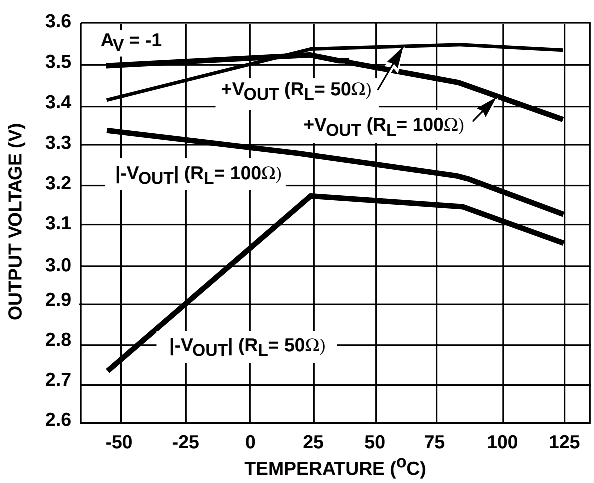


FIGURE 37. OUTPUT VOLTAGE vs TEMPERATURE

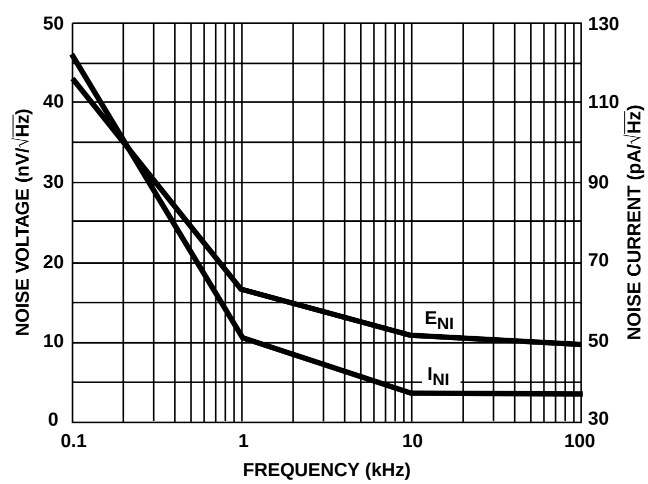


FIGURE 38. INPUT NOISE CHARACTERISTICS

Die Characteristics

DIE DIMENSIONS

63 mils x 44 mils x 19 mils
1600µm x 1130µm 483µm

METALLIZATION

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT

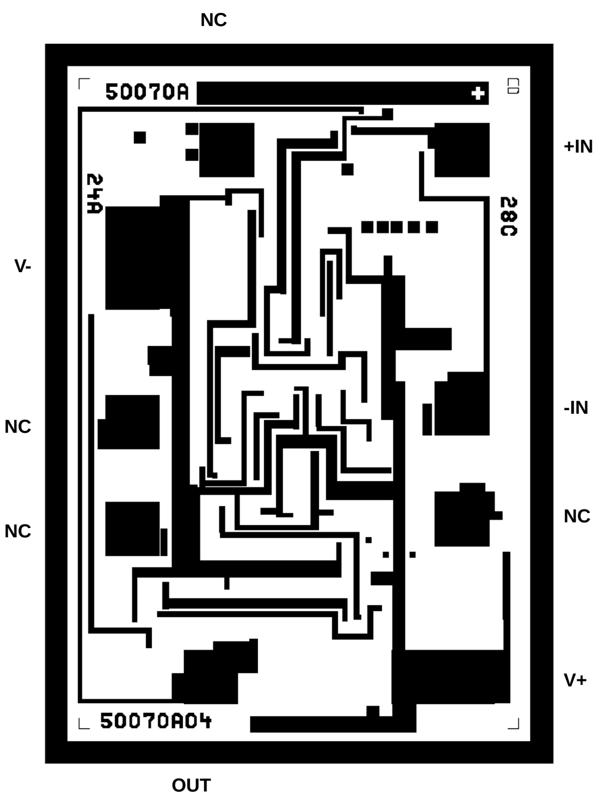
52

SUBSTRATE POTENTIAL (POWERED UP)

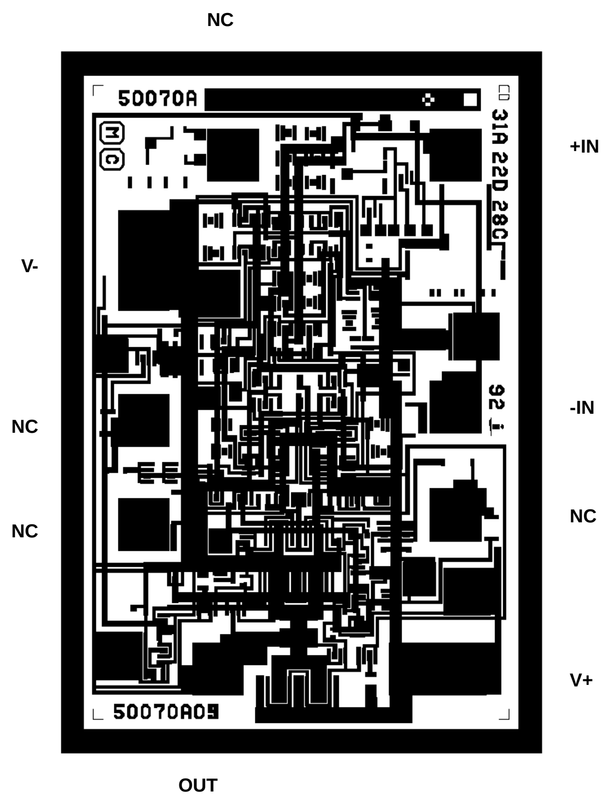
Floating (Recommend Connection to V-)

Metallization Mask Layouts

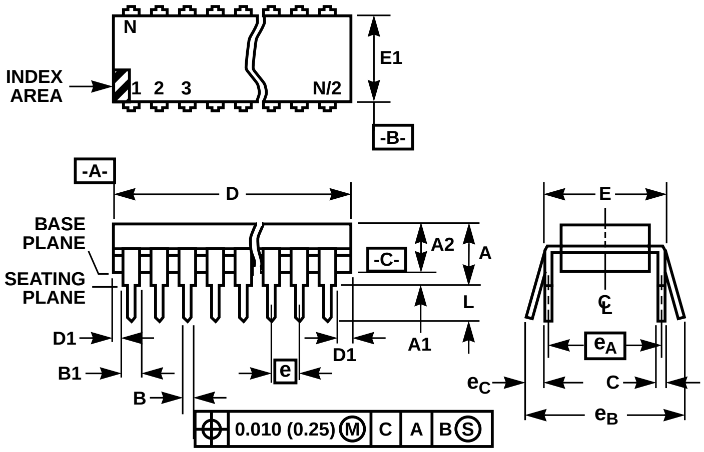
HFA1112



HFA1112A



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3A (JEDEC MS-001-AC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.880	0.920	33.27	34.65	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

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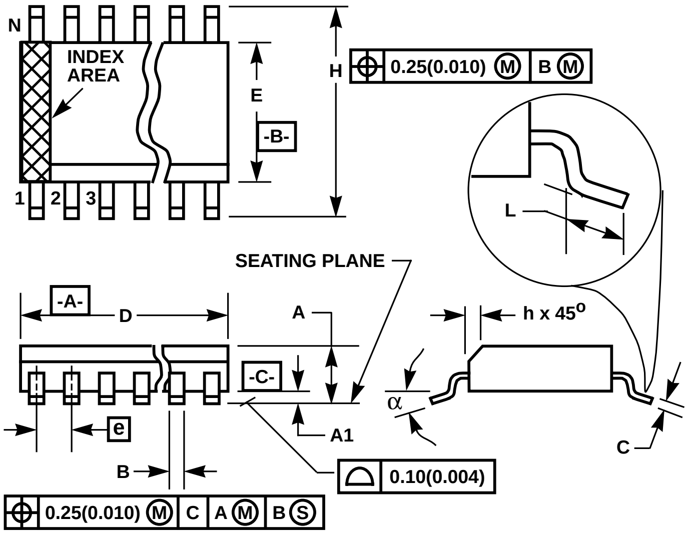
Small Outline Plastic Packages (SOIC)



M8.15 **(JEDEC MS-012-AA ISSUE C)**
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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