HI-7159A

Microprocessor-Compatible, 5-1/2 Digit A/D Converter

FN2936
Rev 4.00
January 1999

The Intersil HI-7159A is a monolithic A/D converter that uses a unique dual slope technique which allows it to resolve input changes as small as 1 part in 200,000 (10µV) without the use of critical external components. Its digital autozeroing feature virtually eliminates zero drift over temperature. The device is fabricated in Intersil' proprietary low noise BiMOS process, resulting in exceptional linearity and noise performance. The HI-7159A's resolution can be switched between a high resolution 200,000 count ($5^1/_2$ digit) mode, and a high speed 20,000 count ($4^1/_2$ digit) mode without any hardware modifications. In the $4^1/_2$ digit uncompensated mode, speeds of 60 conversions per second can be achieved. The HI-7159A is designed to be easily interfaced with most microprocessors through either of its three serial and one parallel interface modes. In the serial modes, any one of four common baud rates is available.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3-7159A-5	0 to 70	28 Ld PDIP	E28.6

Features

- ±200,000 Count A/D Converter
- 2V Full Scale Reading With 10µV Resolution
- 15 Conversions Per Second in $5^1/_2$ Digit Mode
- 60 Conversions Per Second in $4^1/_2$ Digit Mode
- Serial or Parallel Interface Modes
- Four Selectable Baud Rates
- Differential Analog Input
- Differential Reference Input
- Digital Autozero

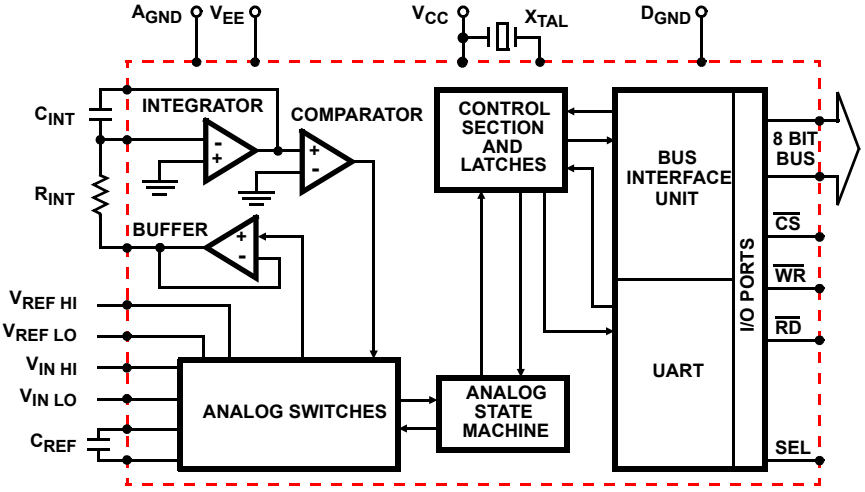
Applications

- Weigh Scales
- Part Counting Scales
- Laboratory Instruments
- Process Control/Monitoring
- Energy Management
- Seismic Monitoring

Pinout

HI-7159A
(PDIP)
TOP VIEW

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{CC} to GND (A_{GND}/D_{GND}) . . . . . -0.3V < V_{CC} < +6V
- V_{EE} to GND (A_{GND}/D_{GND}) . . . . . +0.3V < V_{CC} < -6V

Digital Pins, (pins 15 - 28) . . . . . D_{GND} -0.3V < V_D <V_{CC} +0.3V

Analog Pins, (pins 2 - 13). . . . . V_{EE} -0.3V < V_A < V_{CC} +0.3V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	50

Maximum Junction Temperature . . . . . 150^oC

Maximum Storage Temperature, T_{STG} . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Range. . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V, V_{EE} = -5V, D_{GND} = 0V, A_{GND} = 0V, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = AGND, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, T_A = 25^oC, $V_{IN\ LO}$ = A_{GND}, C_{REF} = 1.0µF, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Integral Non-Linearity, INL	0V to +2V (Notes 2, 3, 4, 5)	-	±0.0015	±0.0035	% FS
	-2V to 0V (Notes 2, 3, 4, 5)	-	±0.0015	±0.0035	% FS
Ratiometric Reading	$V_{IN\ HI}$ = $V_{REF\ HI}$ = 1.00000V	99996	100000	100003	Counts
Zero Error, ZE	$V_{IN\ HI}$ = 0.00000V	-	0	±1	Counts
Voltage Range of $V_{IN\ LO}$ Input (Pin 13), $V_{IN\ LO}$	-2V ≤ $V_{IN\ HI}$ - $V_{IN\ LO}$ ≤ 2V	-1	-	1	V
Voltage Range of $V_{IN\ HI}$ Input (Pin 12), $V_{IN\ HI}$	-2V ≤ $V_{IN\ HI}$ - $V_{IN\ LO}$ ≤ 2V	$V_{IN\ LO}$-2V	-	$V_{IN\ LO}$ +2V	V
Common Mode Rejection, CMR	$V_{IN\ HI}$ = $V_{IN\ LO}$ = -3V to +3V	-	3	-	Counts
Input Leakage Current, I_{IN}	Pins 9, 10, 12, 13, V_{IN} = +3V, -3V	-	-	±0.1	µA
Input Capacitance, C_{IN}	Pins 9, 10, 12, 13	-	5	-	pF
Noise (Peak-to-Peak Value, Not Exceeded 95% of Time), e_N		-	±1	-	Counts
Zero Drift, $T_{C(ZE)}$	$V_{IN\ HI}$ = 0.00000V	-	0	-	Counts/^oC
Full Scale Error Tempco, $T_{C(FSE)}$	$V_{IN\ HI}$ = ±2.00000V	-	±0.1	-	Counts/^oC
Supply Range, V_{SUPPLY}					
V_{CC}		+4.75	+5.0	+5.5	V
V_{EE}		-4.75	-5.0	-5.5	V
V_{CC} Supply Current, I_{CC}		-	-	10	mA
V_{EE} Supply Current, I_{EE}		-	-	4.5	mA
Digital GND Current, I_{DGND}		-	-	5.5	mA
Analog GND Current, I_{AGND}		-	+3	-	µA
V_{CC}, V_{EE} Power Supply Rejection, PSR	$V_{IN\ HI}$ = $V_{REF\ HI}$ = 1.00000V, V_{CC} = +4.75V, V_{EE} = -4.75V to V_{CC} = +5.50V, V_{EE} = -5.50V	-	3	-	Counts
Guard Driver Pins 5, 8 Output Current, I_{OGD}	V_{IN} (Pins 9, 10) = +3V, -3V	±10	-	-	µA

NOTES:

2. All typical values have been characterized but are not production tested.
3. Not production tested, guaranteed by design and characterization.
4. Reference adjusted for correct full-scale reading.
5. V_{IN} = $V_{IN\ HI}$ - $V_{IN\ LO}$.

DC Electrical Specifications

Test Conditions: V_{CC} = +5V, V_{EE} = -5V, D_{GND} = 0V, A_{GND} = 0V, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = A_{GND}, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, T_A = 25°C, $V_{IN\ LO}$ = A_{GND}, C_{REF} = 1.0µF, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage, V_{IL}	Pins 15-25, 28	-	-	0.8	V
Input High Voltage, V_{IH}	Pins 15-25, 28	2.0	-	-	V
Output Low Voltage, V_{OL}	Pins 16, 18-25, I_{OL} = 1.6mA	-	-	0.4	V
Output High Voltage, V_{OH}	Pins 16, 18-25, I_{OH} = -400µA	2.4	-	-	V
Three-State Leakage Current, Pins 18-25, I_{OL}	All Digital Drivers In High Impedance State, Parallel Mode. CS = V_{CC}, V_{IN} = 0V, V_{CC}	-	-	±10	µA
Leakage, Pins 15-17, 28, I_{IN}	V_{IN} = 0V, V_{CC}	-	-	±1	µA
Input Capacitance, C_{IN}	Pins 15, 17-25, 28	-	5	-	pF
	Pin 16	-	10	-	pF
Input Pullup Current (Pins 18-25), I_{PU}	Pins 18-25 at D_{GND} SEL = D_{GND} (Serial Modes)	-	-5	-	µA

AC Electrical Specifications

T_A = 0°C to 75°C; Test Conditions: V_{CC} = +4.75V, V_{EE} = -5.00V (Note 8), D_{GND} = 0V, A_{GND} = 0V, $V_{IN\ LO}$ = A_{GND}, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = A_{GND}, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, V_{IL} = 0V, V_{IH} = 4V, V_{OL} = V_{OH} = 1.5V, t_r = t_f < 10ns, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Setup/Hold of $\overline{WR}$, t_1		0	-	-	ns
$\overline{WR}$ Setup of Data In, t_2		50	-	-	ns
$\overline{WR}$ Pulse Width, t_3		150	-	-	ns
Data Hold After $\overline{WR}$, t_4		20	-	-	ns
$\overline{CS}$ Setup/Hold of $\overline{RD}$, t_5	(Note 7)	25	-	-	ns
$\overline{RD}$ to Data Out, t_6	C_L = 50pF, V_O = 1.5V	-	-	100	ns
$\overline{RD}$ to Hi-Z State, t_7		-	-	70	ns
$\overline{WR}$ to $\overline{RD}$, $\overline{WR}$ to $\overline{WR}$, t_A	(Note 7)	$5/f_{CLOCK}$	-	-	s
$\overline{RD}$ to $\overline{WR}$, t_B	(Note 7)	200	-	-	ns
RXD Setup of Data In, t_C	(Note 7)	60	-	-	ns
Data Hold After EXT CLK, t_D		40	-	-	ns
EXT CLK to DATA OUT, t_E		-	-	300	ns
$\overline{CS}$ Setup of TXD, t_f		100	-	-	ns

NOTES:

6. All typical values have been characterized but are not production tested.
7. Not production tested, guaranteed by design and characterization.
8. All AC characteristics are guaranteed for V_{CC} = +5V 15%, V_{EE} = -5V 15%, over T_A = 0°C to 75°C.

Timing Waveforms

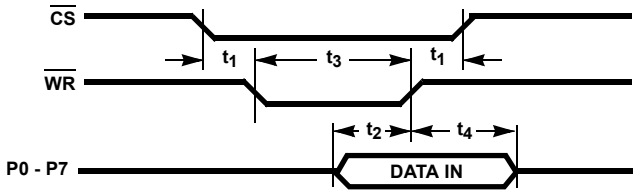


FIGURE 1A. WRITE

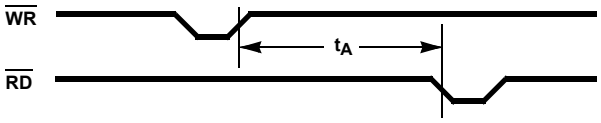


FIGURE 1B. WRITE TO READ CYCLE

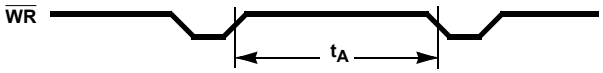


FIGURE 1C. WRITE TO WRITE CYCLE

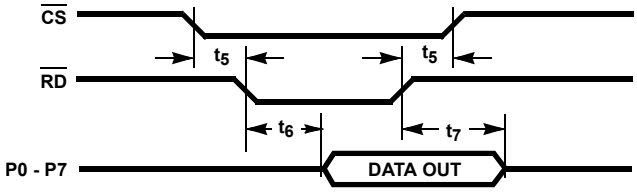


FIGURE 1D. READ

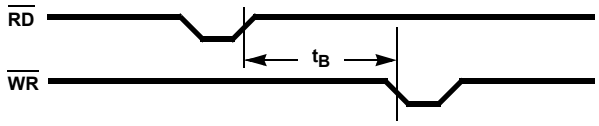


FIGURE 1E. READ TO WRITE CYCLE

FIGURE 1. PARALLEL MODE TIMING

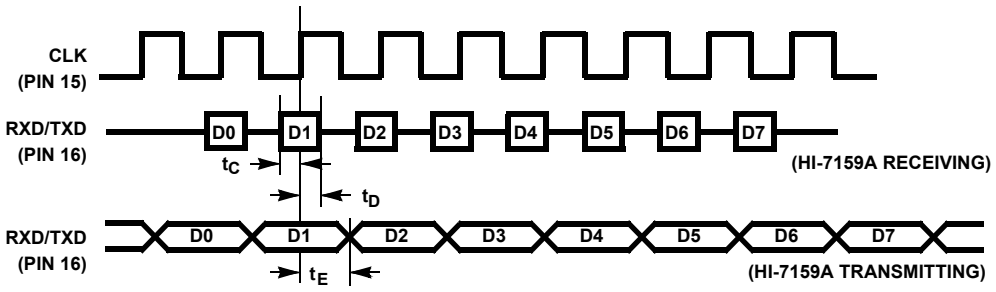
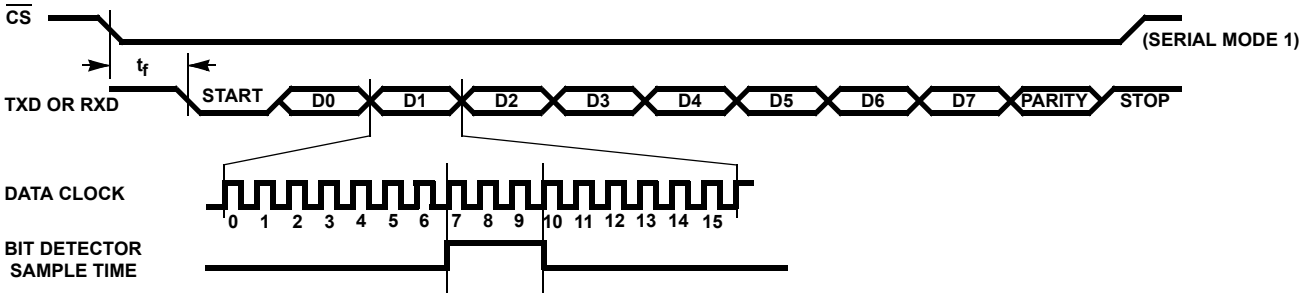


FIGURE 2A. SERIAL MODE 0 TIMING



NOTE: All input timing shown is defined at 50% points.

FIGURE 2B. SERIAL MODE TIMING

Pin Descriptions

<table>
<tr><th>PIN</th><th>SYMBOL</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>V_{CC}</td><td>Positive 5V Power Supply for analog and digital sections.</td></tr>
<tr><td>2</td><td>INT OUT</td><td>Integrator Output; external component terminal.</td></tr>
<tr><td>3</td><td>INT IN</td><td>Integrator Input; external component terminal.</td></tr>
<tr><td>4</td><td>BUF OUT</td><td>$V_{IN\ HI}$ Voltage Buffer Output; external component terminal.</td></tr>
<tr><td>5</td><td>C_{REF}- Guard</td><td>Reference Capacitor guard ring terminal (negative).</td></tr>
<tr><td>6</td><td>C_{REF}-</td><td>Reference Capacitor negative terminal.</td></tr>
<tr><td>7</td><td>C_{REF}+</td><td>Reference Capacitor positive terminal.</td></tr>
<tr><td>8</td><td>C_{REF}+ Guard</td><td>Reference Capacitor guard ring terminal (positive).</td></tr>
<tr><td>9</td><td>$V_{REF\ HI}$</td><td>Positive Reference Input terminal.</td></tr>
<tr><td>10</td><td>$V_{REF\ LO}$</td><td>Negative Reference Input terminal.</td></tr>
<tr><td>11</td><td>A_{GND}</td><td>Analog Ground (0V).</td></tr>
<tr><td>12</td><td>$V_{IN\ HI}$</td><td>Positive Analog Input Voltage terminal.</td></tr>
<tr><td>13</td><td>$V_{IN\ LO}$</td><td>Negative Analog Input Voltage terminal.</td></tr>
<tr><td>14</td><td>V_{EE}</td><td>Negative 5V Power Supply for analog section.</td></tr>
<tr><td>15</td><td>$\overline{RD}$/RXD</td><td>Parallel Read; serial receive (modes 1 and 2), serial clock (mode 0).</td></tr>
<tr><td>16</td><td>$\overline{WR}$/TXD</td><td>Parallel Write; serial transmit (modes 1 and 2), serial receive/transmit (mode 0).</td></tr>
<tr><td>17</td><td>$\overline{CS}$/SAD4</td><td>Chip Select (parallel and serial modes 0 and 1), serial address bit 4 (mode 2).</td></tr>
<tr><td>18</td><td>P0/SMS0</td><td>Parallel I/O Port (P0); serial mode select pin.</td></tr>
<tr><td>19</td><td>P1/SMS1</td><td>Parallel I/O Port (P1); serial mode select pin.
<table>
<tr><th>MODE</th><th>SMS0</th><th>SMS1</th></tr>
<tr><td>Serial Mode 0</td><td>0</td><td>0</td></tr>
<tr><td>Serial Mode 1</td><td>0</td><td>1</td></tr>
<tr><td>Serial Mode 2</td><td>1</td><td>0</td></tr>
<tr><td>Reserved</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>20</td><td>P2/SAD0</td><td>Parallel I/O Port (P2); serial address bit 0.</td></tr>
<tr><td>21</td><td>P3/SAD1</td><td>Parallel I/O Port (P3); serial address bit 1.</td></tr>
<tr><td>22</td><td>P4/SAD2</td><td>Parallel I/O Port (P4); serial address bit 2.</td></tr>
<tr><td>23</td><td>P5/SAD3</td><td>Parallel I/O Port (P5); serial address bit 3.</td></tr>
<tr><td>24</td><td>P6/BRS0</td><td>Parallel I/O Port (P6); serial baud rate select.</td></tr>
<tr><td>25</td><td>P7/BRS1</td><td>Parallel I/O Port (P7); serial baud rate select.
<table>
<tr><th>BAUD RATE</th><th>BRS0</th><th>BRS1</th></tr>
<tr><td>300</td><td>0</td><td>0</td></tr>
<tr><td>1200</td><td>0</td><td>1</td></tr>
<tr><td>9600</td><td>1</td><td>0</td></tr>
<tr><td>19200</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>26</td><td>D_{GND}</td><td>Digital Ground (0V).</td></tr>
<tr><td>27</td><td>X_{TAL}</td><td>Oscillator Out; crystal connection pin (other crystal pin connected to V_{CC}).</td></tr>
<tr><td>28</td><td>SEL</td><td>Select pin for parallel or serial operation.
Parallel SEL = 1
Serial Modes SEL = 0</td></tr>
</table>

Theory of Operation

The HI-7159A attains its $5^1/_2$ digit resolution through the use of multiple integrations per conversion, creating an effective integrator swing greater than the supply rails, and a successive integration technique used to measure the residue on the integrator capacitor to $5^1/_2$ digit accuracy.

In the $5^1/_2$ digit mode, the input voltage is integrated and reference de-integrated four times. This results in a count with the same effective resolution as a single integration with four times the integrator swing amplitude. In this manner effective integrator swings of ±12V or greater can be achieved with ±5V supplies. The four integrations are spaced so that common-mode signals whose frequency is an integer multiple of $f_{CRYSTAL}/40,000$ are rejected. In the $4^1/_2$ digit mode, only one input integration is performed, thus the minimum frequency for common-mode rejection becomes $f_{CRYSTAL}/10,000$.

These first four integrations measure the input voltage to an resolution of $3^1/_2$ digits, or 1mV/count. To achieve $5^1/_2$ digit accuracy (10µV/count), the error voltage remaining on the integrator capacitor (representing the overshoot of the integrator due to comparator delay and clock quantization) must be measured and subtracted from the $3^1/_2$ digit result. This is accomplished by multiplying the residue by a factor of 10, then integrating and reference de-integrating the error. This error is subtracted from the $3^1/_2$ digit result, yielding a $4^1/_2$ digit accurate result. The error remaining from this step is then multiplied by 10 and subtracted, and the process is repeated a third time to achieve an internal accuracy of $6^1/_2$ digits. This result is rounded to $5^1/_2$ digits and transferred to the holding register, where it can be accessed by the user through one of the three communications modes.

Conversion Types

The HI-7159A offers the user a choice of three different conversion types. They are: (1) the converter's internal offset voltage, measured by internally connecting $V_{IN\ HI}$ and $V_{IN\ LO}$ to A_{GND} and doing a conversion (Error Only Mode); (2) the input voltage ($V_{IN\ HI}$ minus $V_{IN\ LO}$) including the converter's internal offset (Uncompensated Mode); and (3) the input voltage including internal offset errors, minus the internal offset errors (Compensated Mode). This last measurement is a digital subtraction of an Error Only conversion from an Uncompensated conversion, and is the default conversion type. Since a Compensated conversion consists of two conversions, it takes twice as long to perform as the first two types.

Under some conditions, it may be desirable to increase the conversion rate without loss of resolution or accuracy. Since the short term drift of the internal offset error is slight when temperature is controlled, it is not always necessary to convert the error voltage once for every input voltage conversion. It is possible for the host processor to do an error conversion periodically, store the result, and subtract the error from a stream of uncompensated input conversions with its own internal ALU. In this way the conversion rate can be effectively doubled.

Communication Modes

The HI-7159A A/D converter receives instructions from and transmits data to the user host processor through one of four communication modes. The modes are: parallel microprocessor (Parallel); synchronous serial (Serial Mode 0); serial non-addressed (Serial Mode 1); and serial addressed (Serial Mode 2). The mode is determined by the states of the SEL, SMS0, and SMS1 pins as shown in Table 1.

The parallel mode allows the converter to be attached directly to a microprocessor data bus. Data is read and written to the device under control of the microprocessor's $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ signals. Serial Mode 0 permits high speed serial data transfer at up to 1 megabits/s. Serial Mode 1 reads and writes industry standard serial data packets consisting of 1 start bit, 8 data bits, 1 parity bit (EVEN), and 1 stop bit, at one of 4 hardware selectable baud rates. Serial Mode 2 is identical to Serial Mode 1 with the addition of addressing capabilities which allow up to 32 HI-7159As to share the same serial line, with each assigned a unique address.

TABLE 1. COMMUNICATION MODE SELECTION

COMMUNICATION MODE	SEL PIN 28	SM S0 PIN 18	SM S1 PIN 19
Parallel	V_{CC}	N/A	N/A
Serial 0	D_{GND}	D_{GND}	D_{GND}
Serial 1	D_{GND}	D_{GND}	V_{CC}
Serial 2	D_{GND}	V_{CC}	D_{GND}

All four modes follow the same interface protocol: a request or a command is sent from the host to the HI-7159A, and the converter responds with the requested data and, in the case of a command, begins a new conversion.

Parallel Mode Operation

The parallel communication mode (Figure 3) is selected when SEL (Pin 28) is high. Pins 18-25 become the eight bidirectional data bits, P0-P7. Pins 15, 16, and 17 respectively become read ($\overline{RD}$), write ($\overline{WR}$), and chip select ($\overline{CS}$). Timing parameters for the parallel mode are shown in Figure 1.

Serial Mode 0

Serial Mode 0 is the high speed synchronous serial interface, directly compatible with the MCS-51 series of microcontrollers. It is enabled by tying SEL (Pin 28), SMS0 (Pin 18) and SMS1 (Pin 19) low (Figure 4A). Pin 16 is the bidirectional serial data path, and pin 15 is the data clock input. Data sent to the HI-7159A is latched on the rising edge of the serial clock. See Figure 2A for detailed timing information.

Only 8 data bits are used in this mode - no start, stop, or parity bits are transmitted or received. $\overline{CS}$ must either be tied to D_{GND} or pulled low to access the device. The SAD0 - SAD3 and BRS0 - BRS1 pins are unused in this mode and should be tied high.

Serial Mode 1

Serial Mode 1 is selected by tying SMS0 (Pin 18) low, SMS1 (Pin 19) high, and SEL (Pin 28) low (Figure 4B). In this mode the HI-7159A interface emulates a UART, reading and writing data in serial data packets of 1 start bit, 8 data bits, 1 parity bit (EVEN), and 1 stop bit. The baud rate is determined by the state of BRS0 and BRS1 (Pins 24 and 25) as shown in Table 2. Pin 15 becomes the serial receiver pin (RXD) and pin 16 the serial transmitter pin (TXD). $\overline{CS}$ (Pin 17) remains a chip select and must either be tied to D_{GND} or pulled low (see Figure 2B) to access the device. SAD0-SAD3 (Pins 20-23) are unused in this mode and should be tied high.

TABLE 2. BAUD RATE SELECTION FOR MODES 1 AND 2

BRS0 PIN 24	BRS1 PIN 25	BAUD RATE (f_{XTAL} = 2.4576MHz)	BAUD RATE vs f_{XTAL}
D_{GND}	D_{GND}	300	$f_{XTAL}/8192$
D_{GND}	V_{CC}	1200	$f_{XTAL}/2048$
V_{CC}	D_{GND}	9600	$f_{XTAL}/256$
V_{CC}	V_{CC}	19200	$f_{XTAL}/128$

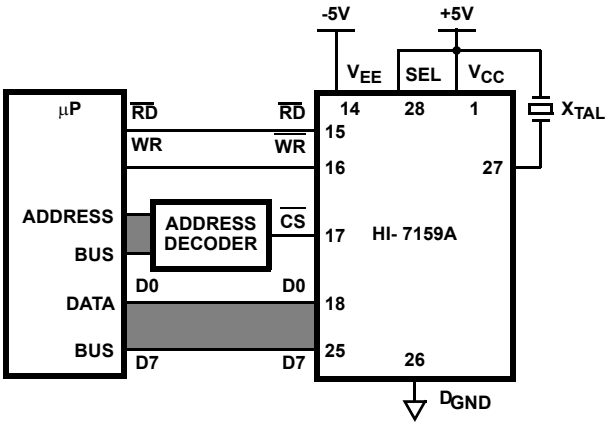


FIGURE 3. PARALLEL MODE CONFIGURATION

Design Hints for Operating in the Parallel Mode

1. Always read the status byte twice to make sure that it is cleared.
2. Make sure the status byte is cleared before issuing a command to change modes.
3. Read each digit pair five times before reading the next byte to ensure that the output data is correct.
4. Use a watchdog timer to monitor conversion time. If conversion time is either too long or too short, reissue the conversion command.

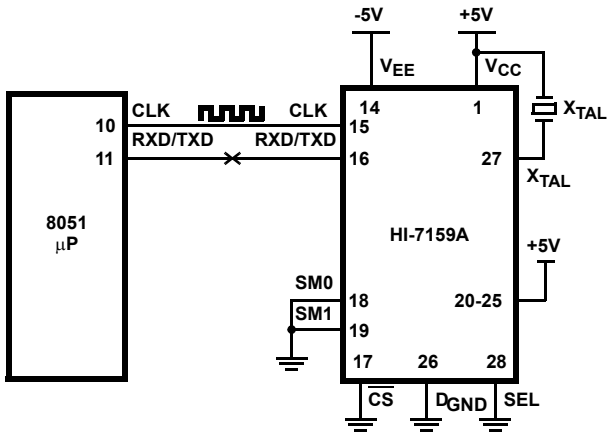


FIGURE 4A. SERIAL MODE 0

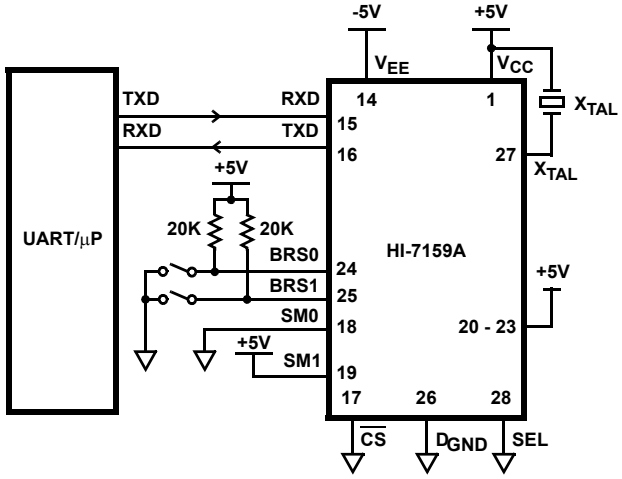


FIGURE 4B. SERIAL MODE 1

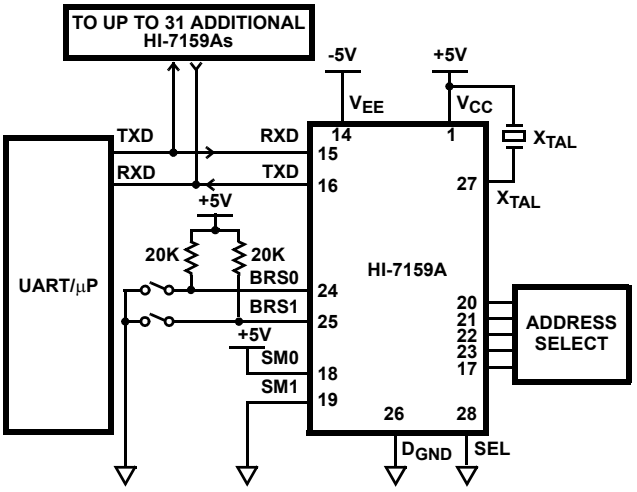


FIGURE 4C. SERIAL MODE 2

FIGURE 4. SERIAL MODE CONFIGURATIONS

Serial Mode 2

Serial Mode 2 is selected by tying SEL (pin 28) low, SMS0 (pin 18) high, and SMS1 (pin 19) low, as shown in Figure 4C. This mode of operation is identical to Serial Mode 1, except that each device now has one of 32 unique addresses determined by the state of pins 20-23 and 17, as shown in Table 3. This allows multiple HI-7159As to be attached to the same pair of serial lines.

When the microprocessor sends out an Address Byte (Table 4) that matches one of the HI-7159As' hardwired addresses, that particular HI-7159A is selected for all further I/O until another Address Byte with a different address is transmitted.

TABLE 3. HARDWARE ADDRESS SELECTION FOR MODE 2

PIN 17	PIN 23	PIN 22	PIN 21	PIN 20
B4 (MSB)	B3	B2	B1	B0 (LSB)

Reading the HI-7159A

Despite the wide variety of interface options available on the HI-7159A, the procedure for communicating with it is essentially the same in all four modes. (Serial Mode 2 differs from the rest in two respects: the chip to be communicated with must first be sent an address byte to select it, and the digit bytes are sent one by one, for a total of six bytes, instead of in pairs.) There are two types of bytes that can be sent to the converter, commands and requests. A command byte (Table 5) sets the parameters of and initiates a conversion. Those parameters are: continuity of the conversion (single or continuous), resolution ($5^1/_2$ or $4^1/_2$ digits), and type of conversion (Compensated, Uncompensated, or Error Only). Bit D0 = 0 indicates that this is a command byte and a new conversion(s) should be started.

A request byte (Table 6) asks for either the status of the converter or the result of a conversion. All bits of a request should be set to 0 except D3, D2, and D0. D3 and D2 determine the type of request (status or digit pair), and D0 = 1 indicates to the HI-7159A that this is a request byte. Serial Mode 2 uses a slightly modified request byte, shown in Table 7, allowing it to individually select each of the six digit bytes.

Upon receipt of a request, the HI-7159A will respond with either a status or a digit byte. The status byte (Table 8) returns the current state of the converter. Bit D6 = 1 indicates that a new conversion has been completed since the last time the status byte was read. Bit D6 is cleared after it is read. Bit D4 shows the current continuity (single or continuous). Bit D3 indicates the resolution ($5^1/_2$ or $4^1/_2$ digits) of the conversion, and bits D2 and D1 indicate the type (Compensated, Uncompensated, or Error Only). Bit D0 = 0 indicates that there was no parity error detected in the last request byte.

The three digit bytes (Table 9) each contain two nibbles representing two digits of the conversion. The sixth nibble contains the MSD (most significant digit), polarity (1 = positive) and overrange (1 = overrange) information. In Serial Mode 2 the digits (Table 10) are requested and received individually, so a total of six requests and six reads is necessary to obtain all $5^1/_2$ digits.

TABLE 4. SERIAL MODE 2 ADDRESS BYTE FORMAT (SENT TO HI-7159A)

ADDRESS BIT	(RESERVED)		(MSB)				(LSB)
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	B4	B3	B2	B1	B0

TABLE 5. COMMAND BYTE FORMAT (SENT TO HI-7159A)

(RESERVED)			CONTINUITY		RESOLUTION		CONVERSION TYPE			COMMAND BIT
D7	D6	D5		D4		D3		D2	D1	D0
0	0	0	Single	0	$5^1/_2$	1	Comp	1	1	0
			Continuous	1	$4^1/_2$	0	Uncomp	1	0	
							Error Only	0	1	

TABLE 6. REQUEST BYTE FORMAT, PARALLEL AND SERIAL MODE 1 (SENT TO HI-7159A)

(RESERVED)				BYTE REQUEST			(RESERVED)	REQUEST BIT
D7	D6	D5	D4		D3	D2	D1	D0
0	0	0	0	Digit Pair 0, 1	0	0	0	1
				Digit Pair 2, 3	0	1		
				Digit Pair 4, 5	1	0		
				Converter Status	1	1		

TABLE 7. REQUEST BYTE FORMAT, SERIAL MODE 2 (SENT TO HI-7159A)

(RESERVED)				BYTE REQUEST				REQUEST BIT
D7	D6	D5	D4		D3	D2	D1	D0
0	0	0	0	Digit 0	0	0	0	1
				Digit 1	0	0	1	
				Digit 2	0	1	0	
				Digit 3	0	1	1	
				Digit 4	1	0	0	
				Digit 5	1	0	1	
				Converter Status	1	1	0	

TABLE 8. STATUS BYTE FORMAT (RECEIVED FROM HI-7159A)

(†)	CONVERTER UPDATE STATUS		(†)	CONTINUITY		RESOLUTION		CONVERSION TYPE			PARITY ERROR	
D7		D6	D5		D4		D3		D2	D1		D0
0	No Update	0	0	Single	0	$5^1/_2$	1	Comp	1	1	No	0
	Updated	1		Continuous	1	$4^1/_2$	0	Uncomp	1	0	Yes	1
								Error	0	1		

(† = Reserved)

TABLE 9. DIGIT BYTE FORMAT, PARALLEL AND SERIAL MODE 1 (RECEIVED FROM HI-7159A)

DIGIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
Digit Pair 0, 1	MSB1			LSB1	MSB0			LSB0
Digit Pair 2, 3	MSB3			LSB3	MSB2			LSB2
Digit Pair 4, 5	Polarity (1 = POS)	Overrange (1 = OR)	MSB5	LSB5	MSB4			LSB4

TABLE 10. DIGIT BYTE FORMAT, SERIAL MODE 2 (RECEIVED FROM HI-7159A)

DIGIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
Digits 0 - 4	0	0	1	1	MSB		LSB	
Digit 5	0	0	1	1	Polarity (1 = POS)	Overrange (1 = OR)	MSB	LSB

Single Conversion Mode

The suggested algorithm for reading the HI-7159A in its single conversion mode of operation is shown in Figure 5. Essentially it consists of initiating a conversion, waiting until the conversion is complete, and then reading the results. Since no further conversions take place, the data may be read out at any time and at any speed. This is the most straightforward method of reading the HI-7159A.

Continuous Conversion Mode

Once a command byte is sent to the HI-7159A initiating the continuous conversion mode, the output data registers will be updated continuously after every conversion. This makes obtaining a valid reading more difficult, since the possibility exists that the current data could be overwritten by a new conversion before all the digit bytes are read. To prevent this, the status byte should be read before and after the data is read from the converter, to ensure that the converter has not updated during the reads. This is demonstrated in Figure 6.

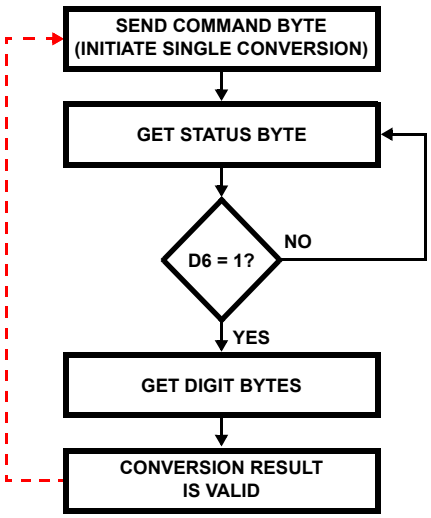


FIGURE 5. READING THE HI-7159A IN THE SINGLE CONVERSION MODE

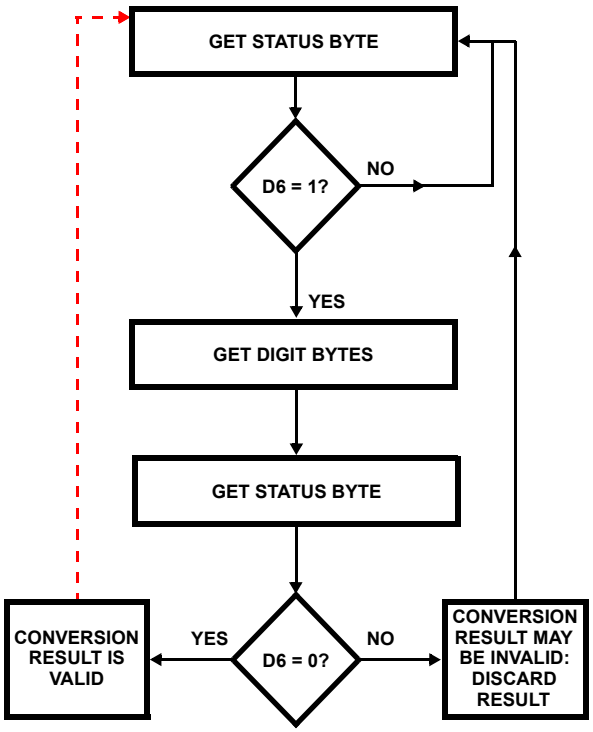


FIGURE 6. READING THE HI-7159A IN THE CONTINUOUS CONVERSION MODE

Due to the wide range of baud rates available in the serial modes, some of the lower baud rates will take longer to transfer the output data than it takes to perform a conversion. In these cases the continuous mode should not be used. Table 11 shows the percentage of the total conversion time that it takes to read all the data from the converter for the two serial modes. These are best case numbers, assuming that the bytes are transmitted and received end-to-end. An asterisk indicates that it is impossible to get all the data out within one conversion. Percentages in the 20-50% range indicate that it is possible to get valid data out with very tight code. In all cases the status byte should be checked before and after the reading to ensure data integrity.

TABLE 11. SERIAL MODES $^1/_2$

BAUD RATE	CONVERSION TYPE			
	$5^1/_2$ COMP	$5^1/_2$ UNCOMP	$4^1/_2$ COMP	$4^1/_2$ UNCOMP
300	*/*	*/*	*/*	*/*
1200	54%/*	*/*	*/*	*/*
9600	7%/13%	14%/25%	27%/50%	54%/*
19200	4%/7%	7%/13%	14%/25%	27%/50%

Crystal Oscillator

The HI-7159A uses a single pin crystal oscillator design (Figure 7). The crystal is connected between Pin 27 and V_{CC}; no load capacitors or other components are necessary. The user has a choice of crystal frequencies: 2.4576MHz or 2.4MHz. An off-the-shelf 2.4576MHz crystal works well and provides baud rates of exactly 19.2K, 9600, 1200, and 300. However its total integration period will be 16.28ms, or 0.39ms shorter than a 60Hz cycle. This effectively reduces the normal mode AC rejection.

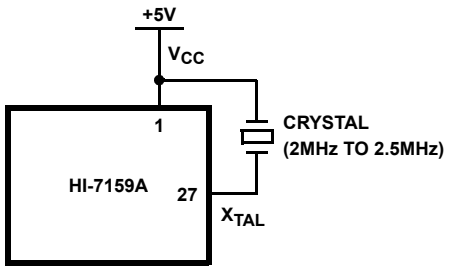


FIGURE 7. SINGLE-PIN OSCILLATOR

A 2.4MHz crystal results in an integration period of 16.67ms, exactly the length of one 60Hz AC cycle. Normal mode AC rejection is greatest at this frequency. At 2.4MHz, however, the Baud rates will be off by -2.34%. This error is not large enough to cause any errors with most peripherals, and only applies to operation in Serial Modes 1 and 2. Communication in Serial Mode 0 and the Parallel Mode is independent of the crystal frequency. For this mode a 2.4MHz crystal is recommended.

While the oscillator was designed to operate at 2MHz - 2.5MHz, the HI-7159A itself will operate reliably down to less than 600kHz when driven with an external clock. Benefits at lower clock frequencies include reduced rollover error (gain error for negative input voltages) and lower noise. The baud rates mentioned throughout this data sheet correspond to a crystal frequency of 2.4576MHz. At 1.2MHz, the actual baud rates will be half the speed they were at 2.4MHz, i.e., 9600, 4800, 600 and 150 baud. At 600kHz they will be one-fourth.

It may also be possible to directly program the host's serial hardware for operation at nonstandard baud rates, allowing HI-7159A operation at any arbitrary frequency. For example: 50Hz AC rejection requires a 2MHz clock. At this frequency the "9600" baud rate becomes 7812.5 baud. The host's UART must be programmed with the proper divider to operate at this baud rate. The data clock (see Figure 2) is defined as 16 times the baud rate, so the data clock of this configuration would be 125kHz. The data clock can also be determined by dividing the oscillator (clock) frequency by the correct divider from Table 12.

TABLE 12. CRYSTAL DIVIDER RATIOS

BAUD RATE SELECTED	CRYSTAL DIVIDER
"300"	512
"1200"	128
"9600"	16
"19200"	8

The following equation determines the divider needed to operate the HI-7159A at any given crystal frequency:

$$\frac{f_{CLOCK}(7159A)}{Divider(7159A)} = \frac{f_{CRYSTAL}(Host\ UART)}{Divider(Host\ UART)} = Data\ Clock$$

Once determined, the new divider must be written directly to the Host's UART. Most PC compatibles use an 8250 UART with a 1.8432MHz crystal, so the proper divider for the 2MHz example given above would be 15. Again, these considerations apply only to Serial Modes 1 and 2. Parallel and Serial Mode 0 communication rates are independent of crystal frequency.

Conversion Time

The conversion time of the HI-7159A is a function of the crystal frequency and the type of conversion being made. The conversion times for f_{CLOCK} = 2.4MHz are shown in Table 13. At other clock frequencies the times may be calculated from the following formula:

$$t_{CONV} = \frac{C}{f_{CLOCK}}$$

where the constant C is determined from Table 13.

TABLE 13. CONVERSION TIMES

	CONVERSION TYPE			
	$5^1/_2$ COMP	$5^1/_2$ UNCOMP	$4^1/_2$ COMP	$4^1/_2$ UNCOMP
f = 2.4MHz	133ms	66.7ms	33.3ms	16.7ms
C	320,000	160,000	80,000	40,000

Component Selection

Three external passive components must be chosen for the HI-7159A: the integrating capacitor (C_{INT}), the integrating resistor (R_{INT}), and the reference capacitor (C_{REF}). They are chosen based on the crystal frequency, the reference voltage (V_{REF}), and the desired integrating current. Figure 8 illustrates the analog components necessary for the HI-7159A to function.

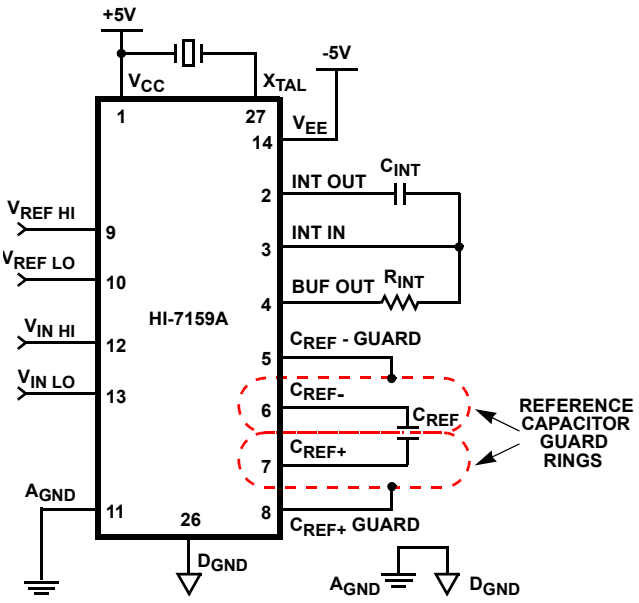


FIGURE 8. ANALOG COMPONENTS AND INPUTS

TABLE 14. RECOMMENDED COMPONENT VALUES vs CLOCK FREQUENCY

f_{CLOCK}	R_{INT}	C_{INT}	C_{REF}
2.4MHz	400kΩ	0.01µF	1.0µF
1.2MHz	360kΩ	0.022µF	2.2µF
600kHz	330kΩ	0.047µF	4.7µF

NOTE: C_{INT} MUST be a high quality polypropylene capacitor or performance may be degraded.

The reference capacitor and integrating components can either be selected from Table 14, or calculated from the following equations.

C_{REF} acts as a voltage source at different times during a conversion. Its value is determined by two considerations: it must be small enough to be fully charged from its discharged state at power-on; yet it also must be large enough to supply current to the circuit during conversion without significantly drooping from its initial value. For 2.4MHz operation, a 1µF capacitor is recommended. The equation for other frequencies is:

$$C_{REF} = \frac{2.5}{f_{CLOCK}}$$

The values of R_{INT} and C_{INT} are selected by choosing the maximum integration current and the maximum integrator output voltage swing. The maximum integration current and voltage swing occurs when V_{IN} = full scale = 2 X V_{REF}. The recommended integration current for the HI-7159A is 5mA - 10mA. This will help determine the value of R_{INT}, since:

$$I_{INT} = \frac{V_{IN}}{R_{INT}} \quad so \quad R_{INT} = \frac{V_{IN}}{I_{INT}},$$

where $V_{IN} = V_{IN\ HI} - V_{IN\ LO} = 2 \times V_{REF}$.

Therefore values of R_{INT} should be between 200kΩ and 400kΩ. The exact value of R_{INT} may be altered to get the exact integrator swing desired after choosing a standard capacitor value for C_{INT}.

The most critical component in any integrating A/D converter is the integrating capacitor, C_{INT}. For a converter of this resolution, it is imperative that this component perform as closely to an ideal capacitor as possible. Any amount of leakage or dielectric absorption will manifest itself as linearity errors. For this reason C_{INT} must be a high quality polypropylene capacitor. Use of any other type may degrade performance. The value of C_{INT} is determined by the magnitude of the desired maximum integrator output voltage swing as shown below:

$$V_{SWING} = \frac{(V_{IN})(t_{INT})}{(R_{INT})(C_{INT})}$$

Solving for C_{INT} yields:

$$C_{INT} = \frac{(V_{IN})(t_{INT})}{(R_{INT})(V_{SWING})}$$

where V_{SWING} is the maximum output voltage swing of the integrator, V_{IN} is the full scale input voltage ($V_{IN\ HI}$ - $V_{IN\ LO}$) to the converter (equal to 2 X V_{REF}), and t_{INT} is the time in which V_{IN} is integrated. The best results are achieved when the maximum integrator output voltage is made as large as possible, yet still less than the nonlinear region in the vicinity of the power supply limit. A full scale output swing of about 3V provides the greatest accuracy and linearity.

NOTE: The integrator is auto-zeroed to the voltage at $V_{IN\ LO}$. If $V_{IN\ LO}$ is negative with respect to A_{GND}, the integrator will have | $V_{IN\ LO}$ | less headroom for positive input voltages (inputs where $V_{IN\ HI}$ - $V_{IN\ LO}$ > 0). If $V_{IN\ LO}$ is positive with respect to A_{GND}, the integrator will have | $V_{IN\ LO}$ | less headroom for negative input voltages (inputs where $V_{IN\ HI}$ - $V_{IN\ LO}$ < 0). In most applications $V_{IN\ LO}$ is at or near A_{GND} and the above equations will be adequate. In applications where $V_{IN\ LO}$ may be more than 0.1V away from A_{GND}, it should be included in the integrator swing considerations. The following formula combines all the above considerations:.

$$\left| V_{IN\ LO} - \frac{(V_{IN\ HI} - V_{IN\ LO})(10,000)}{(R_{INT})(C_{INT})(f_{OSC})} \right| \leq 3V$$

Gain Error Adjustments

While the HI-7159A has a very linear transfer characteristic in both the positive and negative directions, the slope of the line is slightly greater for negative inputs than for positive. This results in the transfer characteristic shown in Figure 9. One end point of this curve, typically the positive side, can be adjusted to zero error by trimming the reference voltage. The other (negative) side will have a fixed gain error. This error can be removed in software by multiplying all negative readings by a scale factor, determined by dividing the ideal full scale reading (-200,000 counts) by the actual full scale reading when V_{IN} = -2.00000V.

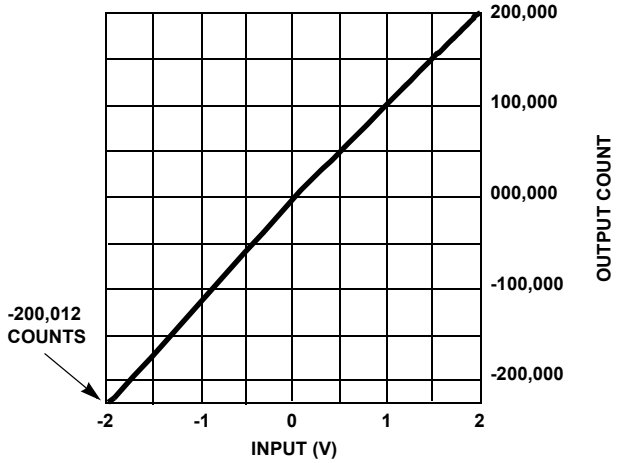


FIGURE 9. TYPICAL HI-7159A TRANSFER CHARACTERISTIC

C_{REF} Guard Pins

Depending on the polarity of the input signal, either the negative or the positive terminal of the reference capacitor will be connected to A_{GND} to provide the correct polarity for reference deintegration. In systems where $V_{REF\ LO}$ is tied to analog ground, the reference capacitor is effectively shifted down by | V_{REF} | for positive input voltages, and is not shifted at all for negative input voltages. This shift can cause some charge on the reference capacitor to be lost due to stray capacitance between the reference capacitor leads and ground traces or other fixed potentials on the board. The reference voltage will now be slightly smaller for positive inputs. This difference in reference voltages for positive and negative inputs appears as rollover error.

The HI-7159A provides two guard ring outputs to minimize this effect. Each guard ring output is a buffered version of the voltage at its respective C_{REF} pin. If the traces going to the C_{REF} pins and under C_{REF} itself are surrounded by their corresponding guard rings, no charge will be lost as C_{REF} is moved. Figure 10 shows two slightly different patterns. The first one is for capacitors of symmetrical construction, the second is for capacitors with outside foils (one end of the capacitor is the entire outside.

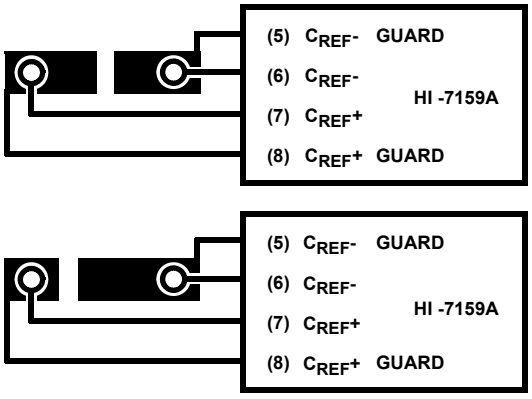


FIGURE 10. TYPICAL GUARD RING LAYOUT

Die Characteristics

DIE DIMENSIONS:

5817µm x 3988µm

METALLIZATION:

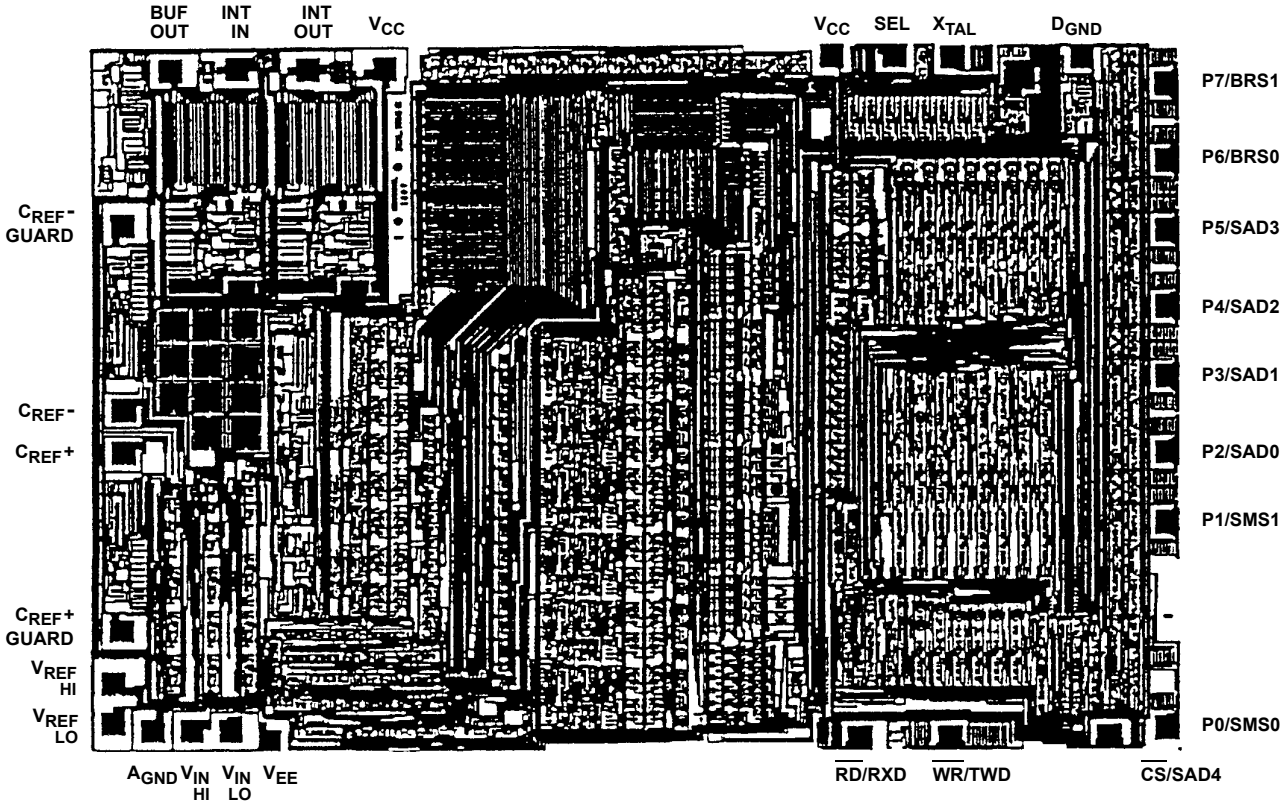
Type: SiAl
Thickness: 10kÅ ±1kÅ

PASSIVATION:

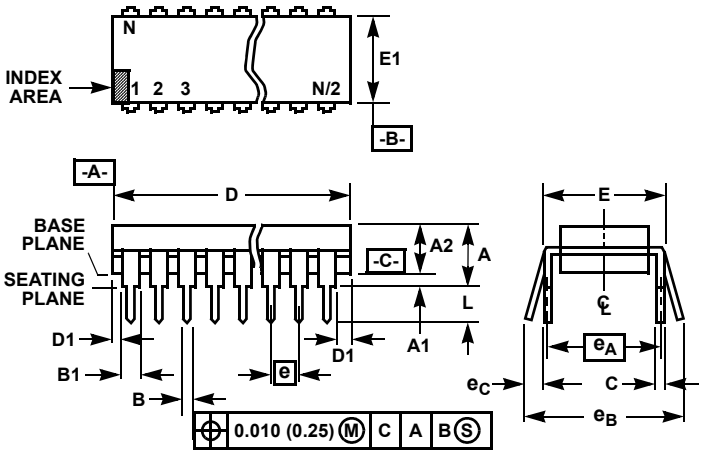
Type: PSG/Nitride
Thickness: 15kÅ ±1kÅ

Metallization Mask Layout

HI-7159A



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-001-BF ISSUE D)
28 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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