HOLT INTEGRATED CIRCUITS INC.

HI-8482

August 2006

ARINC 429 DUAL LINE RECEIVER

GENERAL DESCRIPTION

The HI-8482 bus interface unit is a silicon gate CMOS device designed as a dual differential line receiver in accordance with the requirements of the ARINC 429 bus specification. The device translates incoming ARINC 429 signals to normal CMOS/TTL levels on each of its two independent receive channels. The HI-8482 is also functionally equivalent to the Fairchild/Raytheon RM3183.

The self-test inputs force the outputs to either a ZERO, ONE, or NULL state for system tests. While in self-test mode, the ARINC inputs are ignored.

All the ARINC inputs have built-in hysteresis to reject noise that may be present on the ARINC bus. Additional input noise filtering can also be accomplished with external capacitors.

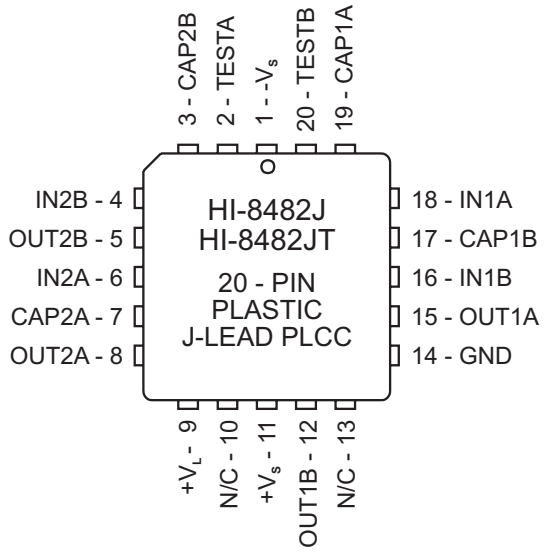
The HI-8482 line receiver is one of several options offered by Holt Integrated Circuits to interface to the ARINC bus. The digital data processing for serial-to-parallel conversion and clock recovery can be accomplished with the HI-6010, HI-8683 or similar devices.

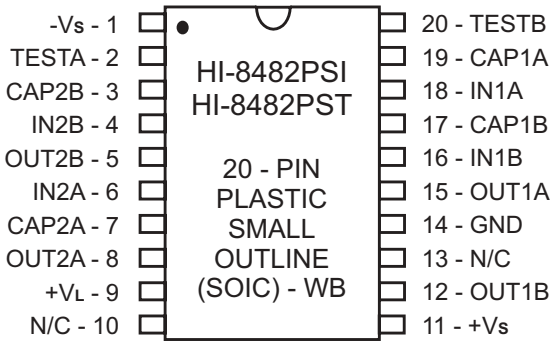
The HI-8482 is available in a variety of ceramic & plastic packages including Small Outline (SOIC), J-Lead PLCC, Cerquad, DIP & Leadless Chip Carrier (LCC).

FEATURES

- Converts ARINC 429 levels to digital data
- Direct replacement for the RM3183
- Greater than 2 volt receiving hysteresis
- TTL and CMOS outputs and test inputs
- Military screening available
- 20-Pin SOIC, PLCC, CERQUAD, DIP & LCC packages are available

PIN CONFIGURATIONS (Top Views)





(See page 6 for additional Package Pin Configurations)

TRUTH TABLE

ARINC INPUTS	TEST INPUTS		OUTPUTS	
V (A) - V (B)	TEST A	TEST B	OUT A	OUT B
Null	0	0	0	0
Zero	0	0	0	1
One	0	0	1	0
Don't Care	0	1	0	1
Don't Care	1	0	1	0
Don't Care	1	1	0	0

FUNCTIONAL DESCRIPTION

The HI-8482 contains two independent ARINC 429 receive channels. The diagram in Figure 1 illustrates a typical HI-8482 receive channel.

The differential ARINC signal input is converted to a positive signal referenced to ground through level shifters and a unity gain differential amplifier.

A positive differential input signal is converted to a positive signal on the plus output of the differential amplifier. This output is proportional in amplitude to the original input signal. At the same time, the corresponding MINUS output is pulled to GND. Likewise when a negative input signal is present at the ARINC inputs, a positive signal is present on the MINUS output and the PLUS output is pulled to GND.

The outputs of the differential amplifier are compared with the ONE, ZERO and NULL threshold levels to produce the appropriate logic level on the OUTA and OUTB outputs of the device. The ARINC clock signal may be recovered through a NOR function of OUTA and OUTB.

The test inputs logically disconnect the outputs of the comparators from OUTA and OUTB and force the device outputs to one of the three valid states (Figure 5). This alleviates having to ground the ARINC inputs during test mode operation.

ARINC LEVELS

The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5V to +13V
NULL	+2.5V to -2.5V
ZERO	-6.5V to -13V

The HI-8482 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±5V for the worst case condition.

NOISE

The input hysteresis is set to reject voltage level transitions in the undefined region between the maximum ZERO level and the minimum NULL level and the undefined region between the maximum NULL level and the minimum ONE level. Therefore, once a valid input differential voltage threshold is detected, the outputs will remain at a valid logic state until a new valid input voltage is detected.

In addition to the hysteresis, the CAPA and CAPB pins make it possible to add simple RC filters to the ARINC inputs.

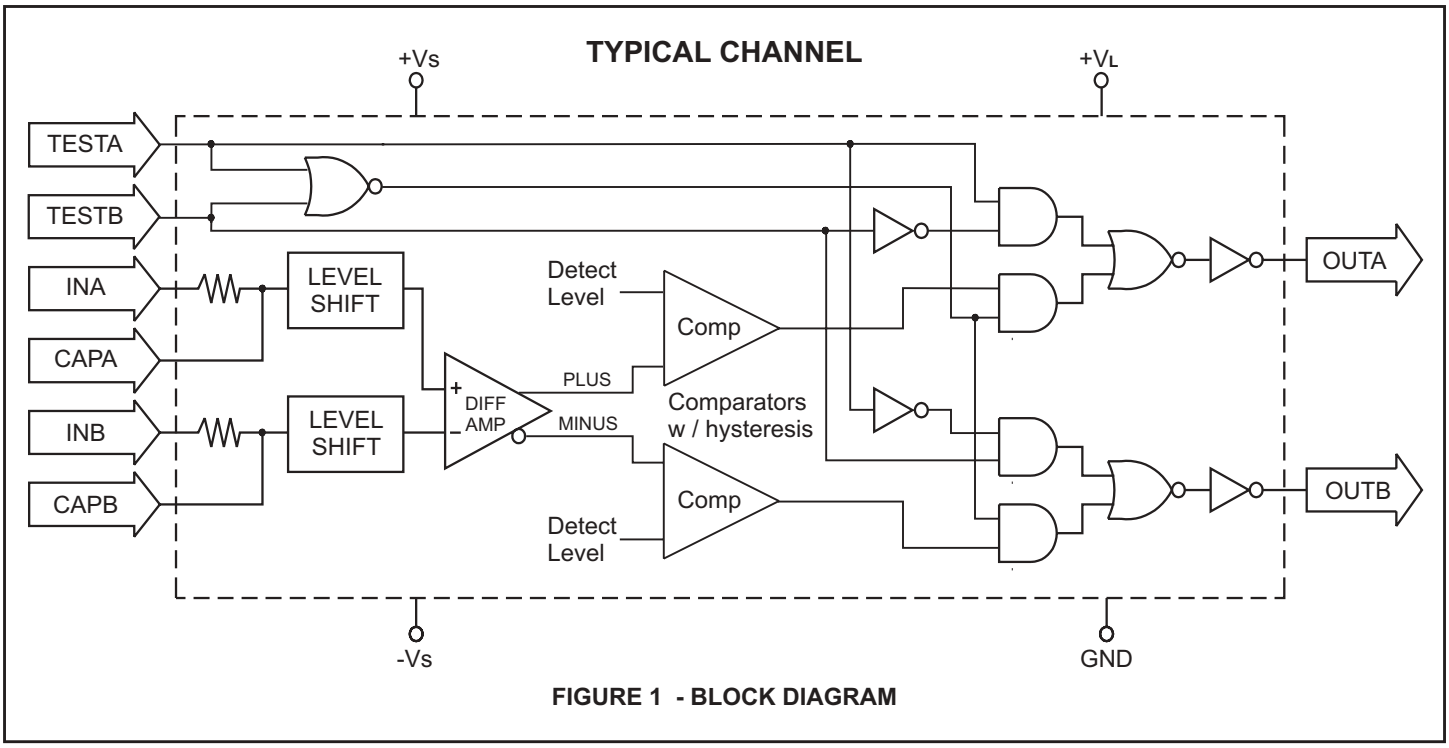


FIGURE 1 - BLOCK DIAGRAM

TYPICAL APPLICATIONS

APPLICATIONS

The standard connections for the HI-8482 are shown in Figure 2. Decoupling of the supply should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground (GND) connection should be sturdy and isolated from large switching currents to provide a quiet ground reference.

The HI-8482 can be used with HI-3182 or HI-8585 Line Drivers to provide a complete analog ARINC 429 interface solution. A simple application, which can be used in systems requiring a repeater type circuit for long transmissions or for test interfaces, is given in Figure 3. More HI-3182 or HI-8585 drivers may be added to test multiple ARINC channels, as shown.

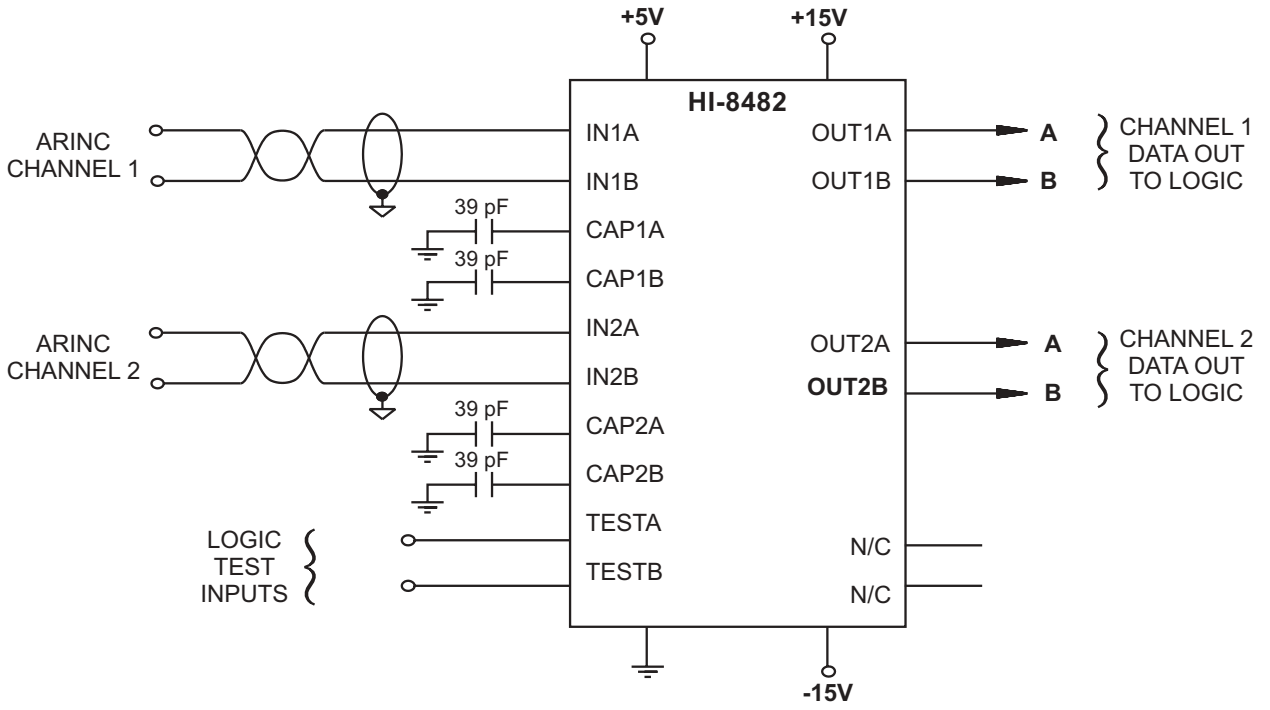


FIGURE 2 - ARINC RECEIVER STANDARD CONNECTIONS

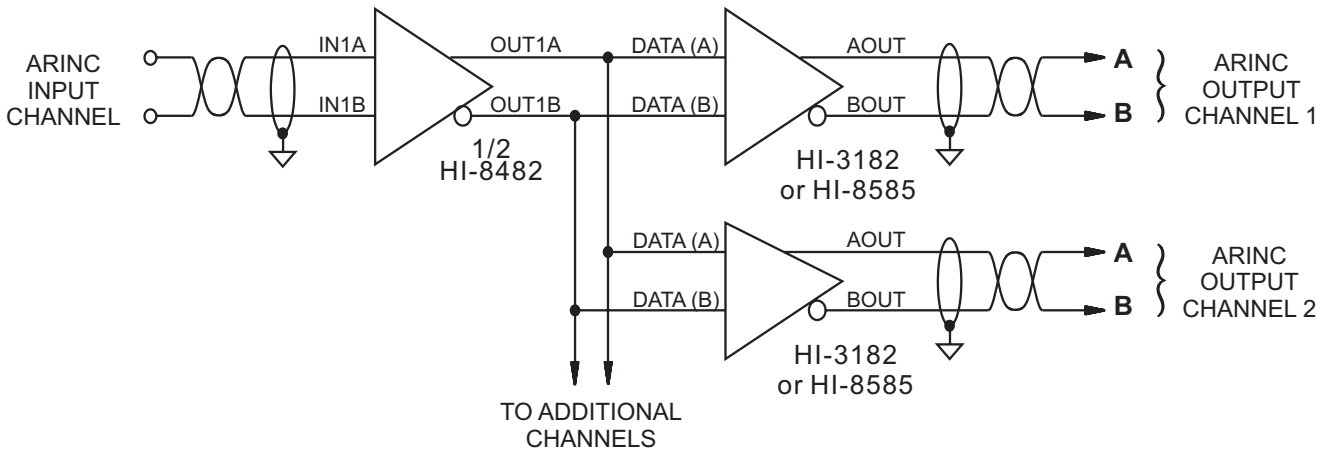


FIGURE 3 - ARINC REPEATER CIRCUIT

PIN DESCRIPTION TABLE

SYMBOL	FUNCTION	DESCRIPTION
CAP1A	INPUT	Filter capacitor input for terminal A of channel 1
CAP1B	INPUT	Filter capacitor input for terminal B of channel 1
CAP2A	INPUT	Filter capacitor input for terminal A of channel 2
CAP2B	INPUT	Filter capacitor input for terminal B of channel 2
GND	POWER	0 Volts
IN1A	INPUT	ARINC input terminal A of channel 1
IN1B	INPUT	ARINC input terminal B of channel 1
IN2A	INPUT	ARINC input terminal A of channel 2

SYMBOL	FUNCTION	DESCRIPTION
IN2B	INPUT	ARINC input terminal B of channel 2
OUT1A	OUTPUT	TTL output terminal A of channel 1
OUT1B	OUTPUT	TTL output terminal B of channel 1
OUT2A	OUTPUT	TTL output terminal A of channel 2
OUT2B	OUTPUT	TTL output terminal B of channel 2
TESTA	INPUT	Test input terminal A
TESTB	INPUT	Test input terminal B
$+V_L$	POWER	+5 Volts ±10%
+Vs	POWER	+12 Volts ±10% or +15 Volts ±10%
-Vs	POWER	-12 Volts ±10% or -15 Volts ±10%

TIMING DIAGRAMS

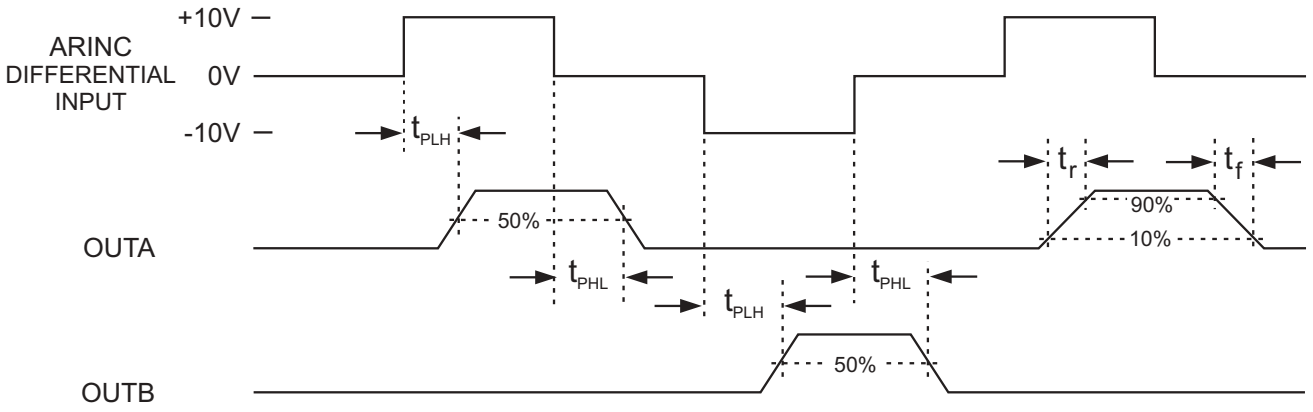


FIGURE 4

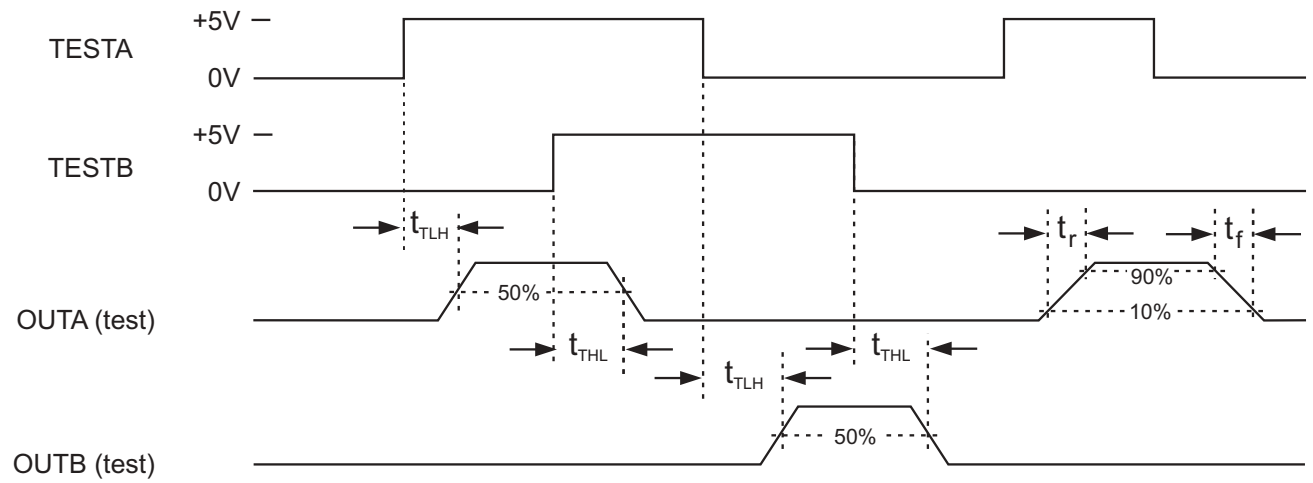


FIGURE 5

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to Gnd = 0V)

Supply Voltage, +Vs: .....+20 VDC -Vs: .....-20 VDC +VL: .....+7 VDC	Voltage at ARINC Inputs: .....-29V to +29V
Operating Temperature Range: (Industrial) .....-40°C to +85°C (Hi-Temp) .....-55°C to +125°C (Military) .....-55°C to +125°C	Voltage at Any Other Input: .....-0.3V to VL + 0.3V
	Output Short Circuit Protected: .....Not Protected
	Storage Temperature Range: .....-65°C to +150°C
Internal Power Dissipation: 900mW	Soldering Temperature: (Ceramic).....30 sec. at +300°C (Plastic - leads).....10 sec. at +280°C (Plastic - body) .....+220°C Max.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

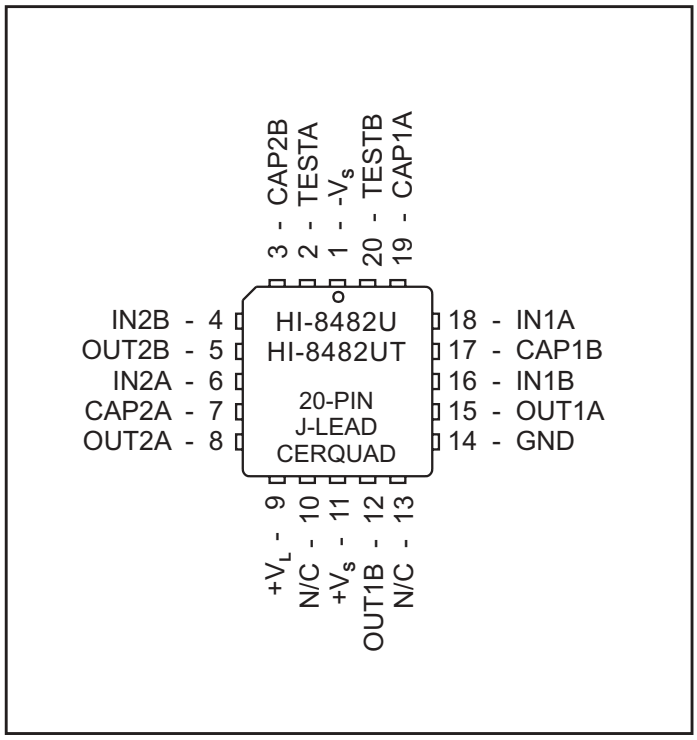
$\pm 12 \leq V_s \leq \pm 15$, $V_L = +5V$, Operating temperature range (unless otherwise noted)

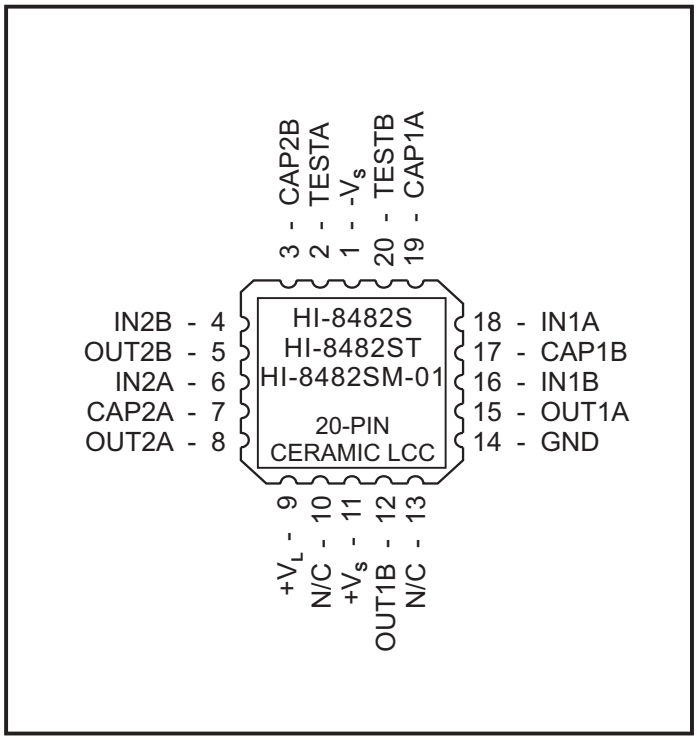
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ARINC inputs - IN1A, IN1B, IN2A, IN2B						
V(A) - V(B)	VIH	OUTA = 1	6.5	10	13	volts
V(A) - V(B)	VIL	OUTB = 1	-6.5	-10	-13	volts
V(A) - V(B)	VNULL	OUTA = OUTB = 0	-2.5	0	2.5	volts
(|V(A)| - |V(B)|) / 2	VCM	Frequency = 80KHz		±5		volts
Input resistance - input A to input B	RI	Supply pins floating	30K	50K		ohms
Input resistance - input A or B to Gnd	RG	Supply pins floating	19K	25K		ohms
Input capacitance - input A to B	CI	Filter caps disconnected - see note 1		5	10	pF
Input capacitance - input A or B to Gnd	CG	Filter caps disconnected - see note 1		5	10	pF
Test inputs - TESTA, TESTB						
Logic 1 input voltage	VIH	ARINC inputs to Gnd, TA = 25°C	2.7			volts
Logic 0 input voltage	VIL	ARINC inputs to Gnd, TA = 25°C			0.8	volts
Logic 1 input current (magnitude)	IIH	VIH = 2.7V		5	15	µA
Logic 0 input current	IIL	VIL = 0V		0.5	1	µA
Outputs - OUT1A, OUT1B, OUT2A, OUT2B						
Voltage - sourcing 100µA	VOH	TA = 25°C	4			volts
Voltage - sourcing 2.8mA	VOH	Full temperature range	3.5			volts
Voltage - sinking 100µA	VOL	TA = 25°C			0.08	volts
Voltage - sinking 2.0mA	VOL	Full temperature range			0.8	volts
Rise time	tr	CL = 50pF, TA = 25°C		40	70	ns
Fall time	tf	CL = 50pF, TA = 25°C		30	70	ns
Propagation delay - low to high (ARINC)	tPLH	CL = 50pF, TA = 25°C and filter caps disconnected		600		ns
Propagation delay - high to low (ARINC)	tPHL	CL = 50pF, TA = 25°C and filter caps disconnected		600		ns
Propagation delay - low to high (TESTA/B)	tTLH	CL = 50pF, TA = 25°C		50		ns
Propagation delay - low to high (TESTA/B)	tTHL	CL = 50pF, TA = 25°C		50		ns
Supply current						
+VS current	IDD	±VS = ±15V, TA =25°C, TESTA and TESTB = 0V		3.7	7	mA
+VS current	IDD	±VS = ±12V, TA =25°C, TESTA and TESTB = 0V		3	6	mA
-VS current	IEE	±VS = ±15V, TA =25°C, TESTA and TESTB = 0V		8.7	15	mA
-VS current	IEE	±VS = ±12V, TA =25°C, TESTA and TESTB = 0V		7.4	14	mA
+VL current	ICC	±VS = ±15V, TA =25°C, TESTA and TESTB = 0V		9	20	mA
+VL current	ICC	±VS = ±12V, TA =25°C, TESTA and TESTB = 0V		8.6	18	mA

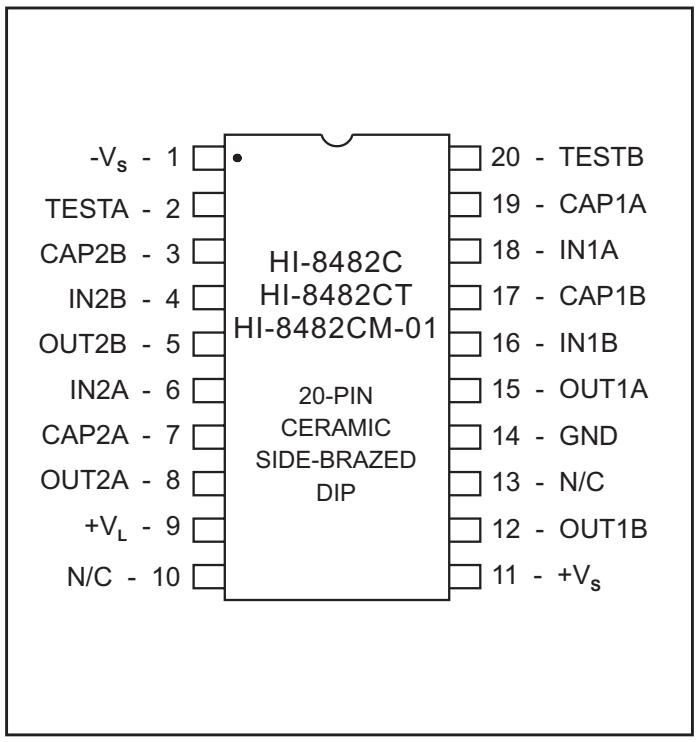
Notes: 1. Guaranteed by design.

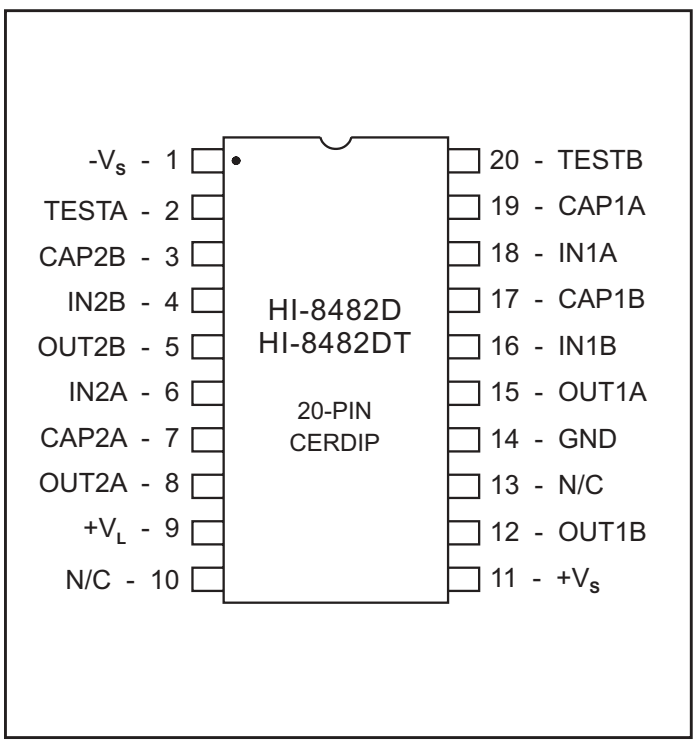
ADDITIONAL HI-8482 PIN CONFIGURATIONS

(All 20-Pin Package Configurations)









ORDERING INFORMATION & THERMAL CHARACTERISTICS

HI - 8482 x x (Ceramic DIP & LCC)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
Blank	-40°C TO +85°C	I	NO	Gold
T	-55°C TO +125°C	T	NO	Gold
M-01	-55°C TO +125°C	M	YES	Tin / Lead (Sn / Pb) Solder

PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES.	
		Θ_{JC}	Θ_{JA}
C	20 PIN CERAMIC SIDE BRAZED DIP	28°C/W	95°C/W
S	20 PIN CERAMIC LEADLESS CHIP CARRIER	25°C/W	85°C/W

HI - 8482 x x (CerDIP & CerQUAD)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
Blank	-40°C TO +85°C	I	NO	Tin / Lead (Sn / Pb) Solder
T	-55°C TO +125°C	T	NO	Tin / Lead (Sn / Pb) Solder

PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES.	
		Θ_{JC}	Θ_{JA}
D	20 PIN CERDIP	28°C/W	90°C/W
U	20 PIN J-LEAD CERQUAD	25°C/W	95°C/W

HI - 8482 xx x x (Plastic PLCC & SOIC - Wide Body)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

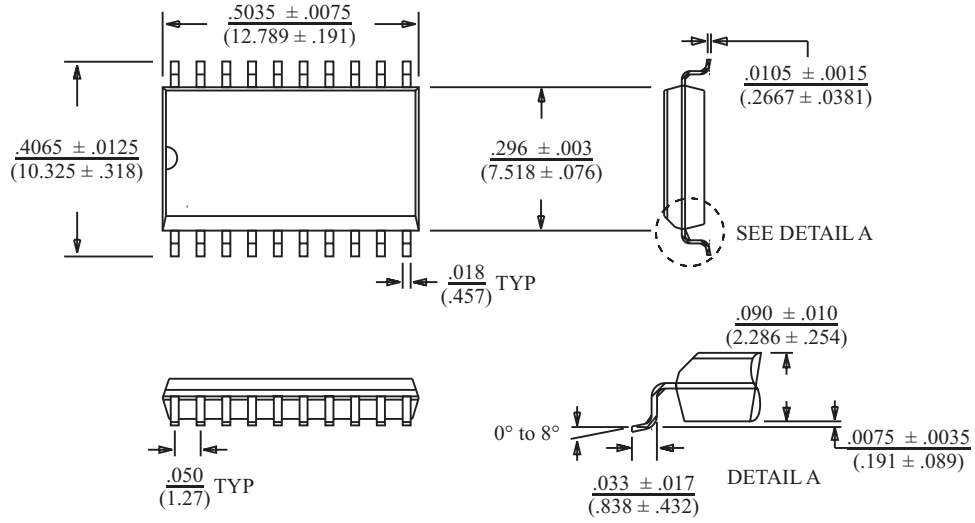
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
Blank (8482J Only)	-40°C TO +85°C	I	NO
I (8482PS Only)	-40°C TO +85°C	I	NO
T (8482J or 8482PS)	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES.	
		Θ_{JC}	Θ_{JA}
J	20 PIN PLASTIC J-LEAD PLCC	30°C/W	85°C/W
PS	20 PIN PLASTIC SMALL OUTLINE (SOIC) - WB	17°C/W	90°C/W

20-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

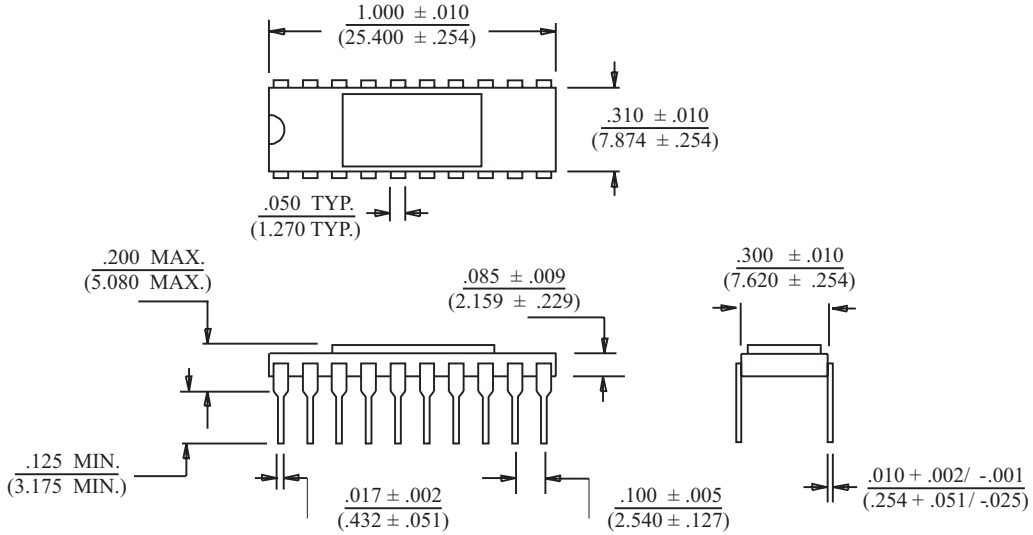
(Wide Body)

Package Type: 20HW



20-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 20C

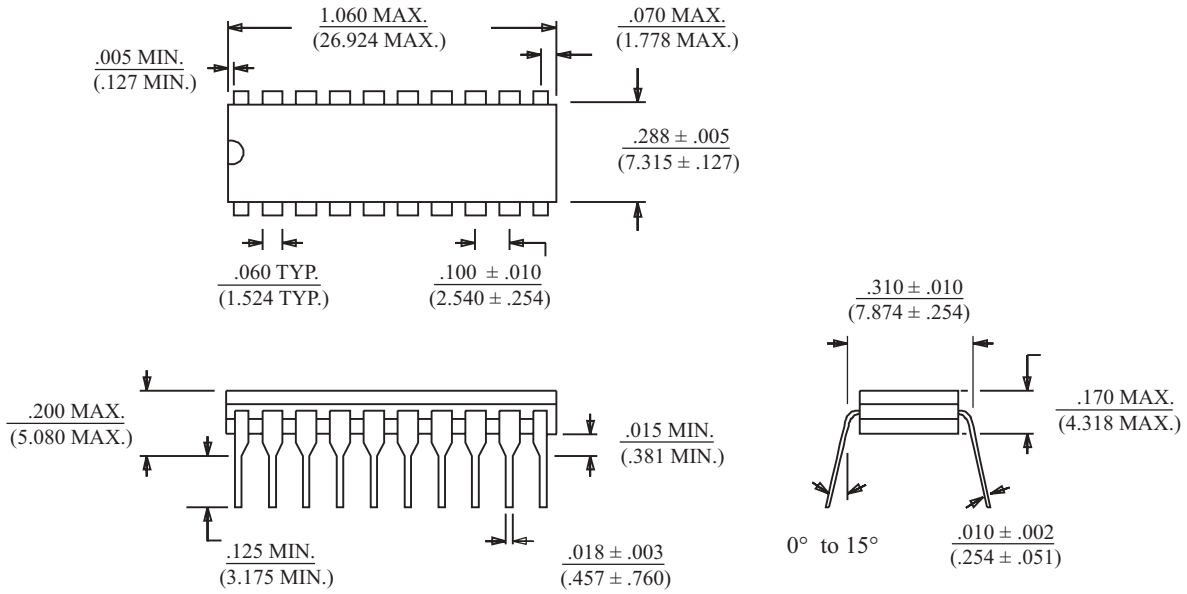


HI-8482 PACKAGE DIMENSIONS

inches (millimeters)

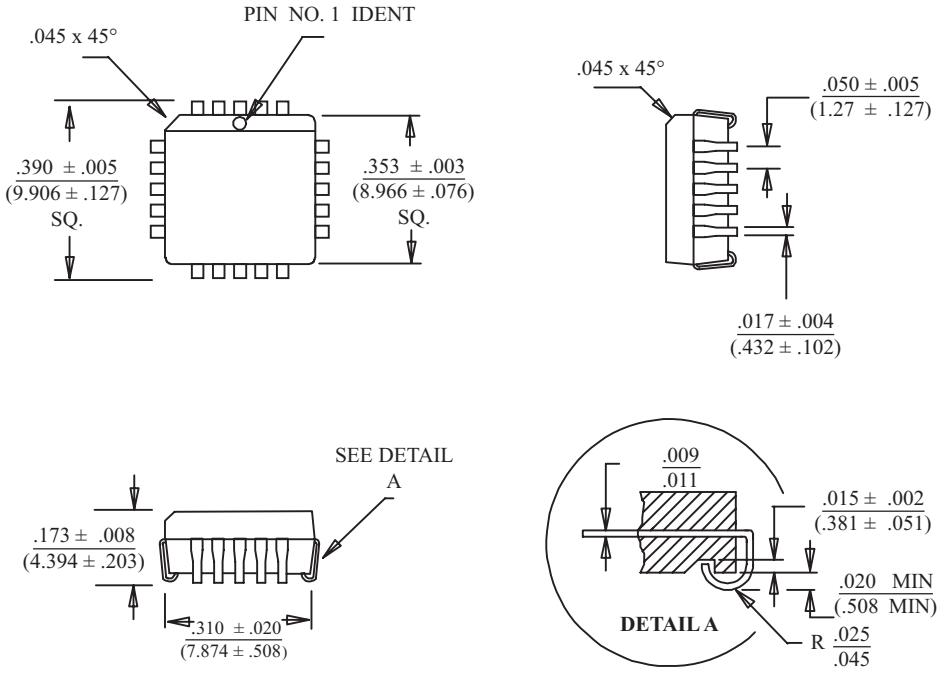
20-PIN CERDIP

Package Type: 20D



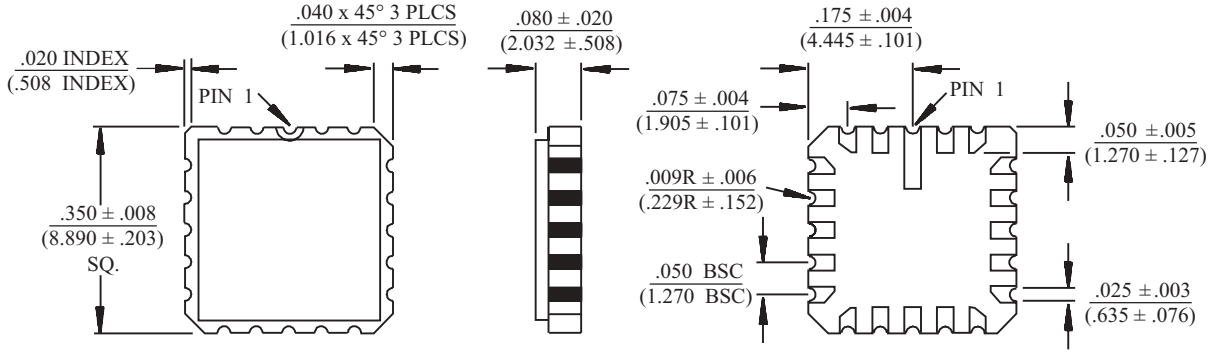
20-PIN PLASTIC PLCC

Package Type: 20J



20-PIN CERAMIC LEADLESS CHIP CARRIER

Package Type: 20S



20-PIN J-LEAD CERQUAD

Package Type: 20U