Data Sheet | September 20, 2006 | FN4071.12

14-Bit, 100MSPS, High Speed D/A Converter

The HI5741 is a 14-bit, 100MSPS, D/A converter which is implemented in the Intersil BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides 20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 14-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI5741BIB	HI5741BIB	-40 to +85	28 Ld SOIC	M28.3
HI5741BIB-T	HI5741BIB	28 Ld SOIC Tape and Reel		M28.3
HI5741BIBZ (Note)	HI5741BIBZ	-40 to +85	28 Ld SOIC (Pb-free)	M28.3
HI5741BIBZ-T (Note)	HI5741BIBZ	28 Ld SOIC Tape and Reel (Pb-free)		M28.3
HI5741-EVS		+25	Evaluation Board (SOIC)	

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

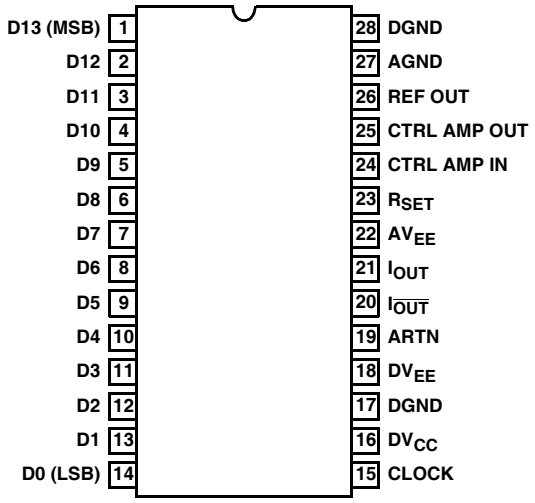
- Throughput Rate 100MSPS
- Low Power 650mW
- Integral Linearity Error . . . . . 1 LSB
- Low Glitch Energy 1pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

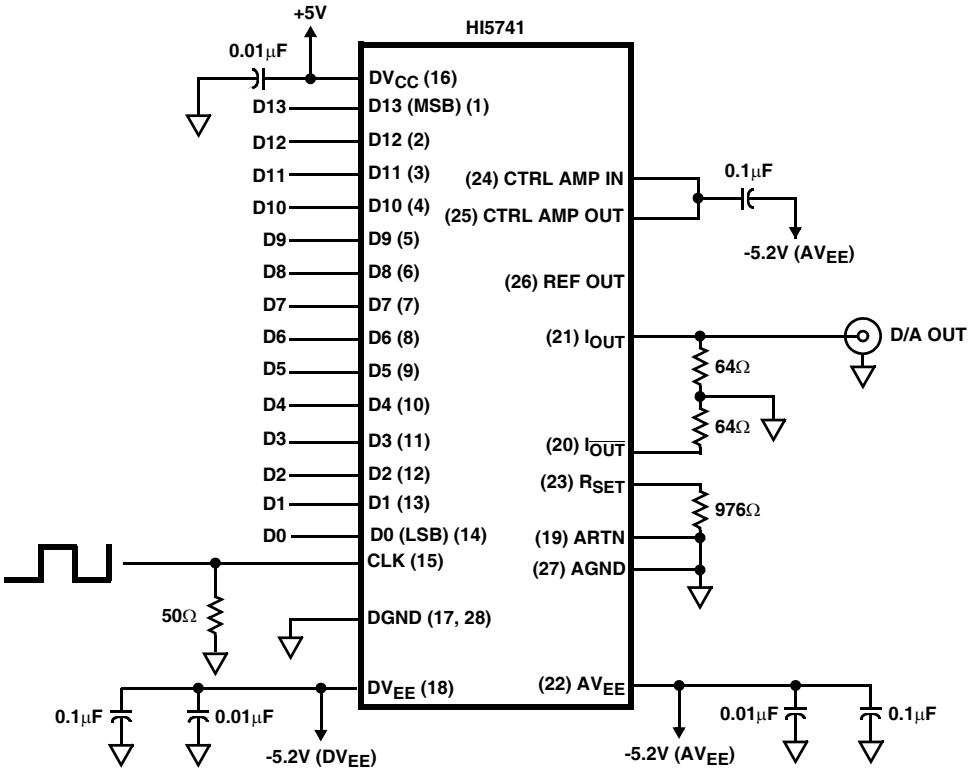
- Cellular Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Pinout

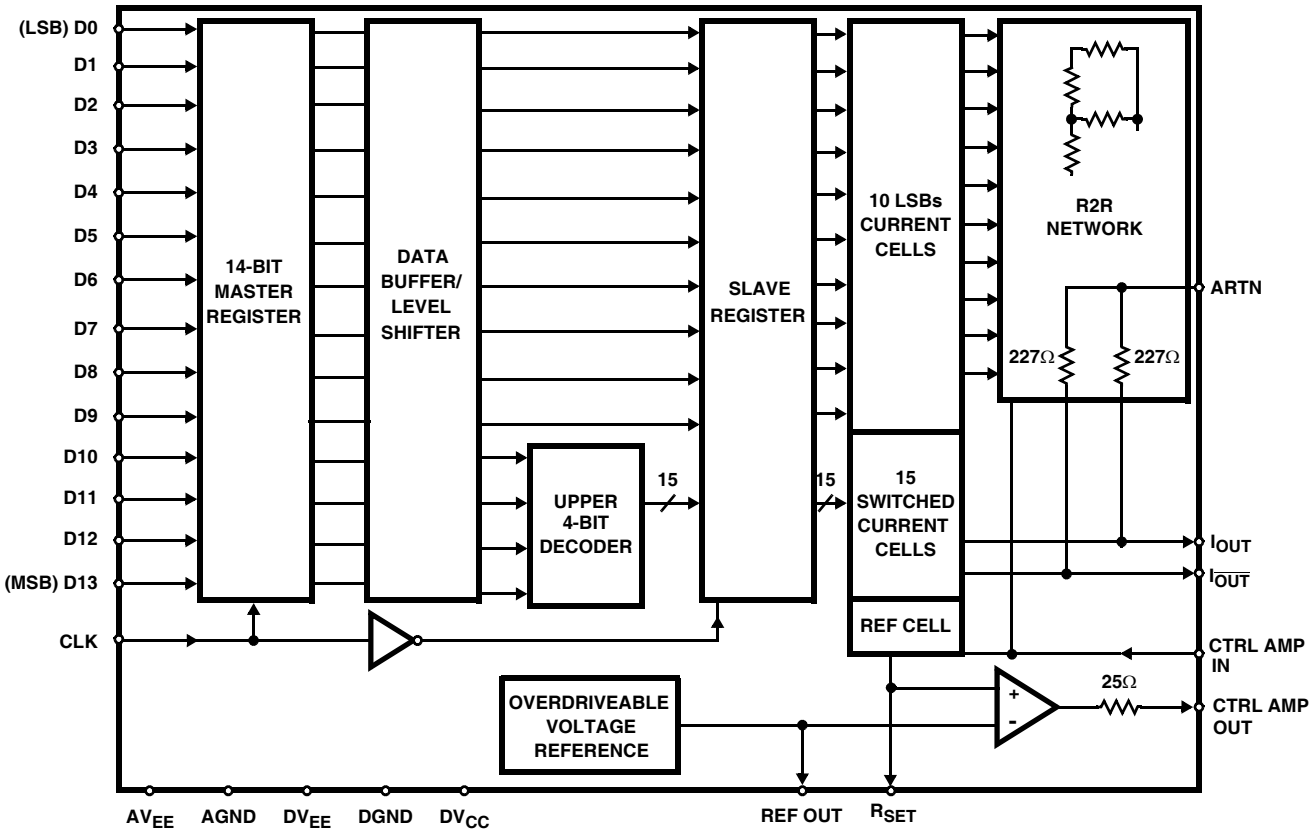
HI5741
(28 LD SOIC)
TOP VIEW



Typical Application Circuit



Functional Block Diagram



Absolute Maximum ratings T_A = +25°C

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . -5.5V
Digital Input Voltages (D13-D0, CLK) to DGND. . . . . DV_{CC} to -0.5V
Internal Reference Output Current. . . . . ±2.5mA
Voltage from CTRL AMP IN to AV_{EE}. . . . . 2.5V to 0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range. . . . . -3.7V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	70

Maximum Junction Temperature
HI5741BIx . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range. . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94V to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal, T_A = +25°C

PARAMETER	TEST CONDITIONS	HI5741BI T_A = -40°C TO +85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		14	-	-	Bits
Integral Linearity Error, INL (Note 5)	"Best Fit Straight Line", T_A = +25°C	-1.5	±1.0	1.5	LSB
	"Best Fit Straight Line", T_A = -40°C to +85°C	-1.75	-	1.75	LSB
Differential Linearity Error, DNL	(Note 5) T_A = +25°C	-1.0	±0.5	1.0	LSB
Offset Error, I_{OS}	(Note 5)	-	8	75	µA
Full Scale Gain Error, FSE	(Notes 3, 5)	-	3.2	10	%
Full Scale Gain Drift	With Internal Reference	-	±150	-	ppm FSR/°C
Offset Drift Coefficient	(Note 4)	-	-	0.05	µA/°C
Full Scale Output Current, I_{FS}		-	-20.48	-	mA
Output Voltage Compliance Range	(Note 4)	-1.25	-	0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 4)	100	-	-	MSPS
Output Voltage Settling Time ($^1/_{16}$th Scale Step Across Segment)	R_L = 64Ω (Note 4) - Settling to 0.024%	-	11	-	ns
	R_L = 64Ω (Note 4) - Settling to 0.012%	-	20	-	ns
Singlet Glitch Area, GE (Peak)	R_L = 64Ω (Note 4)	-	1	-	pV•s
Output Slew Rate	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	1,000	-	V/µs
Output Rise Time	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	675	-	ps
Output Fall Time	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	470	-	ps
Spurious Free Dynamic Range within a Window (Note 4)	f_{CLK} = 10 MSPS, f_{OUT} = 1.23MHz, 2MHz Span	-	87	-	dBc
	f_{CLK} = 20 MSPS, f_{OUT} = 5.055MHz, 2MHz Span	-	77	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 16MHz, 10MHz Span	-	75	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	80	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 5.1MHz, 2MHz Span	-	78	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	79	-	dBc

Electrical Specifications AV_{EE}, DV_{EE} = -4.94V to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal, T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS	HI5741BI T_A = -40°C TO +85°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range to Nyquist (Note 4)	f_{CLK} = 10 MSPS, f_{OUT} = 1.023MHz, 5MHz Span	-	86	-	dBc
	f_{CLK} = 10 MSPS, f_{OUT} = 2.02MHz, 5MHz Span	-	85	-	dBc
	f_{CLK} = 25 MSPS, f_{OUT} = 2.02MHz, 12.5MHz Span	-	77	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.055MHz, 25MHz Span	-	74	-	dBc
	f_{CLK} = 75 MSPS, f_{OUT} = 7.52MHz, 37.5MHz Span	-	73	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 10.1MHz, 50MHz Span	-	71	-	dBc
Multi-Tone Power Ratio (MTPR)	8 Tones, no Clipping, 110kHz Spacing, 220kHz spacing between tones 4 and 5, f_{CLK} = 20 MSPS (Note 7)	-	76	-	dBc
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Note 5)	-1.27	-1.23	-1.17	V
Internal Reference Voltage Drift	(Note 4)	-	50	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 4)	-500	-	+50	µA
Internal Reference Load Regulation	I_{REF} = 0 to I_{REF} = -500µA	-	100	-	µV
Amplifier Input Impedance	(Note 4)	-	3	-	MΩ
Amplifier Large Signal Bandwidth	4.0V_{P-P} Sine Wave Input, to Slew Rate Limited (Note 4)	-	1	-	MHz
Amplifier Small Signal Bandwidth	1.0V_{P-P} Sine Wave Input, to -3dB Loss (Note 4)	-	5	-	MHz
Reference Input Impedance (CTL IN)	(Note 4)	-	12	-	kΩ
Reference Input Multiplying Bandwidth (CTL IN)	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 4)	-	75	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 5)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 5)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 4)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1 (Note 4)	3	2.0	-	ns
Data Hold Time, t_{HLD}	See Figure 1 (Note 4)	0.5	0.25	-	ns
Propagation Delay Time, t_{PD}	See Figure 1 (Note 4)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1 (Note 4)	1.0	0.85	-	ns
POWER SUPPLY CHARACTERISTICS					
IV_{EEA}	(Note 5)	-	42	50	mA
IV_{EED}	(Note 5)	-	75	95	mA
IV_{CCD}	(Note 5)	-	13	20	mA
Power Dissipation	(Note 5)	-	650	-	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	5	-	µA/V

NOTES:

2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 1.28mA). Ideally the ratio should be 16.
4. Parameter guaranteed by design or characterization and not production tested.
5. All devices are 100% tested at +25°C.
6. Dynamic Range must be limited to a 1V swing within the compliance range.
7. In testing MTPR, tone frequencies ranged from 1.95MHz to 3.05MHz. The ratio is measured as the range from peak power to peak distortion in the region of removed tones.

Timing Diagrams

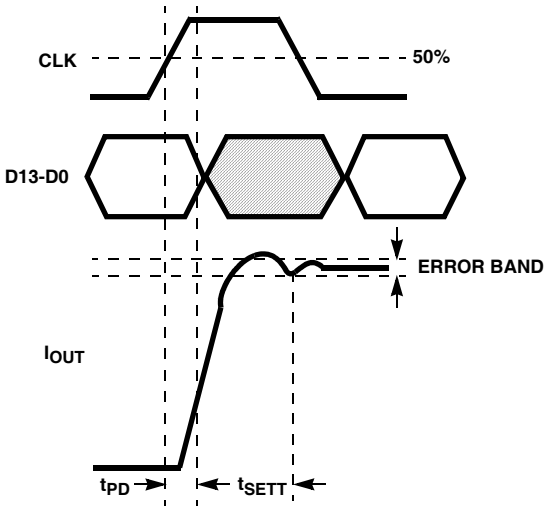


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

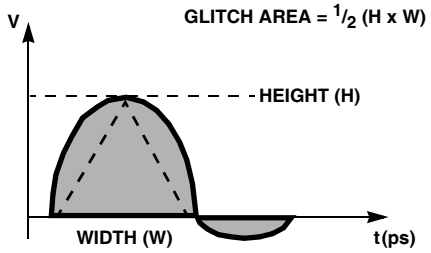


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

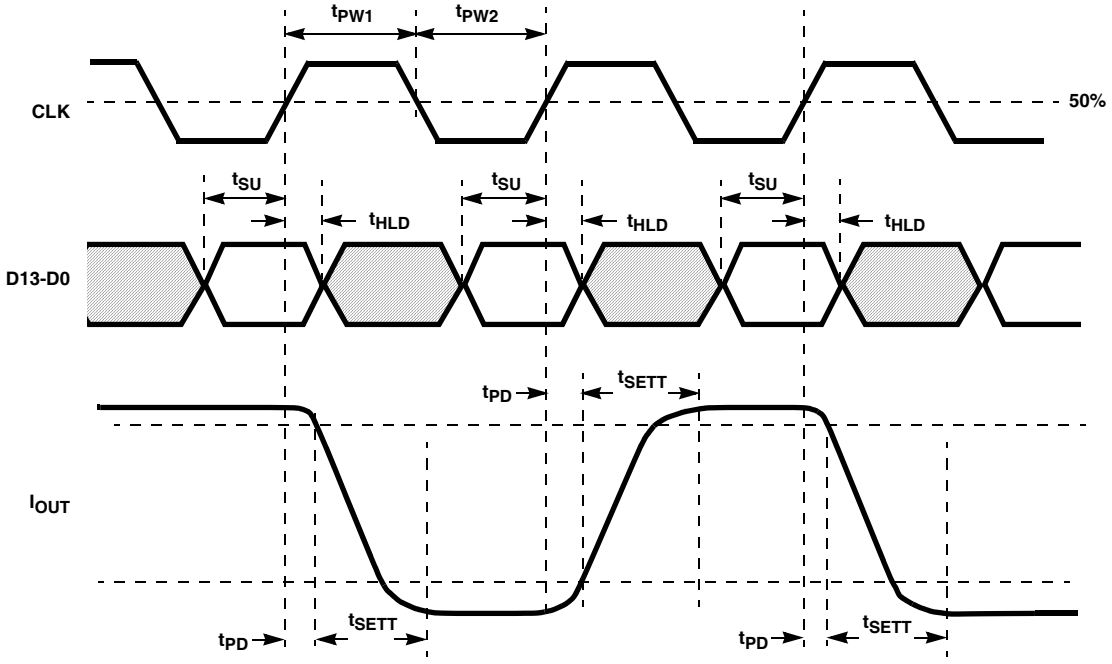


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

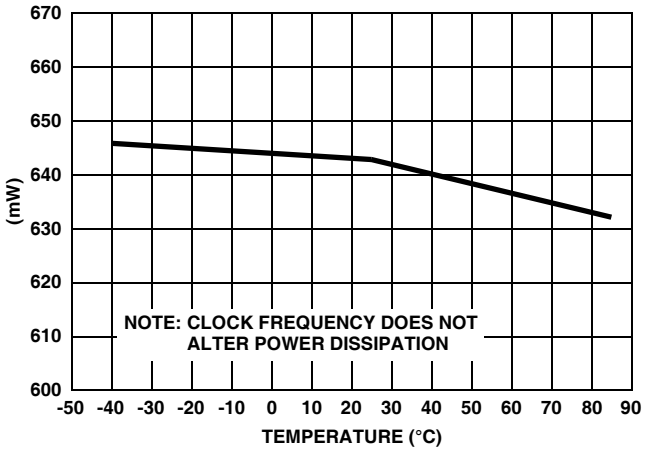


FIGURE 4. TYPICAL POWER DISSIPATION OVER TEMPERATURE

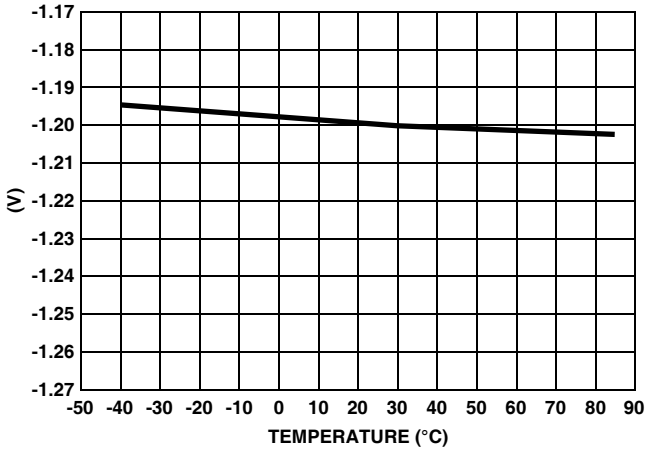


FIGURE 5. TYPICAL REFERENCE VOLTAGE OVER TEMPERATURE

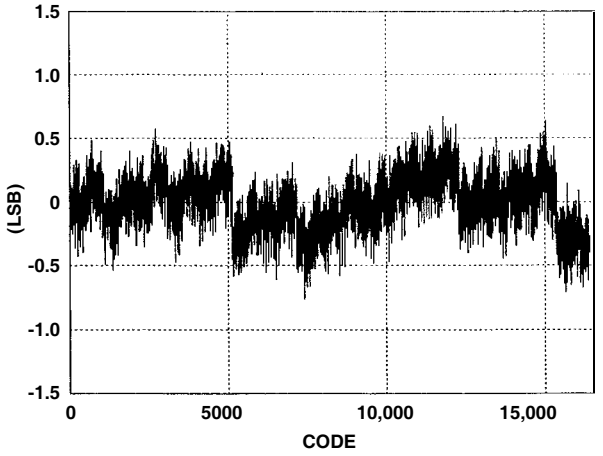


FIGURE 6. TYPICAL INL PERFORMANCE

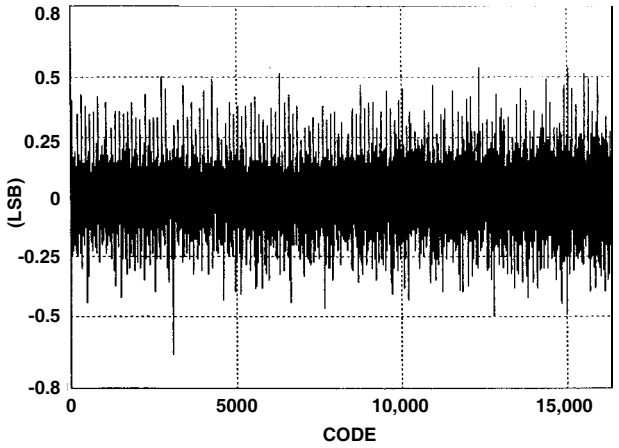


FIGURE 7. TYPICAL DNL PERFORMANCE

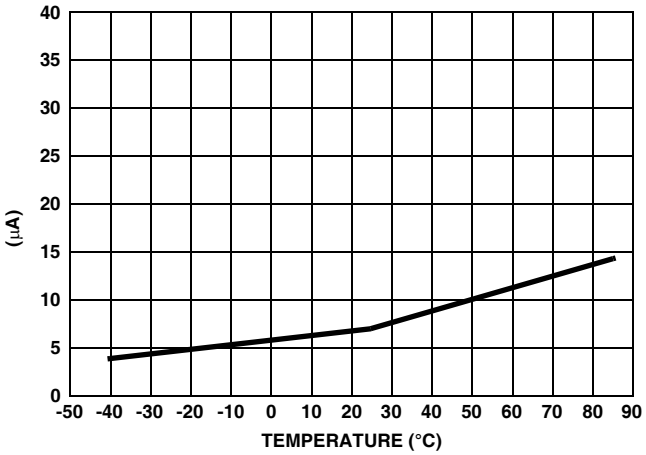


FIGURE 8. TYPICAL OFFSET CURRENT OVER TEMPERATURE

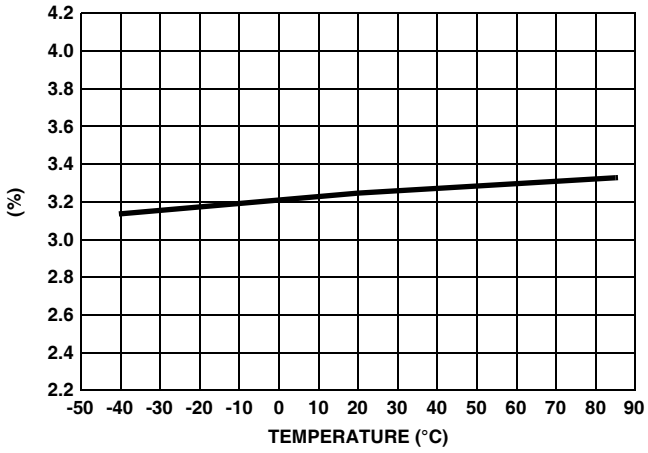


FIGURE 9. TYPICAL GAIN ERROR OVER TEMPERATURE

Typical Performance Curves (Continued)

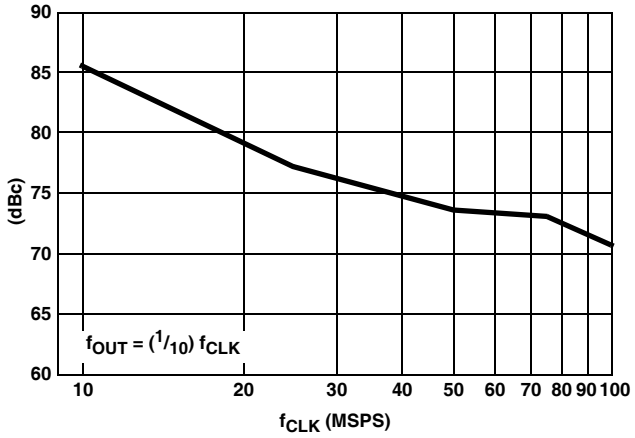


FIGURE 10. SFDR vs CLOCK FREQUENCY

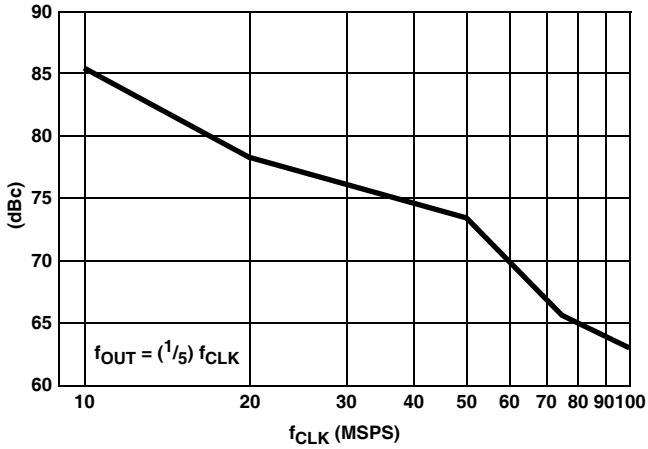


FIGURE 11. SFDR vs CLOCK FREQUENCY

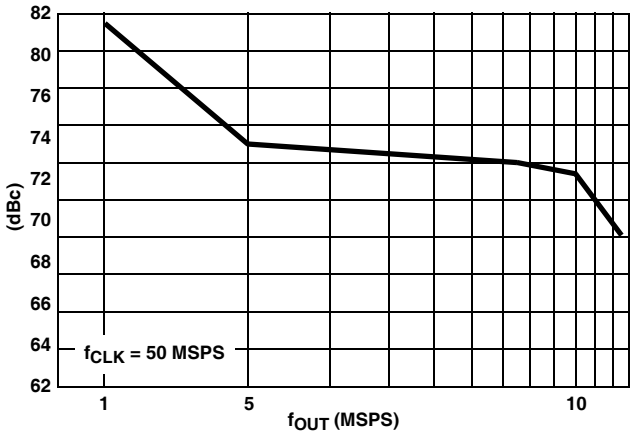


FIGURE 12. SFDR vs f_{OUT}

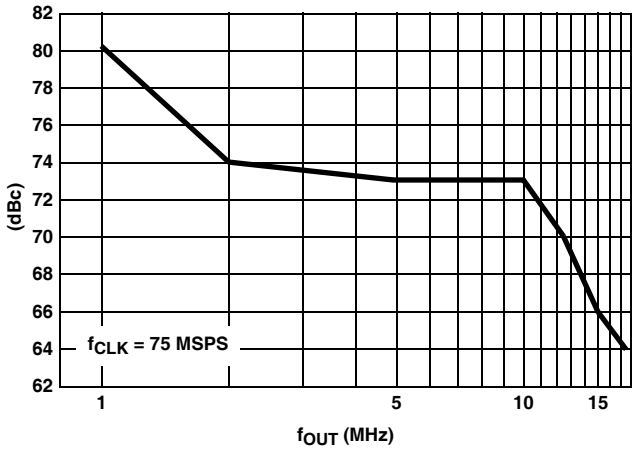


FIGURE 13. SFDR vs f_{OUT}

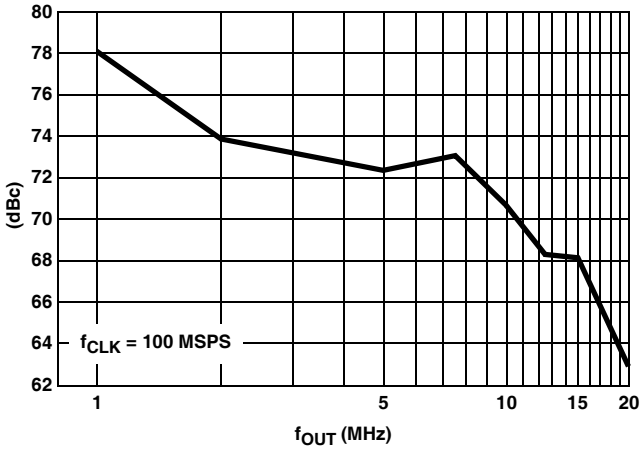


FIGURE 14. SFDR vs f_{OUT}

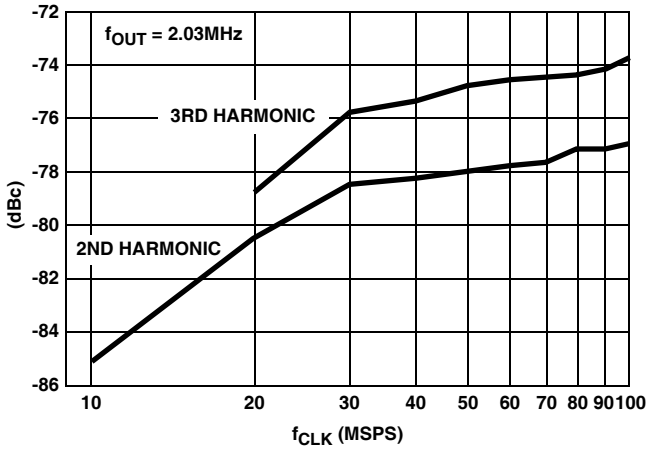


FIGURE 15. HARMONIC DISTORTION vs CLOCK FREQUENCY

Typical Performance Curves (Continued)

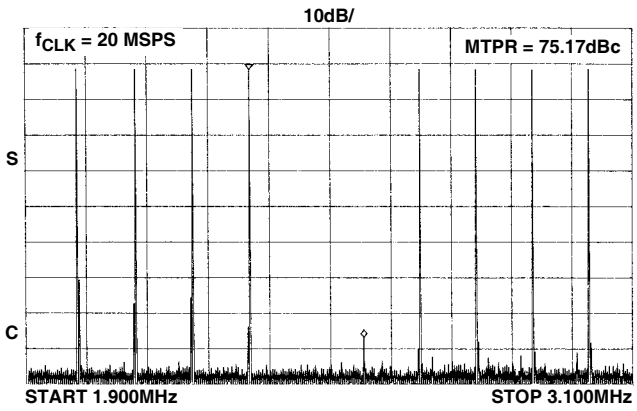


FIGURE 16. TYPICAL MTPR PERFORMANCE

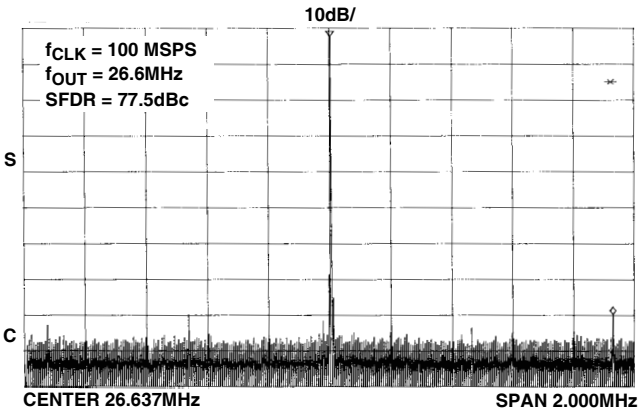


FIGURE 17. SFDR WITHIN A WINDOW

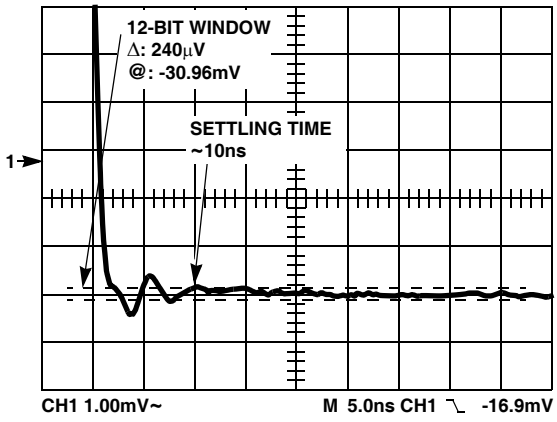


FIGURE 18. TYPICAL SETTLING TIME PERFORMANCE

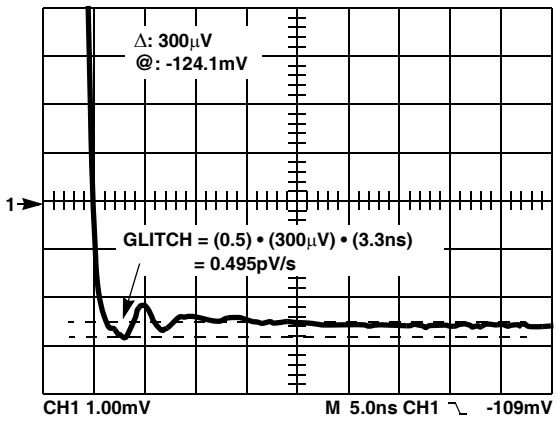


FIGURE 19. TYPICAL GLITCH ENERGY

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-14	D13 (MSB) thru D0 (LSB)	Digital Data Bit 13, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit.
15	CLK	Data Clock Pin 100kHz to 100 MSPS.
16	DV_{CC}	Digital Logic Supply +5V.
17, 28	DGND	Digital Ground.
18	DV_{EE}	-5.2V Logic Supply.
23	R_{SET}	External Resistor to set the full scale output current. I_{FS} = 16 x (V_{REFOUT}/R_{SET}). Typically 976Ω.
27	AGND	Analog Ground Supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
21	I_{OUT}	Current Output Pin.
20	$I_{\overline{OUT}}$	Complementary Current Output pin.
22	AV_{EE}	-5.2V Analog Supply.
24	CTRL AMP IN	Input to the current source base rail. Typically connected to CTRL AMP OUT and a 0.1μF capacitor to AV_{EE}. Allows external control of the current sources.
25	CTRL AMP OUT	Control amplifier out. Provides precision control of the current sources when connected to CTRL AMP IN such that I_{FS} = 16 x (V_{REFOUT}/R_{SET}).
26	REF OUT	-1.23V (typical) bandgap reference voltage output. Can sink up to 500μA or be overdriven by an external reference capable of delivering up to 2mA.

Detailed Description

The HI5741 is a 14-bit, current out D/A converter. The DAC can convert at 100 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch. Laser trimming is employed to tune linearity to true 14-bit levels. The HI5741 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5741 consumes 650mW (typical) and has an improved hold time of only 0.25ns (typical). The HI5741 is an excellent converter for use in communications applications and high performance video systems.

Digital Inputs

The HI5741 is a TTL/CMOS compatible D/A. Data is latched by a Master register. Once latched, data inputs D0 (LSB) through D13 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R ladder and segmented current source arrangement. Bits D0 (LSB) through D9 directly drive a typical R/2R network to create the binary weighted current sources. Bits D10 through D13 (MSB) pass through a "thermometer" decoder that converts the incoming data into 15 individual segmented current source enables. This split architecture helps to improve glitch, thus resulting in a more constant glitch characteristic across the entire output transfer function.

Clocks and Termination

The internal 14-bit register is updated on the rising edge of the clock. Since the HI5741 clock rate can run to 100 MSPS, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line, a shunt terminator to ground is the most effective type at a 100 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5741 CLK pin as possible.

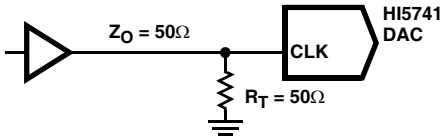


FIGURE 20. HI5741 CLOCK LINE TERMINATION

Rise and Fall times and propagation delay of the line will be affected by the shunt terminator. The terminator should be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1μF and 0.01μF ceramic capacitors placed as close to the body of the HI5741 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should also be decoupled with a 0.1μF capacitor.

Reduction of digital noise (caused by high slew rates on the bit inputs to the HI5741) can be accomplished through the use of series termination resistors. The use of serial resistors, which combine with the input capacitance of the HI5741 to induce a low pass filter characteristic, keeps the noise generated by high slew rate digital signals from corrupting the high accuracy analog data. Refer to Application Note AN9619 "Optimizing setup conditions for high accuracy measurements of the HI5741" for further details on selecting the proper value of series termination to meet application specific needs.

Reference

The internal reference of the HI5741 is a -1.23V (typical) bandgap voltage reference with 50μV/°C of temperature drift (typical). The internal reference is connected to the Control Amplifier which in turn drives the segmented current cells. Reference Out (REF OUT) is internally connected to the Control Amplifier. The Control Amplifier Output (CTRL OUT) should be used to drive the Control Amplifier Input (CTRL IN) and a 0.1μF capacitor to analog V_{EE}. This improves settling time by providing an AC ground at the current source base node. The Full Scale Output Current is controlled by the REF OUT pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = ($V_{REF\ OUT}/R_{SET}$) x 16.

The internal reference (REF OUT) can be overdriven with a more precise external reference to provide better performance over temperature. Figure 21 illustrates a typical external reference configuration.

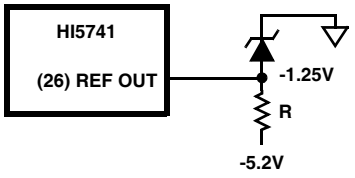


FIGURE 21. EXTERNAL REFERENCE CONFIGURATION

Multiplying Capability

The HI5741 can operate in two different multiplying configurations. For frequencies from DC to 100kHz, a signal of up to $0.6V_{P-P}$ can be applied directly to the REF OUT pin as shown in Figure 22.

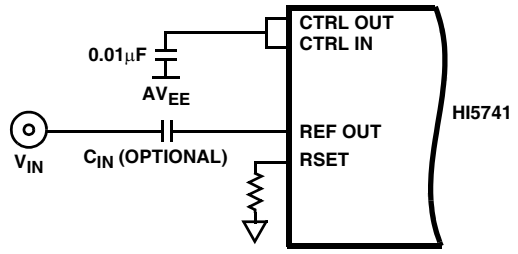


FIGURE 22. LOW FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The signal must have a DC value such that the peak negative voltage equals -1.25V. Alternately, a capacitor can be placed in series with REF OUT if a DC multiplying is not required. The lower input bandwidth can be calculated using the following formula:

$$C_{IN} = \frac{1}{(2\pi)(1400)(f_{IN})}$$

For multiplying frequencies above 100kHz, the CTRL IN pin can be driven directly as seen in Figure 23.

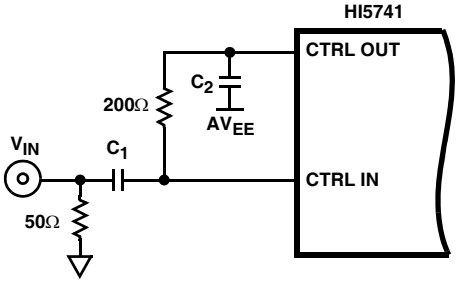


FIGURE 23. HIGH FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The nominal input/output relationship is defined as:

$$\Delta I_{OUT} = \frac{\Delta V_{IN}}{80\Omega}$$

In order to prevent the full scale output current from exceeding 20.48mA, the R_{SET} resistor must be adjusted according to the following equation:

$$R_{SET} = \frac{16V_{REF}}{I_{OUT(Full\ scale)} - \left(\frac{V_{IN(PEAK)}}{80\Omega}\right)}$$

The circuit in Figure 23 can be tuned to adjust the lower cutoff frequency by adjusting capacitor values. Table 1 illustrates the relationship.

TABLE 1. CAPACITOR SELECTION

f_{IN}	C_1	C_2
100kHz	0.01µF	1µF
>1MHz	0.001µF	0.1µF

Also, the input signal must be limited to $1V_{P-P}$ to avoid distortion in the DAC output current caused by excessive modulation of the internal current sources.

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

I_{OUT} is defined in the reference section. $I_{\overline{OUT}}$ is not trimmed to 14 bits, so it is not recommended that it be used in conjunction with I_{OUT} in a differential-to-single-ended application. The compliance range of the output is from -1.25V to 0V, with a $1V_{P-P}$ voltage swing allowed within this range.

TABLE 2. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D13-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
11 1111 1111 1111	-20.48	0
10 0000 0000 0000	-10.24	-10.24
00 0000 0000 0000	0	-20.48

Settling Time

The settling time of the HI5741 is measured as the time it takes for the output of the DAC to settle to within a ±defined error band of its final value during a $^1/_{16}$th (code 0000... to 0001 0000.... or 1111... to 1110 1111...) scale transition. In defining settling time specifications for the HI5741, two levels of accuracy are considered. The accuracy levels defined for the HI5741 are 12 (or 0.024%) and 13 (0.012%) bits.

Glitch

The output glitch of the HI5741 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically, the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source

to change before another. In order to minimize this, the Intersil HI5741 employs an internal register, just prior to the current sources, which is updated on the clock edge. Lastly, the worst case glitch on traditional D/A converters usually occurs at the major transition (i.e., code 8191 to 8192). However, due to the split architecture of the HI5741, the glitch is moved to the 1023 to 1024 transition (and every subsequent 1024 code transitions thereafter). This split R/2R segmented current source architecture, which decreases the amount of current switching at any one time, makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5741 the output is terminated into a 64Ω load. The glitch is measured at any one of the current cell carry (code 1023 to 1024 transition or any multiple thereof) throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 25 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).

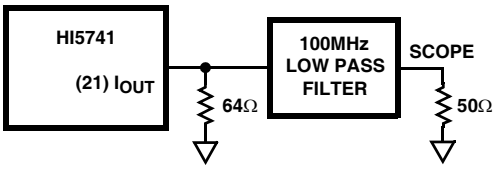


FIGURE 24. GLITCH TEST CIRCUIT

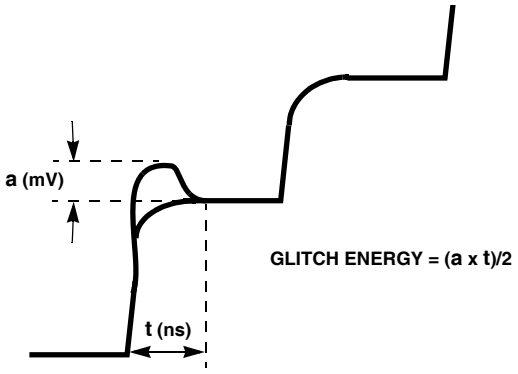


FIGURE 25. MEASURING GLITCH ENERGY

Applications

Bipolar Applications

To convert the output of the HI5741 to a bipolar 4V swing, the following applications circuit is recommended. The reference can only provide 125μA of drive, so it must be buffered to create the bipolar offset current needed to generate the -2V output with all bits 'off'. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the voltage swing and error.

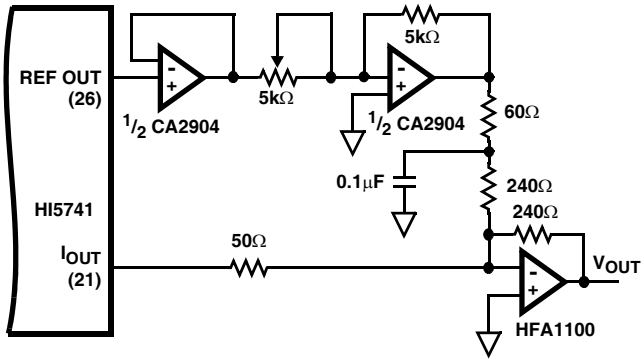


FIGURE 26. BIPOLAR OUTPUT CONFIGURATION

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit Numerically Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 27 shows how to interface an HI5741 to the HSP45106.

Definition of Specifications

Integral Linearity Error (INL) is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error (DNL) is the measure of the error in step size between adjacent codes along the converter's transfer curve. Ideally, the step size is 1 LSB from one code to the next, and the deviation from 1 LSB is known as DNL. A DNL specification of greater than -1 LSB guarantees monotonicity.

Feedthru is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time is the time required from the 50% point on the clock input for a full scale step to settle within an $\pm 1/2$ LSB error band.

Output Voltage Small Scale Settling Time is the time required from the 50% point on the clock input for a 100mV step to settle within an $1/2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area (GE) is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a volt • time specification (typically pV-s).

Differential Gain (ΔA_V) is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase ($\Delta\Phi$) is the phase error from an ideal sine wave.

Signal to Noise Ratio (SNR) is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion (THD) is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range (SFDR) is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Multi-Tone Power Ratio (MTPR) is the amplitude difference from peak amplitude to peak distortion (either harmonic or non-harmonic). An 8 tone pattern is loaded into the D/A. The tone spacing of this pattern (Δf) is created such that tones 1 through 4 and 5 through 8 are spaced equally, with tones 4 and 5 spaced at 2Δf. MTPR is measured as the dynamic range from peak power to peak distortion in the 2Δf gap.

Intermodulation Distortion (IMD) is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD can be calculated using the following equation:

$$IMD = \frac{20Log\ (RMS\ of\ Sum\ and\ Difference\ Distortion\ Products)}{(RMS\ Amplitude\ of\ the\ Fundamental)}$$

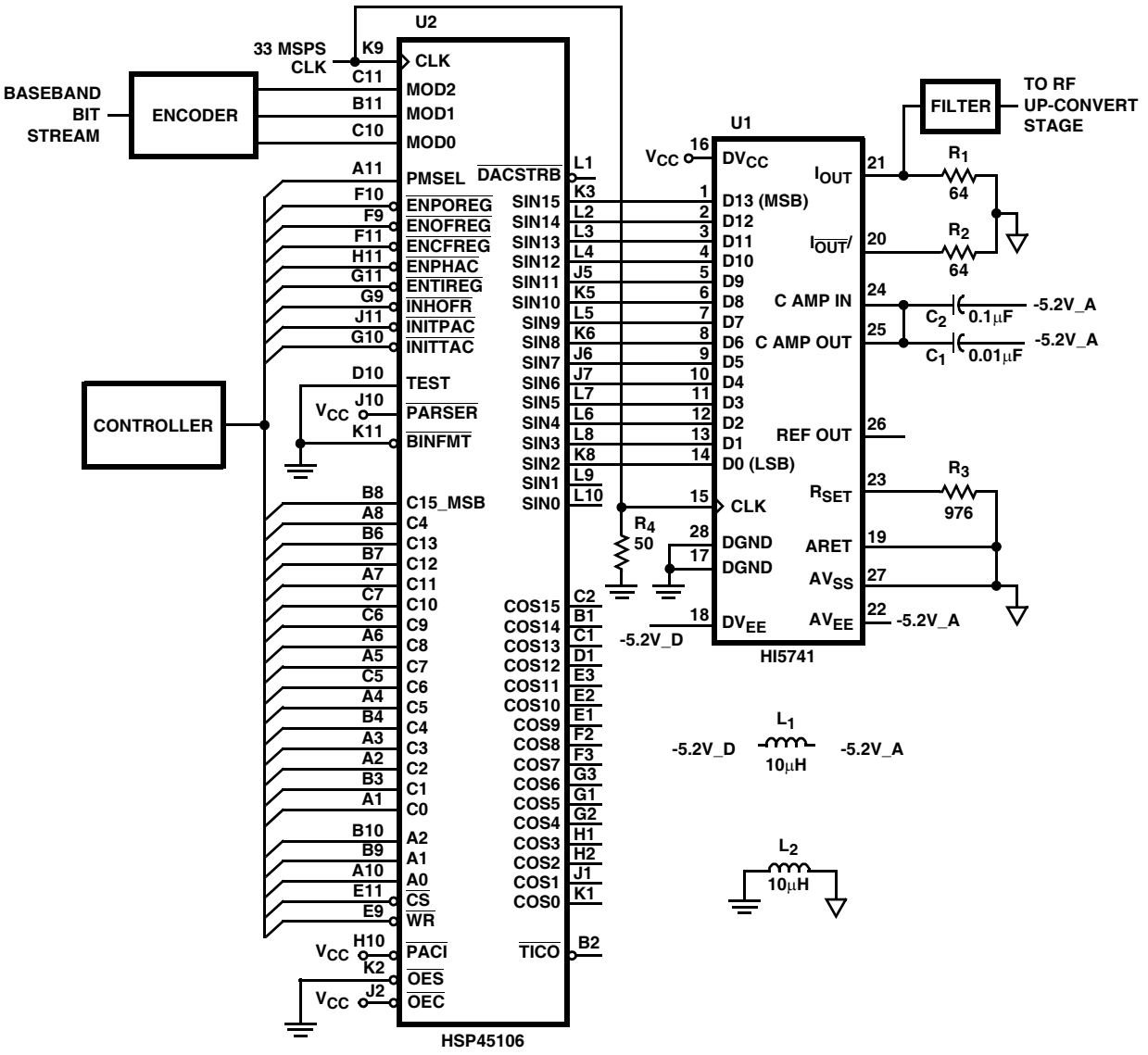
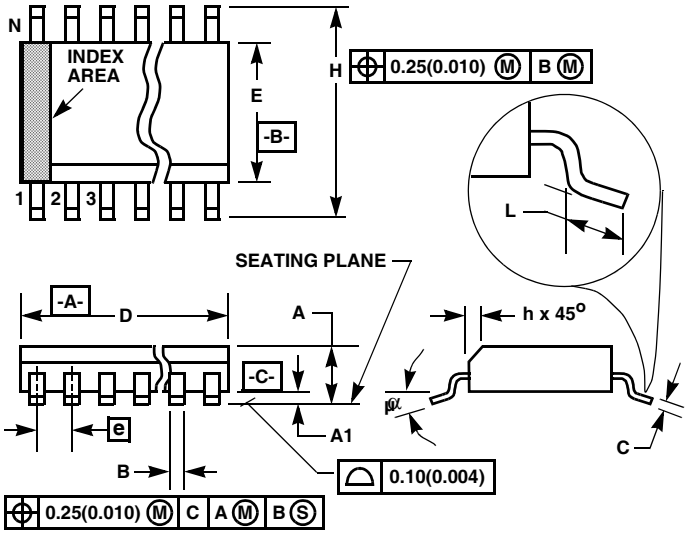


FIGURE 27. PSK MODULATOR USING THE HI5741 AND HSP45106 16-BIT NCO

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.