HIP0082, HIP0084

PRELIMINARY

May 1998

Quad Power Drivers with Serial Diagnostic Interface

Features

- Low Side Power MOSFET Output Drivers
  - Output Voltage Clamp (Typ) 80V
  - Maximum Output Current 5A/2A
  - Output $r_{DS(ON)}$ (T_J = 150°C) (Max) 0.57Ω/0.62Ω
- Controlled Slew Rate Switching (HIP0084)
- Single Pulse Energy Rating 70mJ
- Programmable Output Over Current Shutdown Threshold
  - Bit Select 2A or 5A on Outputs 3 and 4
- Output Protection
  - Output Over Current Shutdown
  - Output Over Voltage Clamp
  - Over Temperature Diagnostic Feedback
- Diagnostics for Shorts, Opens and Over Temperature
- Synchronous Serial Interface with
  - 22-Bit Serial Diagnostic Register
  - SPI Compatible Interface
- Single 5V Supply Operation with CMOS Logic Inputs
- Supply Current, I_{CC}, Full Load (Typ) . . . . . <10mA
- Low θ_{JC} Power SIP Packages
  SIP . . . . . 3°C/W
  PSOP . . . . . 2°C/W
- -40°C to 125°C Operating Temperature

Applications

- Drivers For
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Description

The HIP0082 and HIP0084 Quad Power Drivers contain four individually protected NDMOS transistor switches to drive inductive and resistive loads such as: fuel injectors, relays, solenoids, etc. The outputs are low-side switches driven by active-low CMOS logic inputs. Each output is protected against excessive current due to a short-circuit. Internal drain-to-gate zener diodes provide output clamping for over voltage. An integrated charge pump allows operation from a single 5V logic supply. Diagnostic circuits provide ground short (SG), supply short (SC) and open load (OL) detection for each of the four output stages and indicate over temperature. Diagnostic information may be read via a synchronous serial interface. Six bits of write/store data sets a long or short OL fault delay time for each output and sets Outputs 3 and 4 to a 2A or 5A current shutdown threshold. The HIP0084 is specified with controlled slew rate switching.

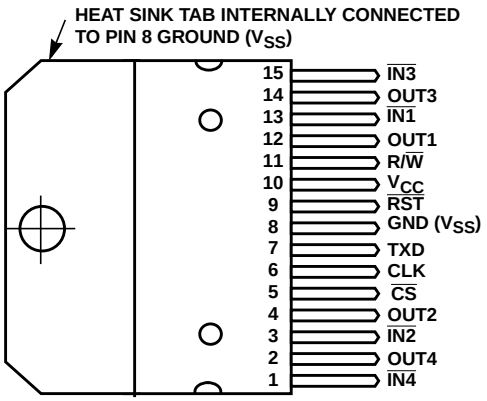
Both types are fabricated in a Power BiMOS IC process and are intended for use in automotive and other applications with a wide range of temperature and electrical stress. They are particularly suited for driving high-current inductive loads requiring high breakdown voltage and high output current. Both types available in the 15 lead Power SIP or 20 lead PSOP packages with low thermal resistance for high power applications.

Ordering Information

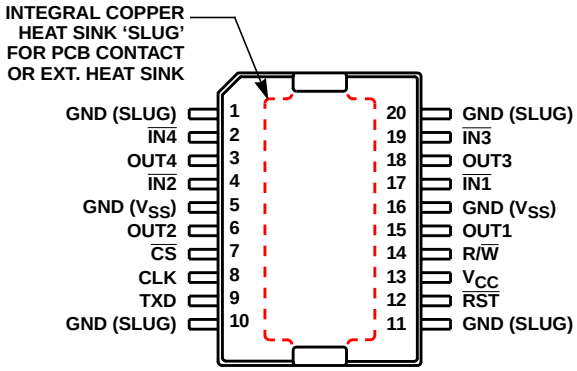
PART NUMBER	TEMP. RANGE(°C)	PACKAGE	PKG. NO.
HIP0082AS1	-40 to 125	15 Ld SIP	Z15.05A
HIP0084AS1	-40 to 125	15 Ld SIP	Z15.05A
HIP0082AS2	-40 to 125	15 Ld SIP	Z15.05B
HIP0082AB	-40 to 125	20 Ld PSOP	M20.433
HIP0084AB	-40 to 125	20 Ld PSOP	M20.433

Pinouts

HIP0082, HIP0084 (SIP)
TOP VIEW



HIP0082, HIP0084 (PSOP W/HEAT SLUG)
TOP VIEW



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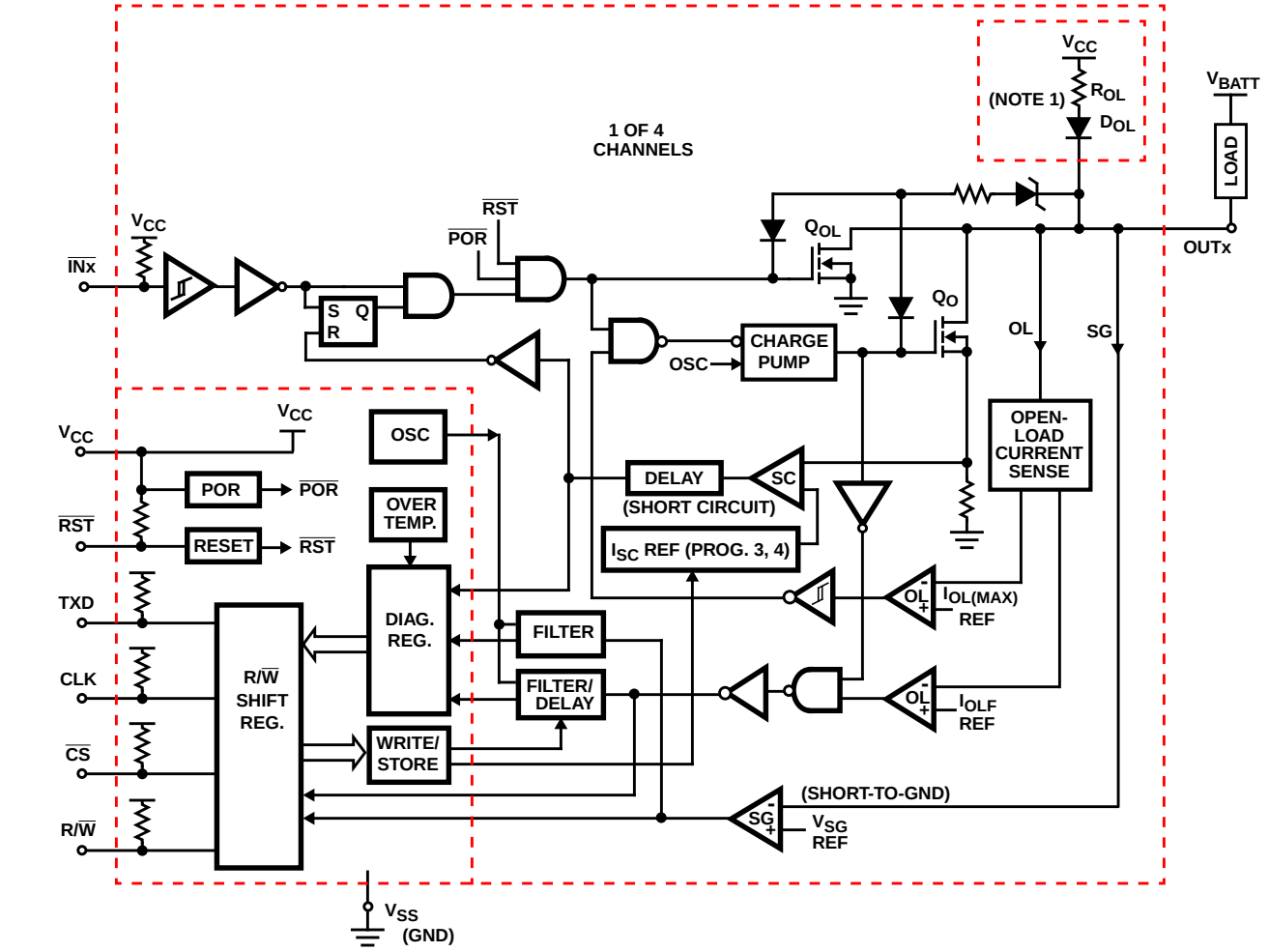
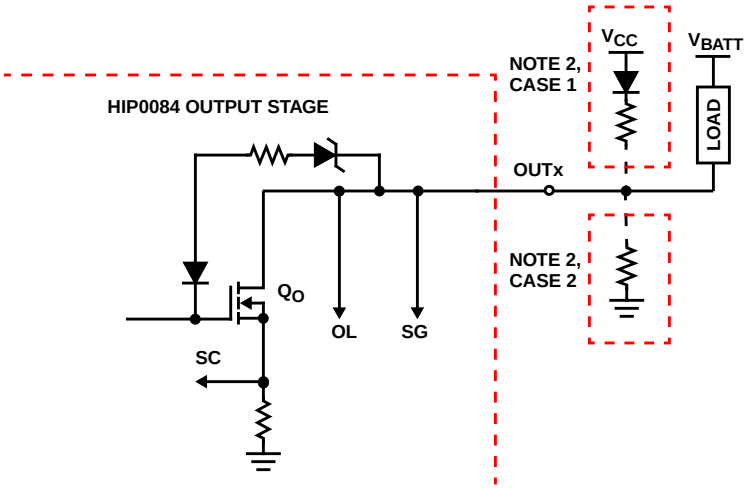
Block Diagram





NOTES:

1. For Open-Load Detection, the HIP0082 has an internal series pullup resistor, R_{OL} and diode, D_{OL} connected from OUTx to V_{CC}.
2. HIP0084 OL (Open-Load) Detection:
   Case 1: For OL Detection, an external series resistor and diode pullup connected from OUTx to V_{CC} is needed.
   Case 2: If no failure distinction for OL or SG (Short-to-GND) is required, both faults may be detected (without distinction), with an external pulldown resistor.
   For either case, the pullup or pulldown resistors should be typically 10kΩ or greater.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (Logic and Control), V_{CC} . . . . . -0.3V to 7V
Power MOSFET Drain Voltage, V_O (Note 3) . . . . . -0.7 to V_{CLAMP}
Output Clamp Energy, E_{OK} (See Note 5) 70mJ
Input Voltage (Logic and Driver Inputs), V_{IN} . . . -0.5V to V_{CC} +0.5V
Maximum Output Current, Outputs 1 and 2 . . . . . +2A
Maximum Output Current, Outputs 3 and 4 . . . . . +5A
Maximum Total Output Current, All Outputs ON . . . . . +8A
Maximum Peak Output Current, $I_{O(MAX)}$, (Note 4) . . . . . -5A to I_{SC}

Operating Conditions

Temperature Range . . . . . -40^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Notes 5, 6, 7)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
Power SIP Package	45	3
PSOP Package	40	2

Maximum Junction Temperature . . . . . -40^oC to 150^oC
Maximum Storage Temperature Range, T_{STG} . . . . -55^oC to 150^oC
Maximum Lead Temperature (During Soldering 10s) . . . . . 300^oC
(PSOP - Lead Tips Only)

Die Characteristics

Back Side Potential . . . . . V_{SS} (Tab Ground)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns on the MOSFET to hold the Drain at the V_{CLAMP} voltage. Refer to the Electrical Specifications Table for the V_{CLAMP} voltage limits.
4. Each Output has Over Current Shutdown protection in the positive current direction. The maximum peak current rating is set equal to the minimum Over Current Shutdown as detailed in the Electrical Specification Table. In the event of an Over Current Shutdown the input drive is latched OFF. The output short must be removed and the input toggled OFF and ON to restore the output drive.
5. Refer to Application Note AN9416 for Single Pulse Energy and Device Dissipation rating information, including inductive load operation and other thermal stress characterization.
6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
7. Maximum PSOP Package Dissipation at 125^oC with $26^oC/W$ Heat Sink (6 sq cm Copper PCB) is 0.96W.

Electrical Specifications $V_{CC} = 5V \pm 10\%$, $T_A = -40^oC$ to 125^oC; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0082			HIP0084			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER OUTPUTS									
Output ON Resistance (Normal Mode)	$r_{DS(ON)1}$, $r_{DS(ON)2}$	Outputs 1 and 2, One Output ON, I_{OUT} = 2A, $T_J = 150^oC$	-	-	0.62	-	-	0.62	Ω
	$r_{DS(ON)3}$, $r_{DS(ON)4}$	Outputs 3 and 4, One Output ON, I_{OUT} = 2A, $T_J = 150^oC$	-	-	0.57	-	-	0.57	Ω
Output ON Resistance (Normal Mode)	$r_{DS(ON)1}$, $r_{DS(ON)2}$	Outputs 1 and 2, One Output ON, I_{OUT} = 2A, $T_J = 75^oC$	N/A			-	-	0.5	Ω
Output ON Resistance (Normal Mode)	$r_{DS(ON)3}$, $r_{DS(ON)4}$	Outputs 3 and 4, One Output ON, I_{OUT} = 2A, $T_J = 105^oC$				-	-	0.5	Ω
Output Zener Clamp Voltage	V_Z	I_{OUT} = 40mA	73	80	90	73	80	90	V
Matching Zener Clamp Voltage	ΔV_Z	I_{OUT} = 40mA, t_Z = 100µs	N/A			-	-	±1.5	V
Output Short Current Limit, Outputs 1 and 2 (Note 8)	$I_{SC(L)}$		2	-	3.4	3	-	5.1	A
Output Short Current Limit, Outputs 3 and 4 (Note 8)	$I_{SC(L)}$	ISC Bit High	2	-	3.4	2	-	3.4	A
Output Short Current Limit, Outputs 3 and 4 (Note 8)	$I_{SC(H)}$	ISC Bit Low	5	-	7.5	5	-	8.3	A
Short Circuit Current Filter Time	t_{SC}		-	-	1	-	-	3	µs
Output Capacitance	C_O	V_{OUTX} = 16V, f = 1MHz	-	-	250	-	-	250	pF

Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to 125°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0082			HIP0084			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Positive Output Voltage Ramp Slew Rate, Inductive Load Switching Off	SR1	I_{OUTX} = 1A, Load 6mH, 12Ω; Measure 25% to 75% of V_Z	6	70	100	6	14	24	V/µs
		I_{OUTX} = 1A, Load 6mH, 12Ω; Measure 4V to 16V of V_Z	N/A			2	9	20	V/µs
		I_{OUTX} = 1A, Load 6mH, 12Ω; Measure 75% to 95% of V_Z				5.1	11	20.4	V/µs
Negative Output Voltage Ramp Slew Rate, Inductive Load Switching On	SR2	V_{BATT} = 12V, Load 6mH, 6Ω; Measure 25% to 75%, V_{CC} = 5V ±2%	0.75	15	25	0.75	1.5	3.75	V/µs
		V_{BATT} = 12V, Load 6mH, 6Ω; Measure 25% to 75%, T_J = 25°C, V_{CC} = 5V ±2%	N/A			1	-	3	V/µs
Output Negative Voltage Ramp Fall Time	t_f	I_{OUTX} = 2A, From 90% to 10%, 6Ω Load	-	-	25	-	15	25	µs
Turn-Off Delay	$t_{d(OFF)}$	I_{OUTX} = 2A, From 50% of $\overline{INx}$ to 10% of OUTx	0.5	-	3	-	-	10	µs
Turn-On Delay	$t_{d(ON)}$	I_{OUTX} = 2A, From 50% of $\overline{INx}$ to 90% of OUTx	N/A			-	-	10	µs
Matching Turn-On Delay	$\Delta t_{d(ON)}$					-	-	±3	µs
Matching Turn-Off Delay	$\Delta t_{d(OFF)}$					-	-	±3	µs
Output Rise Time	t_r	For SR3 Postive Ramp Conditions From 10% to 90% of V_Z				-		10	µs
Output Leakage Current	I_{LK}	$\overline{INx}$ = High, V_{OUTX} = 60V	-	-	10	N/A			µA
		V_{OUTX} = 60V, V_{CC} Open	-	-	10				µA
		$\overline{INx}$ = High, V_{OUTX} = V_{CC+} to 60V	N/A			-10	-	10	µA
		$\overline{INx}$ = Low, V_{OUTX} = 0V to 60V, V_{CC} = 0V				-10	-	10	µA
SUPPLY									
Power Supply Current	I_{CC}	Standby, No Load	-	7.5	15	-	7.5	15	mA
Low V_{CC} Shutdown Threshold	$V_{CC(LOW)}$	(Note 9)	3.4	3.7	4.0	3.4	3.7	4.0	V
Active Supply Range for $\overline{RST}$ Pin	$V_{CC(RST)}$		3.5	-	5.5	3.5	-	5.5	V
INPUTS ($\overline{INx}$, $\overline{CS}$, CLK, $\overline{RST}$, R/$\overline{W}$, TXD)									
Low-Level Input Voltage	V_{IL}		-0.3	-	0.2 X V_{CC}	-0.3	-	0.2 X V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 x V_{CC}	-	V_{CC} + 0.3	0.7 x V_{CC}	-	V_{CC} + 0.3	V
Input Hysteresis Voltage	V_{HYS}		0.85	1.2	2.25	0.85	1.2	2.25	V
Reset Time after $\overline{RST}$ L→H	t_{RST}		48	-	80	48	-	80	µs
Input Pull-Up Resistance	R_{IN}		50	-	150	50	-	150	kΩ
Input Current	I_{IH}	Logic High Input Voltage	-	-	2	-	-	2	µA
TXD PIN (R/$\overline{W}$ = High)									
Three-State Leakage Current	I_{LK_TXD}	$\overline{CS}$ = High, V_{TXD} = V_{CC}	-5	-	5	-5	-	5	µA
Logic High Output Voltage	V_{TXDH}	I_{OH} = -4mA, $\overline{CS}$ = Low	V_{CC} - 0.4	-	-	V_{CC} - 0.4	-	-	V
Logic Low Output Voltage	V_{TXDL}	I_{OL} = 3.2mA, $\overline{CS}$ = Low	-	-	0.42	-	-	0.42	V

Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to 125°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0082			HIP0084			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOAD DETECTION									
Output ON Resistance in High $r_{DS(ON)}$ Open-Load Detection Mode	$r_{DS(ON)1OL}$ $r_{DS(ON)2OL}$	Outputs 1 and 2, One Output ON, I_{OUT} = 10mA, T_J = 150°C	-	-	6.2	N/A			Ω
	$r_{DS(ON)3OL}$ $r_{DS(ON)4OL}$	Outputs 3 and 4, One Output ON, I_{OUT} = 10mA, T_J = 150°C	-	-	5.7				Ω
Max. Output Current in High $r_{DS(ON)}$ Mode	$I_{OL(MAX)}$		90	-	180				mA
Min. Output Current in Low $r_{DS(ON)}$ Normal Mode (Hysteresis Range)	$I_{O(HYS)}$		0.25 x I_{OL} (MAX)	-	0.95 x I_{OL} (MAX)	NA			mA
Open-Load Fault Threshold	I_{OLF}	(ISC Bit is set in Fault Register)	3	-	20	15	60	100	mA
Open-Load Detection Pull-up Resistance	R_{OL}		2	-	6.5	NA			kΩ
Open-Load Delay Time after $\overline{INx}$ H→L	t_{DOLL}	Td_OLx Bit = Low	3	-	5.2	3	-	5.2	ms
Open-Load Delay Time after $\overline{INx}$ H→L	t_{DOLH}	Td_OLx Bit = High (Note 10)	340	-	580	340	-	580	µs
Open Load Filter Time	t_{OL}		150	-	252	150	-	252	µs
OVER TEMPERATURE AND SHORT CIRCUIT PROTECTION									
Over Temperature Detection Threshold	T_{TMP}		155	-	165	155	-	165	°C
Output Short-to-Gnd Threshold	V_{SG}		2.4	-	2.9	2.4	2.6	2.9	V
Short-to-GND Filter Time	t_{SG}		150	-	252	150	-	252	µs
SERIAL INTERFACE (Figure 3) C_{EXT} = 50pF									
Serial Clock Frequency	f_{CLK}	50% Duty Cycle	-	-	3	-	-	3	MHz
Propagation Delay CLK to Data Valid	t_{PCLKDV}		-	-	150	-	-	150	ns
Setup Time, $\overline{CS}$ to CLK	t_{CSLCLK}		150	-	-	150	-	-	ns
$\overline{CS}$ Low to Data Valid	t_{CSLDV}		-	-	100	-	-	100	ns
Hold Time $\overline{CS}$ after CLK	t_{CLKCSH}		150	-	-	150	-	-	ns
$\overline{CS}$ High to Output High Z	t_{CSHDZ}		-	-	100	-	-	100	ns
Minimum Time CLK = High	t_{CLKH}		100	-	-	100	-	-	ns
Minimum Time CLK = Low	t_{CLKL}		100	-	-	100	-	-	ns
Setup Time R/$\overline{W}$ Low to CLK	t_{RWLCLK}		150	-	-	150	-	-	ns
R/$\overline{W}$ Low to Output High Z	t_{RWLDZ}		-	-	100	-	-	100	ns
Setup Time Data Valid to CLK Low	t_{DVCLKL}		20	-	-	20	-	-	ns
Setup Time R/$\overline{W}$ High to CLK	t_{RWHCLK}		100	-	-	100	-	-	ns
Time R/$\overline{W}$ High to Data Valid	t_{RWHDV}		-	-	100	-	-	100	ns

NOTES:

8. Each Output has Over Current Shutdown protection in the positive current direction. The maximum peak current rating is set equal to the minimum Over Current Shutdown as detailed in the Electrical Specification Table. In the event of an Over Current Shutdown the input drive is latched OFF. The output short must be removed and the input toggled OFF and ON to restore the output drive.
9. The "Low V_{CC} Shutdown" is an internal control that switches off all power drive stages when V_{CC} is less than $V_{CC(LOW)}$.
10. Measurement includes the Filter Time.

Functional Description

Power Output Stages

The Block Diagram details the equivalent logic control of each power output driver. Each power output stage has a separately controlled input with hysteresis and is active low with a pull-up to maintain an off state when there is no input. Each output driver has sensors for short circuit, open load and short-to-ground fault detection. The drive to each output is also controlled by the POR, Reset and an RS latch that switches off the output when a short circuit occurs. An internal zener diode feedback from the drain to gate of the output driver provides over voltage clamp protection.

For the HIP0082, each power output channel has a low $r_{DS(ON)}$ (Q_O) and a high $r_{DS(ON)}$ (Q_{OL}) NDMOS drivers in parallel. The high $r_{DS(ON)}$ driver is used to enhance the open load detection while providing one-tenth of the output load current.

The HIP0084 output is modified into one low $r_{DS(ON)}$ driver and provides controlled slew rate switching. In addition, the HIP0084 requires an external zener and resistor network for OL detection. Refer to the Block Diagram, Specifications and OL Detection information.

Reset Operation

An active low reset on the $\overline{RST}$ pin or the writing of a Low to the Test Bit is required to guarantee normal operation after power-up. When $\overline{RST}$ is in the low state all outputs are off and all registers and counters are reset. When the reset pin is taken high the IC remains in reset mode for a time t_{RST}.

When the $\overline{RST}$ pin is switched active low, the on-chip reset circuitry ensures that the output stages are turned off, all counters and registers are reset, and the programmable functions are in their default states. The default state for the Test Bit is a Low. The default state for the short-circuit current for outputs 3 and 4 is the higher value for 5A maximum current operation (ISC Bit Low). The default state for the open-load delay times for each output is the higher value between 3ms and 5.2ms (Td_OLx Bits Low).

Low Power Drive Shutdown

As part of the POR function, there is a low voltage power drive shutdown when the supply voltage, V_{CC} drops below the voltage threshold, $V_{CC(LOW)}$. During the low voltage condition the output stages are held off.

Over Voltage Clamp Operation

A drain-to-gate zener diode on each output driver internally clamps an over voltage pulse, including the kick pulse generated when turning off an inductive load. While providing over voltage protection, it is not part of the diagnostic feedback via the Diagnostic Register.

Short-Circuit (SC) Protection

If the output current is above the current limit for a time delay greater than t_{SC} the output is switched off and the corresponding bit in the diagnostic register set. The current level for shutdown on outputs 3 and 4 is programmable between 2A and 5A with the ISC bit. After shutdown, the output remains off until the corresponding input is taken high and again low.

Open-Load (OL) Detection

Load currents are monitored while the outputs are ON. If the open load current falls below the fault threshold current, I_{OLF}, the open load fault bit is set after a delay time t_{DOL}. The open load fault bits (OLx) are stored in the diagnostic register as shown in Figure 1. The output of open-load detector circuit is input to the Diagnostic Register via the delay filter and is also connected directly to the R/$\overline{W}$ Shift Register for potential monitoring via the serial interface.

For the HIP0082 in an ON state, if a load current falls below the I_{OL} threshold level, a low load current condition is detected and the low $r_{DS(ON)}$, high current DMOS output transistor (Q_O) is switched off. The high $r_{DS(ON)}$ driver (Q_{OL}) continues to conduct. If the load current is then increased from a low level, Q_O will be switched on, with hysteresis, to a normal mode of operation as defined by the $I_{OL(HYS)}$ limits. When the output current is higher than $I_{OL(MAX)}$, both Q_O and Q_{OL} conduct.

The HIP0084 OL detection diagnostics differ from the HIP0082. The HIP0084 does not have an internal pullup resistor (shown in the Block Diagram of the HIP0082 as R_{OL} in series with the diode, D_{OL}) connected between OUTx and V_{CC}. Where no failure distinction between an OL and a SG fault condition is required, an external pulldown resistor from OUTx-to-Ground may be used. For a distinction between an OL and SG fault condition, an external pullup resistor in series with a diode between OUTx and V_{CC} is needed. The pullup resistor must have a value greater than $(V_{CC} - V_{BE} - V_{SG})/I_{OLF}$ where V_{CC} is the external power supply voltage for the outputs, V_{BE} is the diode drop of the series diode; V_{SG} is the short-to-ground comparator threshold level for OUTx and I_{OLF} is the open-load current detection threshold of OUTx. While the values for pullup and pulldown resistors are not critical, they should not be minimally small. In either case, they should be typically 10kΩ or greater.

Output Short-to-Ground (SG) Detection

When the voltage on an output pin is below V_{SG} and the output is off, a ground short is detected and stored in the diagnostic register after a delay t_{SG}. The outputs of the short-to-ground (SG) comparators are also connected directly to the diagnostic register so that they can be monitored via the serial interface. Where V_{SG} is specified in the range of 2.4V to 2.9V, I_{OLF} is specified in the range of 15mA to 100mA for the HIP0084 and 3mA to 20mA for the HIP0082.

Serial Interface Operation

Microprocessor communication to the diagnostic/control registers is via a 4 wire serial interface. Data control is bidirectional, the direction of data transfer being dependent on the state of the R/$\overline{W}$ pin (See Figure 2).

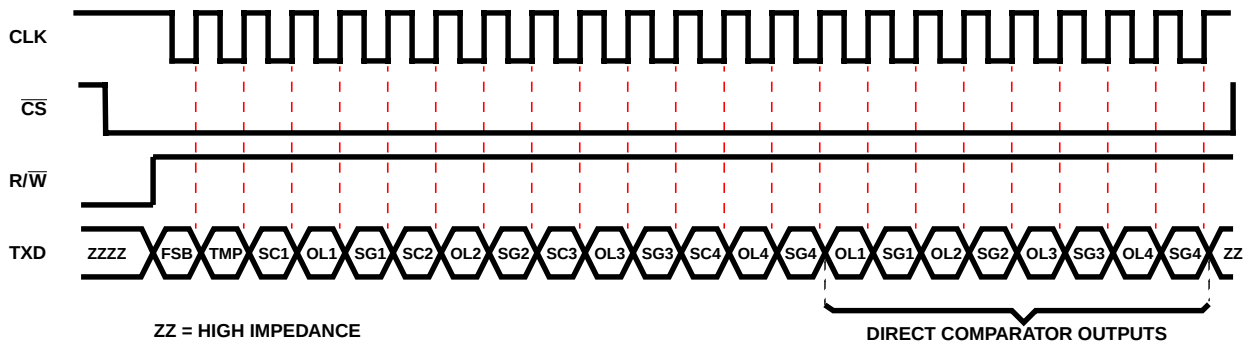


FIGURE 1. SERIAL INTERFACE READ OPERATION

Diagnostic Read Operation

When $\overline{CS}$ goes from high to low (while CLK is high), data from the diagnostic register is jammed into the serial shift register, At the same time, the TXD pin exits three-state and outputs the FSB bit which indicates whether any of the fault bits in the shift register are set. With the first negative transition of CLK, the diagnostic register is cleared. Data from the shift register is shifted to TXD on each low to high transition of the CLK pulse. The Diagnostic Fault Bits as shown in Figure 1 are described as follows:

FSB Bit - Indicates that one or more of the bits in the diagnostic register are set.

TMP Bit - Indicates that the chip temperature has exceeded the limit T_{TMP}. The outputs are not switched off when this occurs; the condition is indicated by the setting of the TMP bit. Sensors for the TMP bit are located near the power drivers and are ORed to provide a single bit for the chip.

SCx Bits - Indicate a short-circuit to battery or over current on the corresponding output. The corresponding output driver has been latched off. It will remain off until the input is toggled off and then on.

OLx Bits - Indicate that no load (or a high resistance load) is connected to the corresponding output. The open load bit is set when the output current is less than I_{OLF}.

SGx Bits - Indicate that the voltage on the corresponding output is below the V_{SG} limit.

The final 8 bits (most significant bits) of the diagnostic word indicate the states of the open load and short-to-ground comparators when the $\overline{CS}$ pin went from high to low. As such, an external microprocessor can monitor the status of the OL and SG comparators directly to cross-check the action of the filtered fault bits, OL1 to OL4 and SG1 to SG4 (See Figure 1). The action of the filters is to suppress switching anomalies that may be read as false data. To avoid potential confusion in normal operation, reading the direct comparator output bits is not necessary or recommended.

Diagnostic Write Operation

When the R/$\overline{W}$ pin is in the low state it is possible to write six bits to the Write/Store register to influence the IC mode of operation. The write operation is illustrated in Figure 3. The FSB (First Significant Bit) is present when $\overline{CS}$ pin goes from high to low while the CLK pin is high and the R/$\overline{W}$ pin is in the high (read) state. The FSB is the error flag and is the same FSB bit shown for the Figure 1 read operation. When FSB is high, a read operation is assumed, until or unless the R/$\overline{W}$ goes low. When the R/$\overline{W}$ pin goes low (write mode), TXD is ready to receive input data. The first write bit occurs when CLK goes low.

In the write mode, data is latched in the Write/Store register when $\overline{CS}$ goes high. The Write/Store data will be in the default state after a $\overline{RST}$ reset or power up reset. The write operation does not affect the data present in the Diagnostic Register and a read operation does not affect the data present in the Write/Store Register.

The programmable bits in the Write/Store register are:

Test Bit - Used to put the IC in test mode (not recommended). This bit should be low for normal operation.

ISC Bit - This bit programs the short circuit level for outputs 3 and 4. When this bit is set high the lower value for the current shutdown threshold is set.

Td_OLx Bits - The t_{DOL} delay times for the Td_OLx Bits are programmable to two levels (t_{DOLL} or t_{DOLH}). These bits set the delay times for the open-load detection at each of the four outputs. A logical high sets the open-load delay time to its shorter value.

Reading Serial Data on the SPI Interface

When interfacing to an 8-bit SPI system and choosing to read all 22 bits as shown in Figure 1, note that the FSB (First Significant Bit) is the first bit present before the first CLK pulse goes low. This leaves 21 bits of available output data to be shifted by the CLK.

An FSB high state when $\overline{CS}$ goes low indicates the presents of a fault bit in the Diagnostic Register. The FSB bit is normally used as a flag to initiate a read of all data bits in the shift register. The FSB output bit should be separately directed to an interrupt or port that is programmed to initiate a fault data read sequence.

Since SPI data is read 8 bits at a time, reading 24 bits leaves 3 (dummy) bits that follow after the 21 bits of diagnostic fault output data. Internally, the shift register has an input low state which will cause the last 3 bits shifted out to be low.

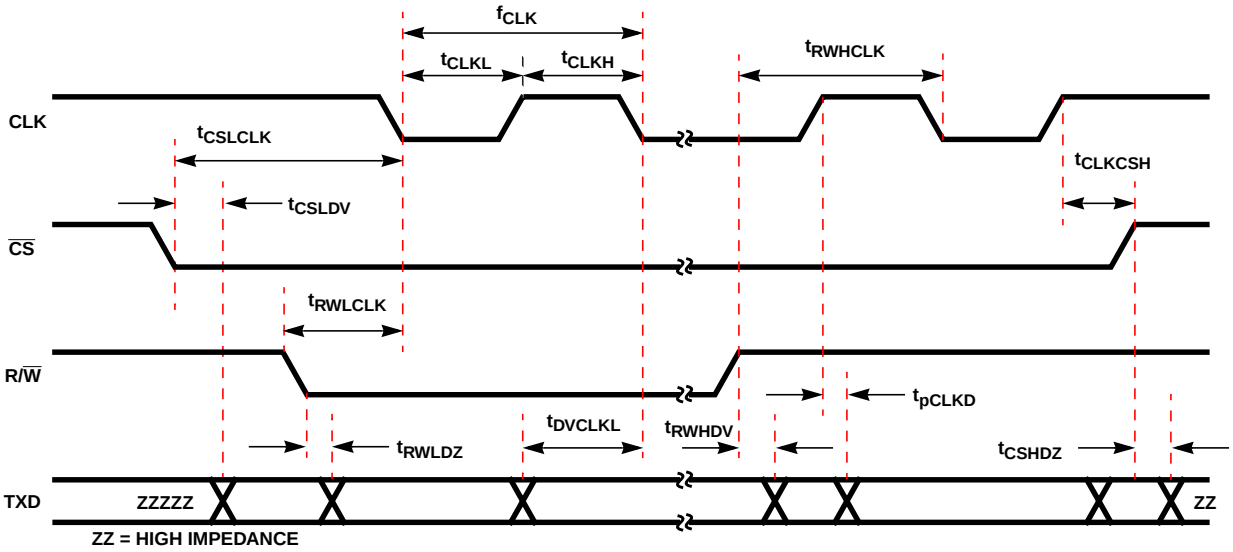


FIGURE 2. SERIAL INTERFACE TIMING DIAGRAM

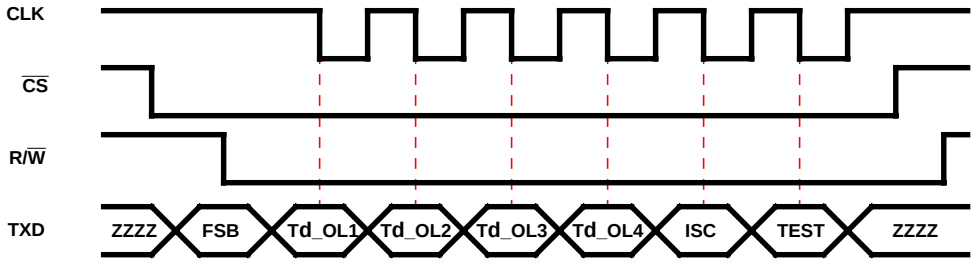


FIGURE 3. SERIAL INTERFACE WRITE OPERATION

There is no need in normal operation to read the Direct Comparator output bits, except to directly read the fault state when $\overline{CS}$ goes low or to cross-check on the filtered OL and SG fault data. If the Direct Comparator data is ignored, then only 16 bits of SPI data is read. In this case the last 3 bits in the 16 bit sequence is the first 3 bits of Direct Comparator data which can be ignored.

Data read from a SPI interface starts with the first clock pulse. The $\overline{CS}$ and R/$\overline{W}$ inputs cannot be changed while reading data from the shift register. And, as noted, an internal low on the shift register input causes low data bits to follow the 21 bits of diagnostic data.

While the Write/Store operation calls for 6 bits of data, a SPI write will output 8 bits. The first 2 bits transmitted should be dummy bits. The 3-bit is the Test bit which should be low for normal operation. The Test bit is used to facilitate testing in the manufacturing process and is not recommended for other use. The 6 programmable bits are described in the section on Diagnostic Write Operation.

Pin Descriptions

V_{CC} and GND - 5V Supply and Ground connections. A charge pump is used to boost the Power MOSFET gate drive. This allows a single 5V supply to satisfy all logic and drive requirements.

OUT1 - OUT4 - Low-side output drivers with 0.62Ω (OUT1 and OUT2) or 0.57Ω (OUT3 and OUT4) on resistance. The outputs are provided with over current shutdown and over voltage clamping. Additionally, open-load and short-to-ground detection is carried out when the outputs are ON.

$\overline{IN1}$ - $\overline{IN4}$ - Active-low CMOS logic inputs which control the output stages OUT1 - OUT4. These inputs are provided with pull-up resistors.

$\overline{RST}$ - Active-low logic-level reset input with internal pull-up resistor.

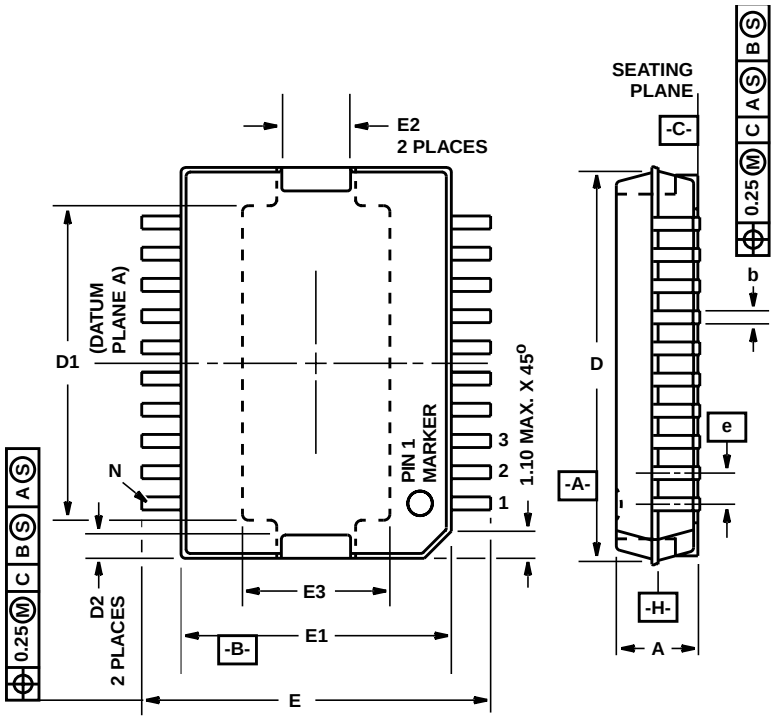
CLK - Clock input for synchronous serial interface with internal pull-up resistor. This input must be high when $\overline{CS}$ transitions from high to low.

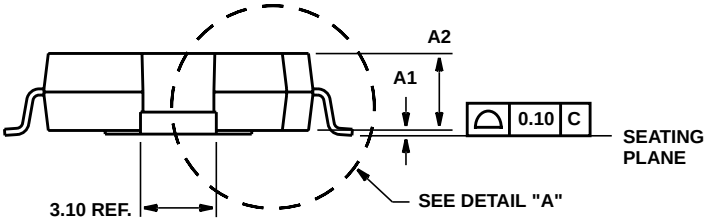
$\overline{CS}$ - Active-low chip select input for serial interface. This input has an internal pull-up resistor.

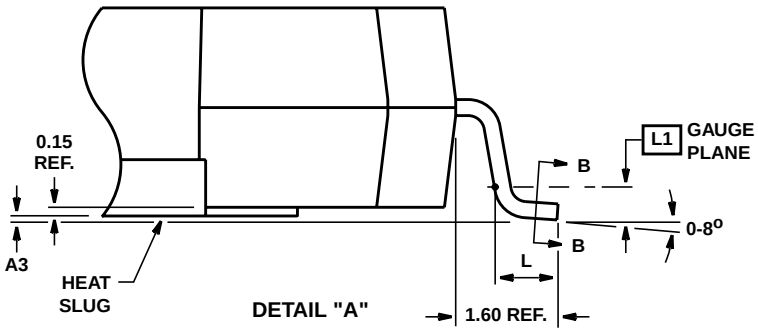
R/$\overline{W}$ - Read/write control pin for serial interface. This input controls whether the TXD pin is an input or output. This input has an internal pull-up resistor.

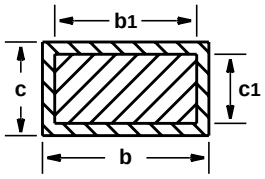
TXD - Bidirectional data pin for serial interface. When R/$\overline{W}$ is high diagnostic data can be read from HIP0082. When R/$\overline{W}$ is low, 6 bits may be written to the internal program register.

Power Small Outline Plastic Package (PSOP)









SECTION "B-B"

M20.433

20 LEAD POWER SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.122	0.142	3.10	3.60	-
A1	0.004	0.012	0.10	0.30	-
A2	0.118	0.130	3.00	3.30	-
A3	0.000	0.004	0.00	0.10	-
b	0.016	0.021	0.40	0.53	6, 7
b1	0.016	0.020	0.40	0.50	6, 7
c	0.009	0.013	0.23	0.32	7
c1	0.009	0.011	0.23	0.29	7
D	0.622	0.630	15.80	16.00	3
D1	0.496	0.512	12.60	13.00	-
D2	-	0.043	-	1.10	-
E	0.547	0.571	13.90	14.50	-
E1	0.429	0.437	10.90	11.10	4
E2	-	0.114	-	2.90	-
E3	0.228	0.244	5.80	6.20	-
e	0.050 BSC		1.27 BSC		-
L	0.031	0.043	0.80	1.10	5
L1	0.014 BSC		0.35 BSC		-
N	20		20		-

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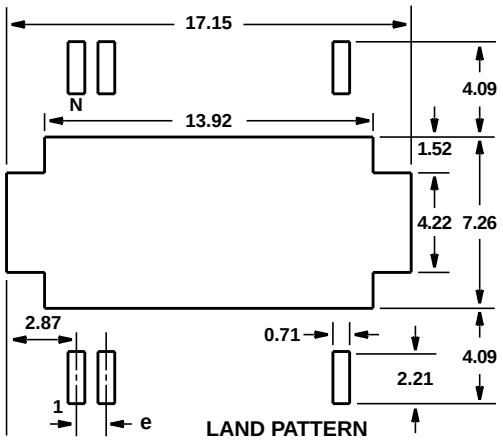
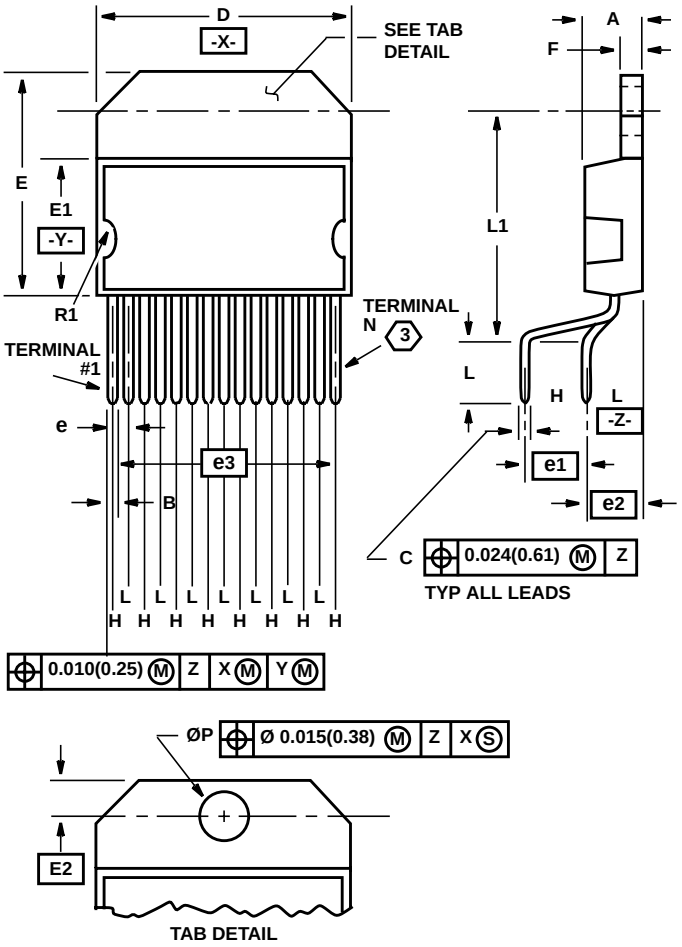
NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "C" is a reference datum. Seating plane is defined by lead tips only.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side. D measured at -H-.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side. E1 measured at -H-.
5. Dimension "L" is the length of terminal for soldering to a substrate.
6. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the lead width dimension at maximum material condition.
7. Section "B-B" to be determined at 0.10mm to 0.25mm from the lead tip.
8. Controlling dimension: MILLIMETER.
9. Dimensions conform with JEDEC Outline MO-166AA Issue B.



LAND PATTERN

Single-In-Line Plastic Packages (SIP)



Z15.05A (JEDEC MO-048 AB ISSUE A)
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE STAGGERED VERTICAL LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e1	0.200 BSC		5.08 BSC	
e2	0.169 BSC		4.29 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

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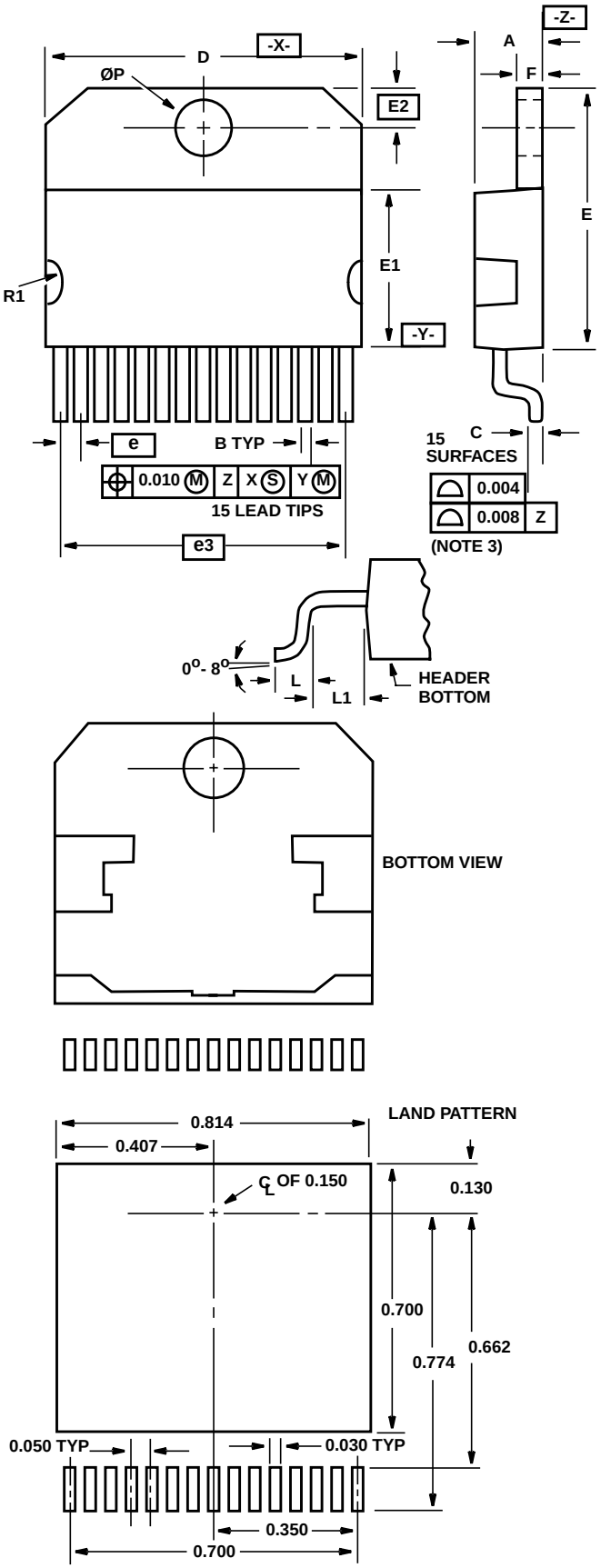
NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP)



Z15.05B

15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.018	0.024	0.46	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.065	0.080	1.66	2.03
L1	0.098	0.108	2.49	2.74
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

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NOTES:

1. Dimensioning and Tolerancing per ANSI Y14.5M - 1982.
2. N is the number of terminals.
3. All lead surfaces are within 0.004 inch of each other. No lead can be more than 0.004 inch above or below the header plane, (-Z- Datum).
4. Controlling dimension: INCH.

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