4M High Speed SRAM (512-kword × 8-bit)

HITACHI

ADE-203-1035A (Z) Rev. 1.0 Apr. 15, 1999

Description

The HM628511HI Series is a 4-Mbit high speed static RAM organized 512-k word \times 8-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell)and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 36-pin plastic SOJ.

Features

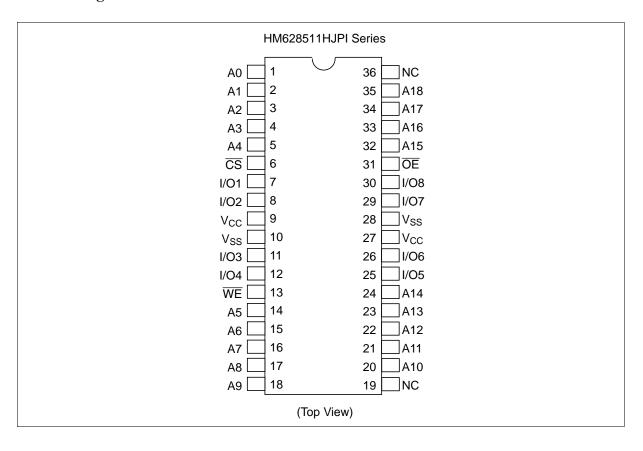
- Single 5.0 V supply : $5.0 \text{ V} \pm 10 \%$
- Access time 12 /15 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 160 / 140 mA (max)
- TTL standby current: 60 / 50 mA (max)
- CMOS standby current : 5 mA (max)
- Center V_{CC} and V_{SS} type pinout
- Temperature range: -40 to 85°C



Ordering Information

Type No.	Access time	Package
HM628511HJPI-12	12 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM628511HJPI-15	15 ns	

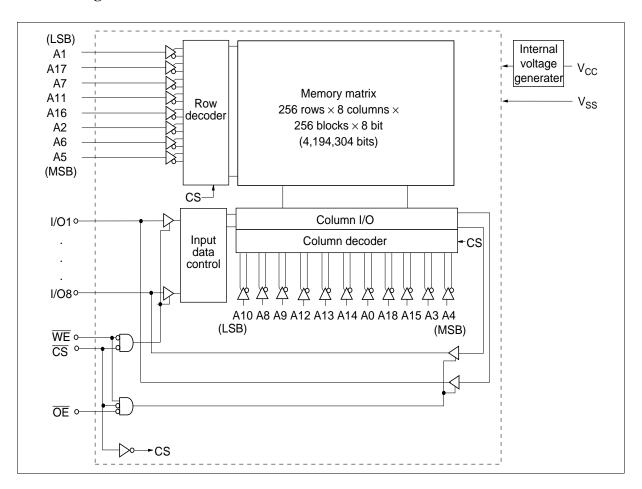
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS	Chip select
ŌĒ	Output enable
WE	Write enable
V _{cc}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS	OE	WE	Mode	V _{cc} current	I/O	Ref. cycle
Н	×	×	Standby	I _{SB} , I _{SB1}	High-Z	_
L	Н	Н	Output disable	I _{cc}	High-Z	_
L	L	Н	Read	I _{cc}	Dout	Read cycle (1) to (3)
L	Н	L	Write	I _{cc}	Din	Write cycle (1)
L	L	L	Write	I _{cc}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	
Supply voltage relative to V _{ss}	V _{cc}	-0.5 to +7.0	V	
Voltage on any pin relative to V _{ss}	V _T	-0.5*1 to V _{CC} +0.5*2	V	
Power dissipation	P _T	1.0	W	
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +125	°C	
Storage temperature under bias	Tbias	-40 to +85	°C	

Notes: 1. V_{T} (min) = -2.0 V for pulse width (under shoot) \leq 8 ns

2. V_T (max) = V_{CC} +2.0 V for pulse width (over shoot) ≤ 8 ns

Recommended DC Operating Conditions ($Ta = -40 \text{ to } +85^{\circ}\text{C}$)

Parameter	Symbol	Min	Тур	Max	Unit
Supply voltage	V _{CC} *3	4.5	5.0	5.5	V
	V _{SS} *4	0	0	0	V
Input voltage	V _{IH}	2.2	_	V _{CC} + 0.5*2	V
	V _{IL}	-0.5* ¹	_	0.8	V

Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 8 ns

- 2. V_{IH} (max) = V_{CC} +2.0 V for pulse width (over shoot) \leq 8 ns
- 3. The supply voltage with all $\rm V_{\rm cc}$ pins must be on the same level.
- 4. The supply voltage with all $V_{\rm SS}$ pins must be on the same level.

DC Characteristics (Ta = -40 to +85°C, V_{CC} = 5.0 V \pm 10 %, V_{SS} = 0V)

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		II _{LI} I	_	_	2	μΑ	$Vin = V_{SS} to V_{CC}$
Output leakage current		II _{LO} I	_	_	2	μΑ	$Vin = V_{SS}$ to V_{CC}
Operation power supply current	12 ns cycle	I _{cc}	_	_	160	mA	$\frac{\text{Min cycle}}{\text{CS}} = V_{\text{IL}}, \text{ lout} = 0 \text{ mA}$ $\text{Other inputs} = V_{\text{IH}}/V_{\text{IL}}$
	15 ns cycle	I _{cc}	_	_	140		
Standby power supply current	12 ns cycle	I _{SB}	_	_	60	mA	Min cycle, $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	15 ns cycle	I _{SB}	_	_	50		
		I _{SB1}	_	0.1	5	mA	$ f = 0 \text{ MHz} \\ V_{\text{CC}} \ge \overline{\text{CS}} \ge V_{\text{CC}} - 0.2 \text{ V}, \\ (1) \ 0 \ V \le V \text{in} \le 0.2 \text{ V or} \\ (2) \ V_{\text{CC}} \ge V \text{in} \ge V_{\text{CC}} - 0.2 \text{ V} $
Output voltage		V _{OL}	_	_	0.4	V	I _{OL} = 8 mA
		V _{OH}	2.4	_	_	V	$I_{OH} = -4 \text{ mA}$

Notes: 1. Typical values are at V_{cc} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Тур	Max	Unit	Test conditions
Input capacitance*1	Cin	_	_	6	pF	Vin = 0 V
Input/output capacitance*1	C _{I/O}	_	_	8	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = -40 to +85 °C, V_{CC} = 5.0 V \pm 10 %, unless otherwise noted.)

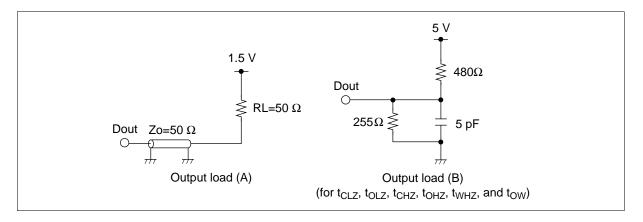
Test Conditions

• Input pulse levels: 3.0 V/0.0 V

• Input rise and fall time: 3 ns

• Input and output timing reference levels: 1.5 V

• Output load: See figures (Including scope and jig)



Read Cycle

			11111020311111					
		-12		-15				
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes	
Read cycle time	t _{RC}	12	_	15	_	ns		
Address access time	t _{AA}	_	12	_	15	ns		
Chip select access time	t _{ACS}	_	12	_	15	ns		
Output enable to outpput valid	t _{oe}	_	6	_	7	ns		
Output hold from address change	t _{oh}	3	_	3	_	ns		
Chip select to output in low-Z	t _{CLZ}	3	_	3	_	ns	1	
Output enable to output in low-Z	t _{OLZ}	0	_	0	_	ns	1	
Chip deselect to output in high-Z	t _{CHZ}	_	6	_	7	ns	1	
Output disable to output in high-Z	t _{OHZ}	—	6	_	7	ns	1	
` `	·		·				·	

HM628511HI

Write Cycle

ШΛ	16	285	11	ш
пι	vi O.	203		п

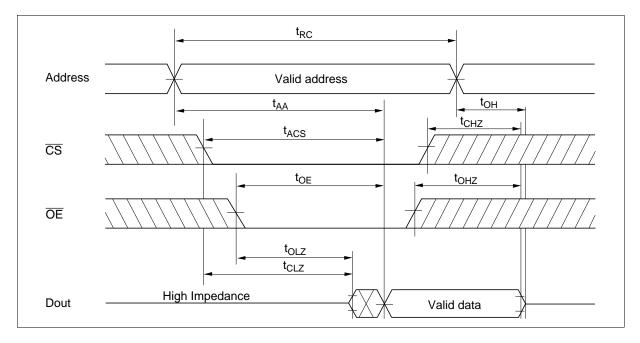
		-12 Min Max		-15 Min Max			Notes
Parameter	Symbol					Unit	
Write cycle time	t _{wc}	12	_	15	_	ns	
Address valid to end of write	t _{AW}	8	_	10	_	ns	
Chip select to end of write	t _{cw}	8	_	10	_	ns	9
Write pulse width	t _{wP}	8	_	10	_	ns	8
Address setup time	t _{AS}	0	_	0	_	ns	6
Write recovery time	t _{wr}	0	_	0	_	ns	7
Data to write time overlap	t _{DW}	6	_	7	_	ns	
Data hold from write time	t _{DH}	0	_	0	_	ns	
Write disable to output in low-Z	t _{ow}	3	_	3	_	ns	1
Output disable to output in high-Z	t _{OHZ}	_	6	_	7	ns	1
Write enable to output in high-Z	t _{wHZ}	_	6	_	7	ns	1

Note: 1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.

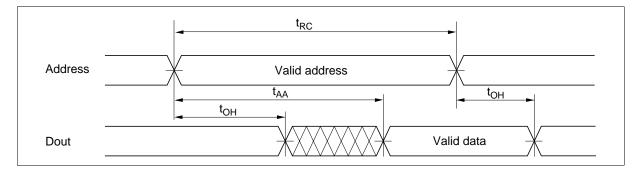
- 2. Address should be valid prior to or coincident with $\overline{\text{CS}}$ transition low.
- 3. WE and/or CS must be high during address transition time.
- 4. if $\overline{\text{CS}}$ and $\overline{\text{OE}}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
- 5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, output remains a high impedance state.
- 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
- 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
- 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- 9. t_{CW} is measured from the later of \overline{CS} going low to the end of write.

Timing Waveforms

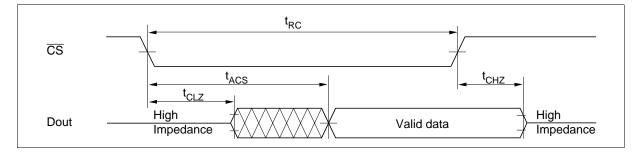
Read Timing Waveform (1) $(\overline{WE} = V_{IH})$



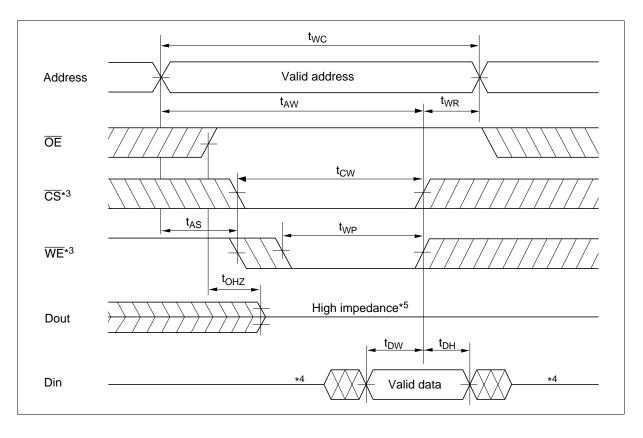
Read Timing Waveform (2) $(\overline{WE}=V_{IH},\overline{CS}=V_{IL},\overline{OE}=V_{IL})$



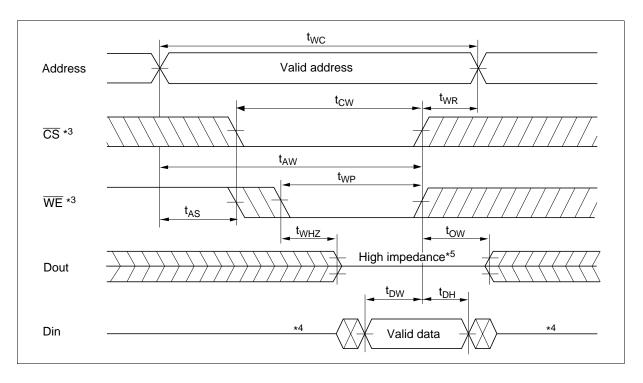
Read Timing Waveform (3) $(\overline{WE}=V_{IH},\overline{CS}=V_{IL},\overline{OE}=V_{IL})^{*2}$



Write Timing Waveform (1) ($\overline{\text{WE}}$ Controlled)

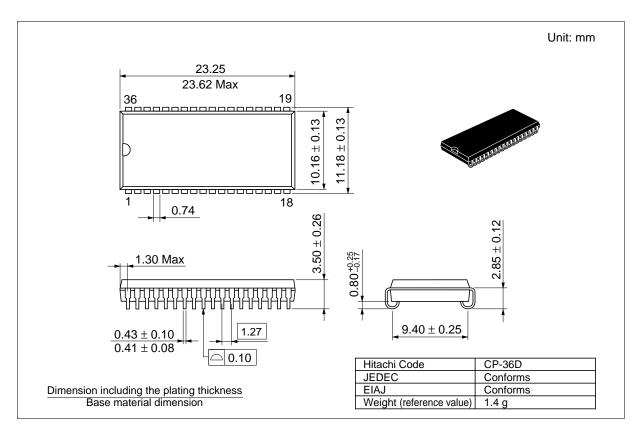


Write Timing Waveform (2) $(\overline{CS} \text{ Controlled})$



Package Dimensions

HM628511HJPI Series (CP-36D)



Cautions

- Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
- 2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
- 3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
- 4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
- 5. This product is not designed to be radiation resistant.
- 6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
- Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : http:semiconductor.hitachi.com/ Europe : http://www.hitachi-eu.com/hel/ecg

Asia (Singapore)
Asia (Taiwan)
Asia (HongKong)

: http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (HongKong)
: http://www.hitachi.com.tw/E/Product/SICD_Frame.htm

Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose,CA 95134 Tel: <1> (408) 433-1990 Fax: <1>(408) 433-0223 n write to:

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00
Hitachi Europe Ltd.

Electronic Components Group.

Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <4/4>, (1628), 585000

Berkshire SL6 8YA, United Kingdo Tel: <44> (1628) 585000 Fax: <44> (1628) 778322 Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533

Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong

Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX

Copyright © Hitachi, Ltd., 1998. All rights reserved. Printed in Japan.

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 15, 1999	Initial issue		_