
HM628512 Series

524288-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-236F (Z)

Rev. 6.0

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Description

The Hitachi HM628512 is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery backup system.

Features

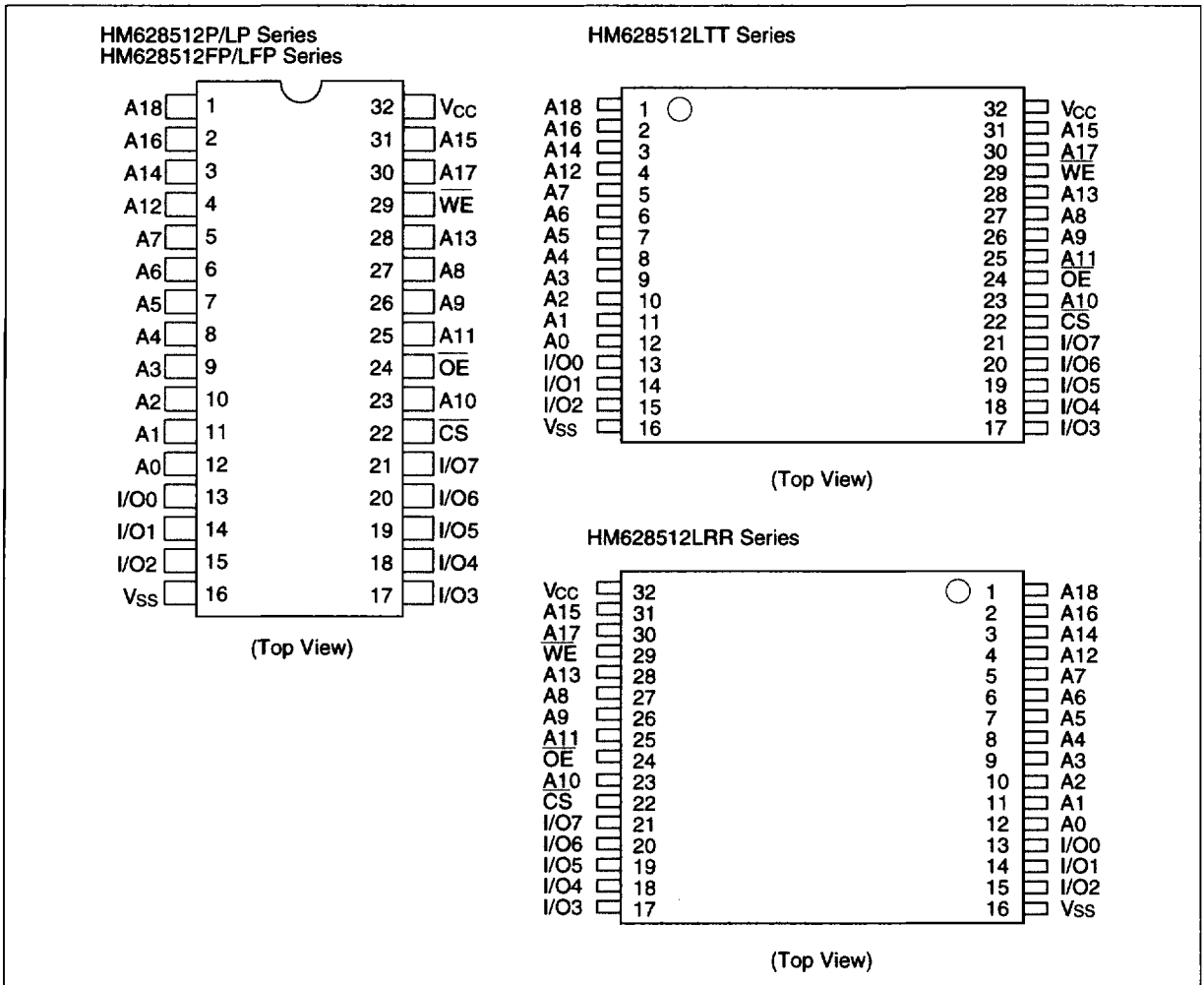
- High speed: Fast access time:
 - 55/65/70 ns (max)
- Low power
 - Standby: 10 μW (typ) (L/L-SL version)
 - Operation: 75 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery backup operation (L/L-SL version)

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Ordering Information

Type No.	Access Time	Package
HM628512P-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512P-7	70 ns	
HM628512LP-5	55 ns	
HM628512LP-7A	65 ns	
HM628512LP-7	70 ns	
HM628512LP-5SL	55 ns	
HM628512LP-7SL	70 ns	
HM628512FP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512FP-7	70 ns	
HM628512LFP-5	55 ns	
HM628512LFP-7A	65 ns	
HM628512LFP-7	70 ns	
HM628512LFP-5SL	55 ns	
HM628512LFP-7SL	70 ns	
HM628512LTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512LTT-7A	65 ns	
HM628512LTT-7	70 ns	
HM628512LTT-5SL	55 ns	
HM628512LTT-7SL	70 ns	
HM628512LRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512LRR-7A	65 ns	
HM628512LRR-7	70 ns	
HM628512LRR-5SL	55 ns	
HM628512LRR-7SL	70 ns	

Pin Arrangement

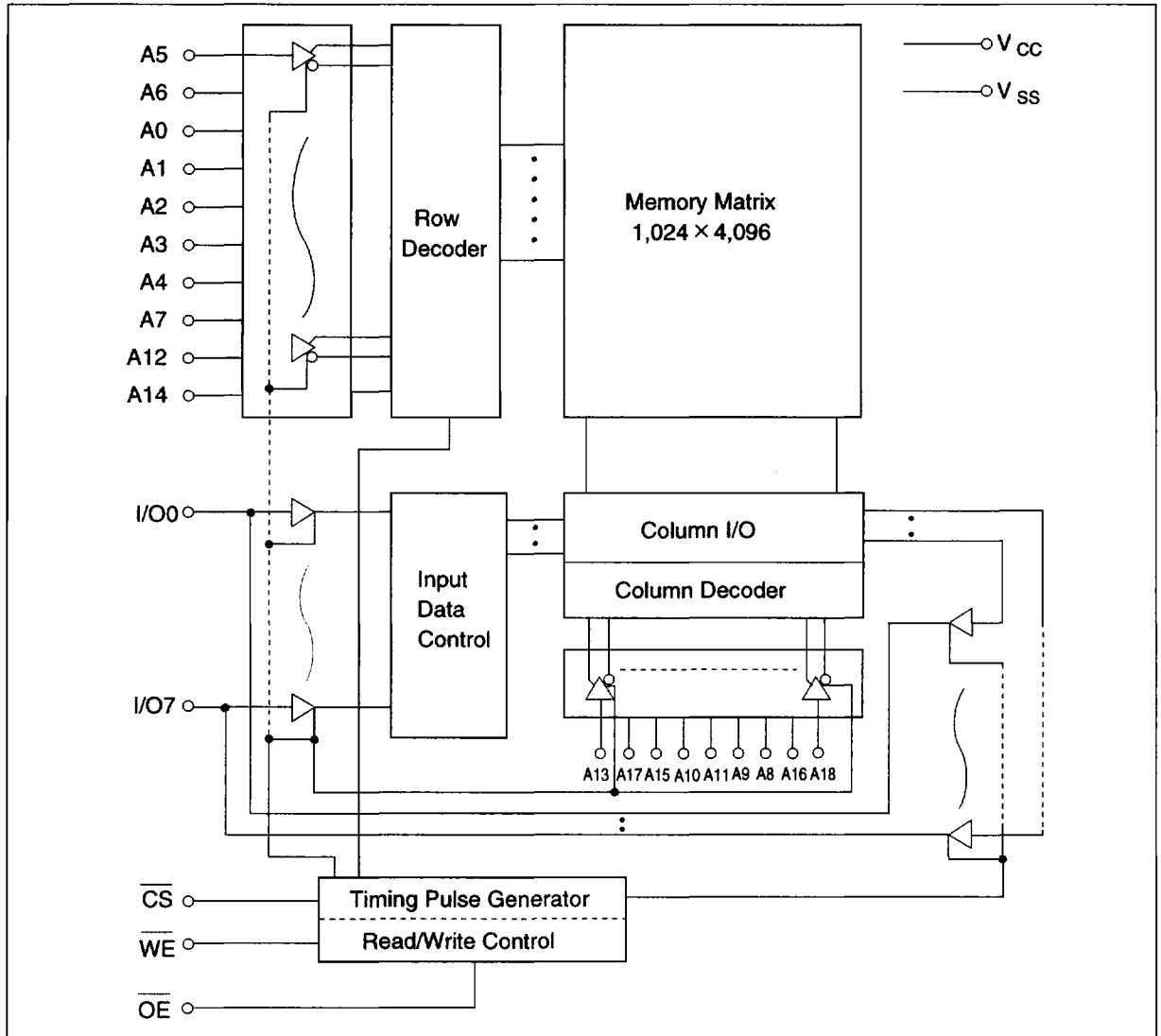


Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
V _{CC}	Power supply
V _{SS}	Ground

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Block Diagram



Function Table

\overline{WE}	\overline{CS}	\overline{OE}	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS} ¹	V_T	-0.5 ² to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. Relative to V_{SS} .

2. -3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	-0.3 ¹	—	0.8	V

Note: 1. -3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test Conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{VO} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC READ}	—	15	25	mA	$\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$ others = V _{IH} /V _{IL} , I _{VO} = 0 mA
	I _{CC WRITE}	—	20	45	mA	$\overline{CS} = V_{IL}$, $\overline{WE} = V_{IL}$ others = V _{IH} /V _{IL} , I _{VO} = 0 mA
Operating power supply current	-5/7A I _{CC1}	—	70	100	mA	Min cycle, duty = 100%
	-7 I _{CC1}	—	60	90	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{VO} = 0 mA
Operating power supply current	I _{CC2}	—	15	30	mA	Cycle time = 1 μs, duty = 100% I _{VO} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I _{SB1}	—	0.02	2	mA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2	100 ²	μA	
		—	2	50 ³	μA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test Conditions
Input capacitance ¹	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance ¹	C _{VO}	—	10	pF	V _{VO} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512-7A/7)
1 TTL Gate + C_L (50 pF) (HM628512-5)
(Including scope & jig)

Read Cycle

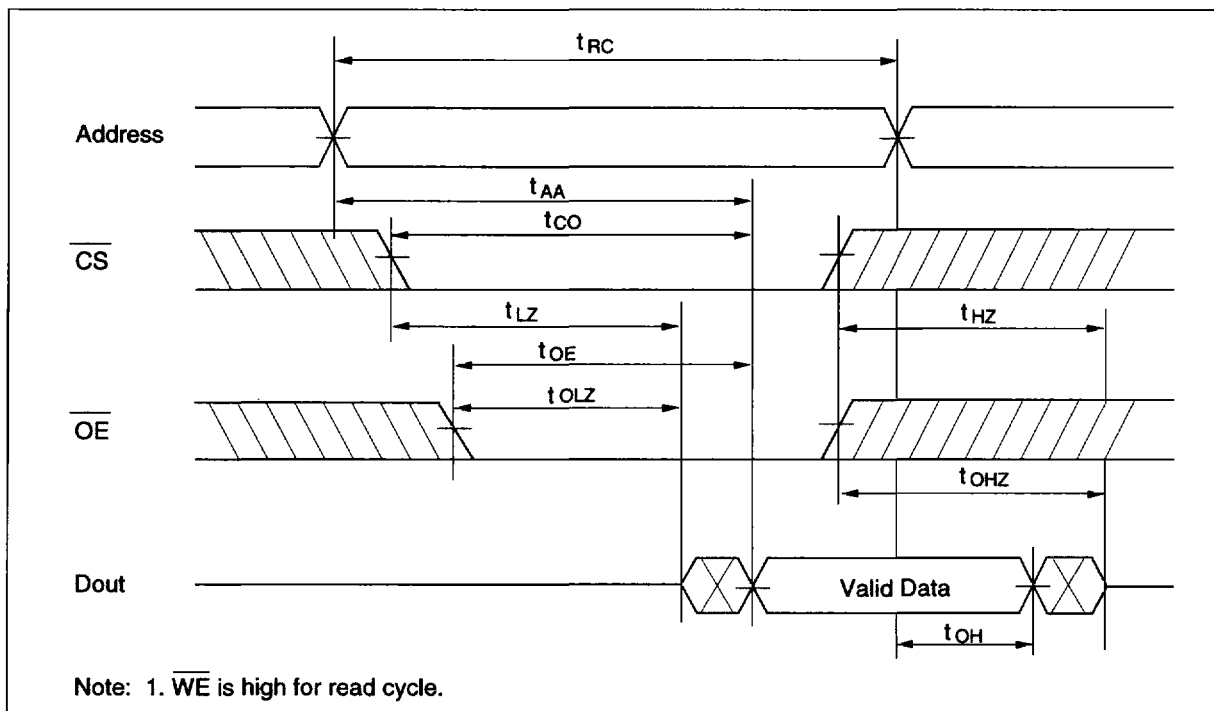
Parameter	Symbol	HM628512						Unit	Notes
		-5		-7A		-7			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	55	—	65	—	70	—	ns	
Address access time	t _{AA}	—	55	—	60	—	70	ns	
Chip select access time	t _{CO}	—	55	—	65	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	30	—	35	ns	
Chip selection to output in low-Z	t _{LZ}	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{HZ}	0	20	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns	

Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

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Read Timing Waveform^{*1}



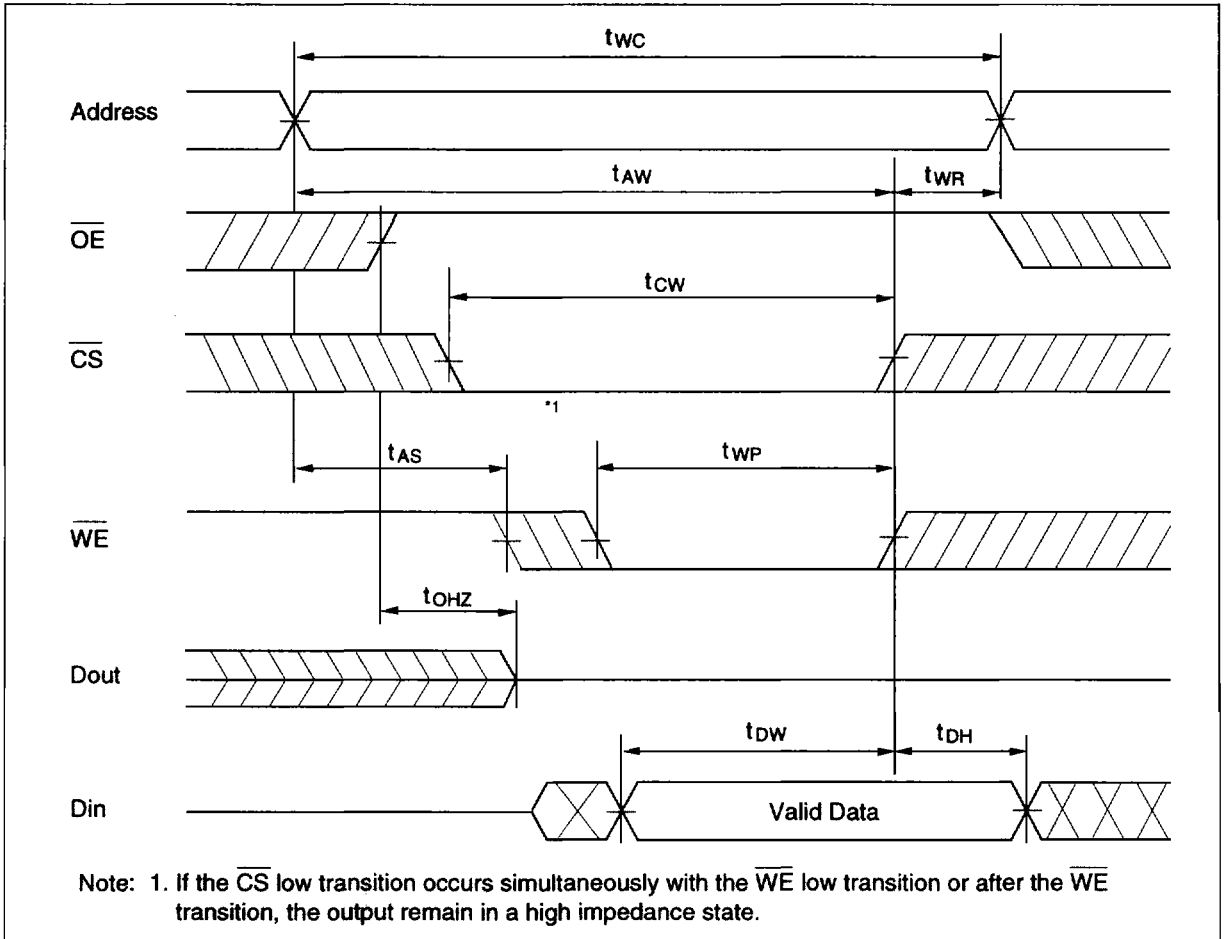
Write Cycle

Parameter	Symbol	HM628512						Unit	Notes
		-5		-7A		-7			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	55	—	70	—	ns	
Chip selection to end of write	t_{CW}	50	—	50	—	60	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	50	—	50	—	60	—	ns	
Write pulse width	t_{WP}	40	—	40	—	50	—	ns	1, 8
Write recovery time	t_{WR}	5	—	5	—	5	—	ns	4
\overline{WE} to output in high-Z	t_{WHZ}	0	20	0	20	0	25	ns	5, 6, 7
Data to write time overlap	t_{DW}	25	—	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	5	—	ns	6
Output disable to output in high-Z	t_{OHZ}	0	20	0	20	0	25	ns	5, 6

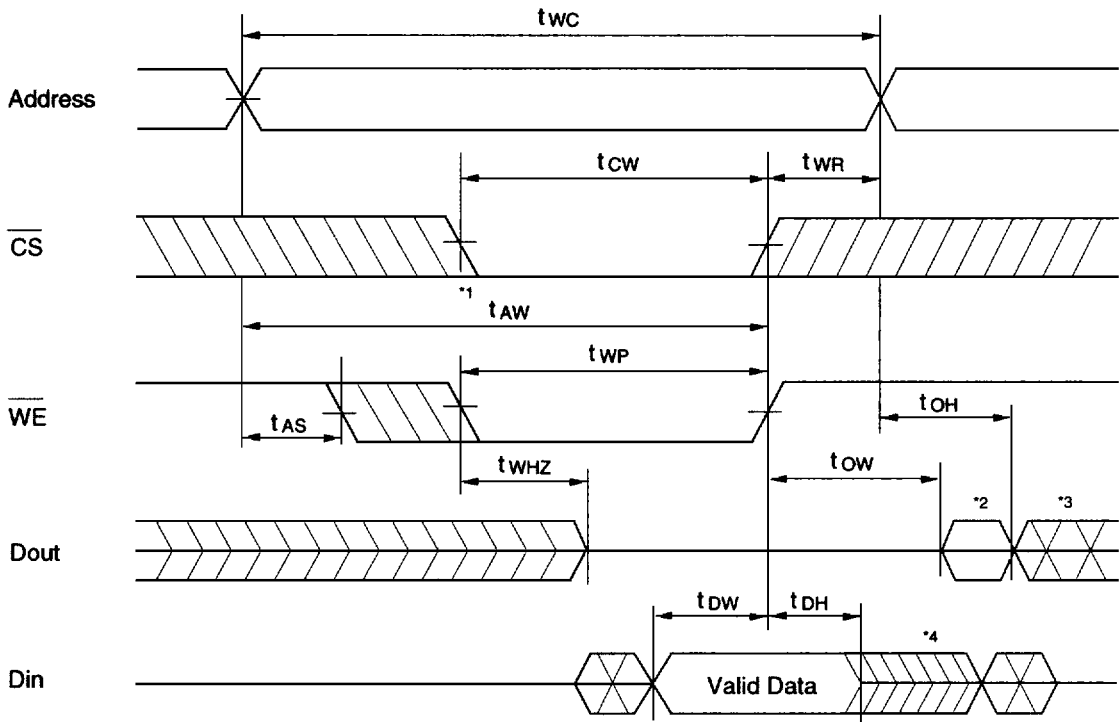
- Notes:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from \overline{CS} going low to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.
 5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 6. This parameter is sampled and not 100% tested.
 7. t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referred to output voltage levels.
 8. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

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Write Timing Waveform (1) (\overline{OE} Clock)



Write Timing Waveform (2) (\overline{OE} Low Fixed)



- Notes:
1. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output remain in a high impedance state.
 2. D_{out} is the same phase of the write data of this write cycle.
 3. D_{out} is the read data of next address.
 4. If \overline{CS} is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions ³
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	1^4	50^1	μA	$V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$
		—	1^4	15^2	μA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Notes: 1. For L-version and $20 \mu\text{A}$ (max.) at $T_a = 0$ to 40°C .

2. For SL-version and $3 \mu\text{A}$ (max.) at $T_a = 0$ to 40°C .

3. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and D_{in} buffer. In data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

4. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = 25^\circ\text{C}$ and specified loading, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)

