USER'S MANUAL May 1999 File Number 3367.3

HSP45116 Daughter Board

The HSP45116-DB is a daughter board designed to mate with the HSP-EVAL for rapid evaluation and prototyping of the HSP45116 Numerically Controlled Oscillator Modulator. Together, the board set provides a mechanism to evaluate HSP45116 operation using IBM PC™ based I/O and control. As shown in Figure 1, the HSP45116-DB maps the input, output, and control signals of the HSP45116 to three 50 pin headers. These headers mate with connectors on board the HSP-EVAL to interface the HSP45116's various I/O and control signals with the HSP-EVAL's data busses. This interface establishes a path for PC™ based I/O and control of the HSP45116-DB via the HSP-EVAL.

An IBM PC™ based software package is supplied which controls operation to the HSP45116-DB/HSP-EVAL board set. The software package provides the user with a DOS command line interface and graphical user interface for daughter board I/O and control. Since the software supports data acquisition from the HSP45116, software based signal analysis may be used to quantify part performance.

The degree of control exerted by the software varies depending upon the clock supplied to the HSP45116-DB. If a high speed clock is supplied via the HSP-EVAL's on board oscillator or external clock pin, the software can be used to exert real time control. If a software controlled clock is provided, the HSP45116-DB can be driven with a user defined data set, while storing results back to the PC for later analysis.

The HSP45116-DB is a 6 layer printed circuit board which comes populated with one HSP45116GC-25. The PC based software required to control the daughter board via the HSP-EVAL is also provided.

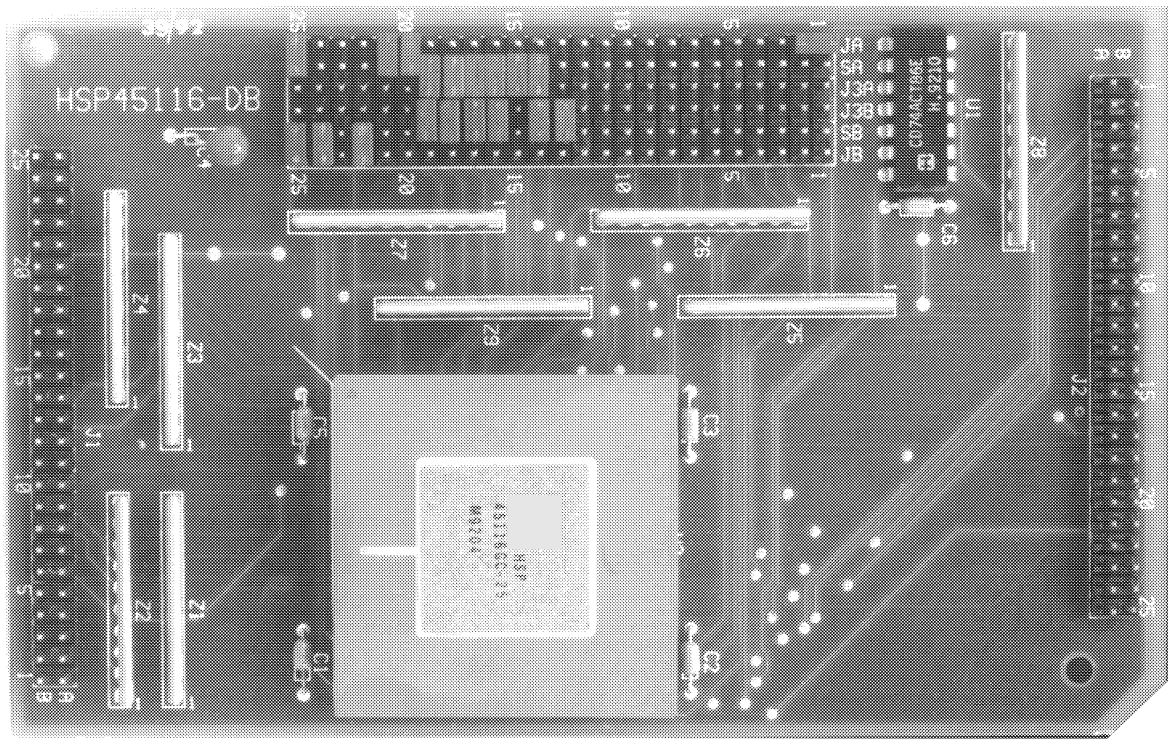
Features

- Designed for Use with HSP-EVAL
- Access to HSP45116s Input, Output, and Control Signals Through Three 50 Pin Headers
- HSP45116 Control Signal States May be Set Through Hardware Configuration or Software
- Two Separate Software Packages for Daughter Board I/O and Control
- High Speed I/O Supported

Applications

- PC Based Performance Analysis of HSP45116 When Used with HSP-EVAL

HSP45116 Daughter Board



Getting Started

This section describes the initial evaluation system setup for the HSP45116-DB and HSP-EVAL board set. The system setup consists of mother/daughter board assembly, software installation, and system test to verify proper operation of the board set.

Assembly

The evaluation board set is assembled by mating the HSP45116-DB daughter board with the HSP-EVAL motherboard. This is accomplished by inserting the header pins sticking through the bottom (solder side) of the daughter board into the three 2 x 25 pin connectors on the motherboard. Proper alignment requires that the J1, J2, and J3 headers on the HSP45116-DB mate with the J1, J2, and J3 connectors on the HSP-EVAL. A moderate amount of force is required to seat the header pins in the motherboard connectors.

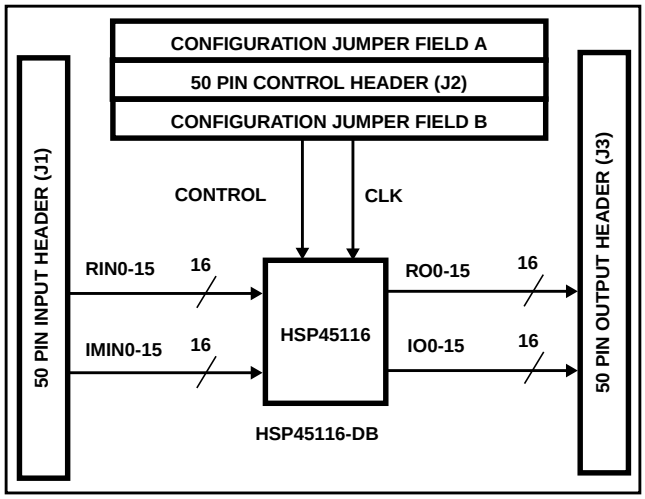


FIGURE 1. HSP45116-DB BLOCK DIAGRAM

As part of the initial assembly, the HSP-EVAL and HSP45116-DB must be provided with the default jumper configuration to ensure proper operation with the system test software. Each board leaving the factory is supplied with the default configuration, but the respective configurations are examined here for completeness. The motherboard's default configuration is realized by inserting jumpers into the HSP EVAL's J4 jumper field as shown in Figure 2 (see the HSP-EVAL User's Manual for more detailed information). The default configuration for the HSP45116-DB requires jumper placement across the Configuration Jumper Fields A and B and the J3 Control Header as shown in Table 1.

Before using the board set with the supplied software, power must be supplied to the boards, and the HSP-EVAL must be connected to the parallel port of the target PC. Power is provided to the boards by connecting the V_{CC} and GND pins of the J6 header on the HSP-EVAL to a standard 5V ±5% supply. As an alternative, power may be supplied through the HSP-EVAL's 96-Pin DIN connectors. The HSP-EVAL is connected to the target PC by connecting the HSP-EVAL's 26-PIN shrouded header to the PC's parallel port using the supplied ribbon cable.

System Requirements for the Evaluation Board Software

The PC system targeted to run the HSP45116-DB software (NCOM-SOFT) and interface with the evaluation board set must meet the following requirements:

- IBM PC/XT/AT, PS/2, or 100% compatible with a minimum of 640K of random access memory (RAM) (NCOM-SOFT does not require extended memory)
- At least 200kB of free disk space on your hard disk
- DOS Version 3.0 or higher
- One parallel port with 27 Pin D-Sub connector

Software Installation

The distribution diskette contains a program called INSTALL.EXE which installs the NCOM-SOFT software onto the target hard disk. ***Note: The steps in this section assume you are installing NCOM-SOFT from a diskette in drive A: onto a hard drive C:. If a different configuration is used, substitute the letter of the drive where the diskette is located for drive A;. Substitute the letter for the hard drive for drive C:***

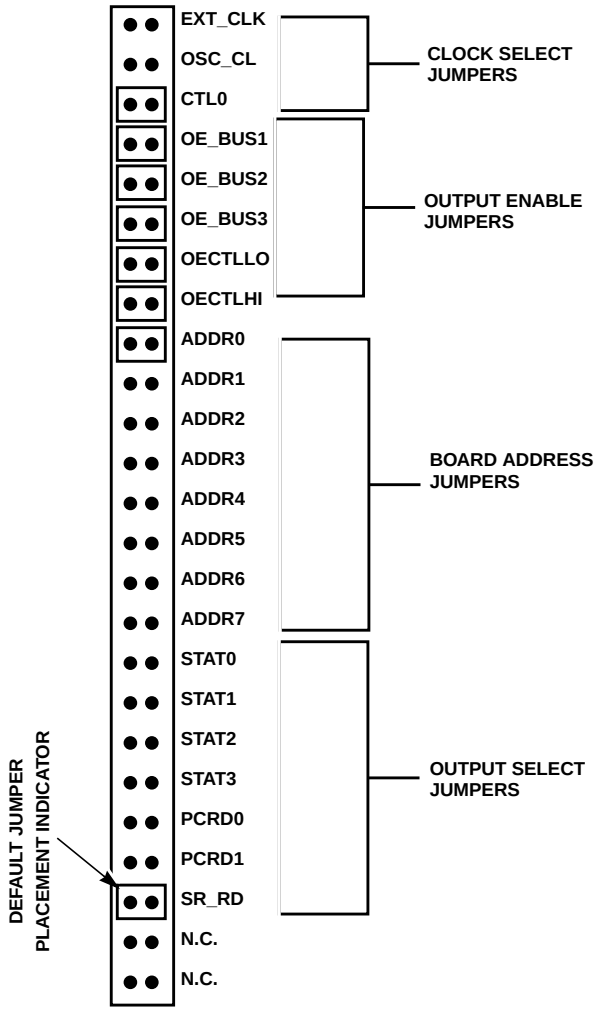


FIGURE 2. CONFIGURATION JUMPER FIELD J4

TABLE 1. OVERLAY OF DEFAULT JUMPER CONFIGURATION ONTO THE SIGNAL MAPPING FOR THE J3 CONTROL HEARDER AND THE CONFIGURATION JUMPER FIELDS A AND B

PIN NUMBER	JA SIGNAL MNEMONIC	SA SIGNAL MNEMONIC	J3A SIGNAL MNEMONIC	J3B SIGNAL MNEMONIC	SB SIGNAL MNEMONIC	JB SIGNAL MNEMONIC	PIN NUMBER
1	CLKOUT	BUF_IN	N.C.	GND	N.C.	GND	1
2	BUF_OUT	CLK_IN	C0	C1	N.C.	GND	2
3	GND	PULL UP	C2	C3	N.C.	GND	3
4	GND	PULL UP	C4	C5	N.C.	GND	4
5	GND	N.C.	C6	C7	N.C.	GND	5
6	GND	N.C.	GND	C8	N.C.	GND	6
7	GND	N.C.	C9	C10	N.C.	GND	7
8	GND	N.C.	C11	C12	N.C.	GND	8
9	GND	N.C.	C13	C14	N.C.	GND	9
10	GND	N.C.	C15	GND	N.C.	GND	10
11	GND	N.C.	N.C.	N.C.	N.C.	GND	11
12	GND	N.C.	CTL1	CT2	N.C.	GND	12
13	GND	PULL UP	CTL3	CTL4	$\overline{\text{ENPHREG}}$	GND	13
14	GND	$\overline{\text{ENTIREG}}$	CTL5	CTL6	$\overline{\text{ENOFREG}}$	GND	14
15	GND	$\overline{\text{ENI}}$	CTL7	GND	N.C.	GND	15
16	GND	$\overline{\text{CLROFR}}$	CTL8	CTL9	$\overline{\text{ENCFREG}}$	GND	16
17	GND	$\overline{\text{LOAD}}$	CTL10	CTL11	$\overline{\text{BINFMT}}$	GND	17
18	GND	PMSEL	CTL12	CTL13	AD0	GND	18
19	GND	AD1	CTL14	CTL15	$\overline{\text{WR}}$	GND	19
20	GND	MUX0	GND	N.C.	N.C.	GND	20
21	GND	MUX1	GND	N.C.	N.C.	GND	21
22	GND	$\overline{\text{PACI}}$	GND	N.C.	ACC	GND	22
23	GND	$\overline{\text{PEAK}}$	GND	N.C.	N.C.	GND	23
24	GND	$\overline{\text{RBYTILD}}$	GND	N.C.	MOD0	GND	24
25	GND	$\overline{\text{MODPI/2PI}}$	GND	N.C.	MOD1	GND	25

JUMPER CONFIGURATION FIELD A — **J3 CONTROL HEADER** — **JUMPER CONFIGURATION FIELD B**

To start the installation program:

Make sure computer is on and the DOS prompt is displayed.

Type: C:<Enter>

Create a subdirectory to contain the NCOM-SOFT Programs by typing:

MD \NCOMSOFT <Enter>

Change current directory to the NCOMSOFT directory:

CD \NCOMSOFT <Enter>

Start the installation process by typing:

A:INSTALL <Enter>

The INSTALL program downloads the NCOM-SOFT programs, NCOMCTRL and NCOM_CMD, to the NCOMSOFT subdirectory on the target hard drive. In addition, a subdirectory called NCOM_CHK is created into which files used to perform functional verification are downloaded.

Modifications to AUTOEXEC.BAT

To run the NCOM-SOFT programs, DOS must be able to find the executable files. To ensure that DOS can always find the NCOM-SOFT executables, modify the search path to include the location of the NCOM-SOFT directory. For example, if the NCOM-SOFT programs are installed on drive C: in a subdirectory called \NCOMSOFT, add the following

line to the end of the existing Path command in the AUTOEXEC.BAT file:

;C:\NCOMSOFT

If your AUTOEXEC.BAT file does not contain a PATH command, add the following command to the file:

PATH=C:\NCOMSOFT

Reboot the PC so that the search path changes will take effect.

System Test

Test software is provided to verify operation of the HSP-EVAL and HSP45116-DB board set. Prior to performing the system test, it is assumed that the evaluation board set has been assembled and configured as described above; power has been applied to the board set, and the 26-Pin shrouded header on board the HSP-EVAL has been connected to the parallel port of the target PC via the supplied cable. The system test is initiated by the following:

Change the current directory to that which contains the software required for the system test by typing

CD C:\NCOMSOFT\NCOM_CHK <Enter>

Run the system test software by typing:

NCOM_CHK <Enter>

The NCOM_CHK.BAT batch file makes use of the Command Line Interface (see Command Line Interface Section) to initialize the evaluation board set; clock a data vector through the HSP45116-DB, and store the output to a file. The output file is then compared, using the DOS command COMP, to a file containing a set of vectors generated by a properly functioning board set. If the files match, the assembled board set passes operational verification. ***NOTE: the user should answer NO to the COMP command prompt to compare additional files.***

The NCOM_CHK system test assumes that the LPT1 printer port is being used for communication with the HSP-EVAL. If another printer port is used, the Command Line Interface, NCOM_CMD, must be used to configure the software for using the other port (see NCOM_CMD's PC and P# command).

HSP45116-DB Control Panel Software

The HSP45116-DB Control Panel is a graphical user interface for controlling the operation of the HSP-EVAL/HSP45116-DB Board Set via an IBM PC or compatible. The control panel, as shown in Figure 3, supports loading the HSP45116's frequency, phase, and timer accumulator configuration registers, as well as setting the state of various control inputs. In addition, the control panel is used to specify files which serve as a data source for the HSP45116's RIN0-15 and IMIN0-15 inputs and a data sink for the RO0-15 and IO0-15 outputs. Operation of the control panel software is dependent on the clock source provided to the HSP45116-DB as specified in the clock select portion of the control panel. The HSP45116-DB Control Panel is invoked by typing:

NCOMCTRL <Enter>

Port Configuration

Communication between the Control Panel software and the evaluation board set requires that the software knows which of the PC's parallel ports is being used for communication with the HSP-EVAL and which board address the HSP-EVAL has been configured for. The default configuration assumes that LPT1 is being used and the HSP-EVAL has been configured for a board address of 0. The Port Configuration can be inspected by opening up the port configuration window using the F9 function key. As shown in Figure 4, the window displays the available parallel ports and their addresses. Also displayed are the current port and HSP-EVAL Board address being used by the Control Panel software.

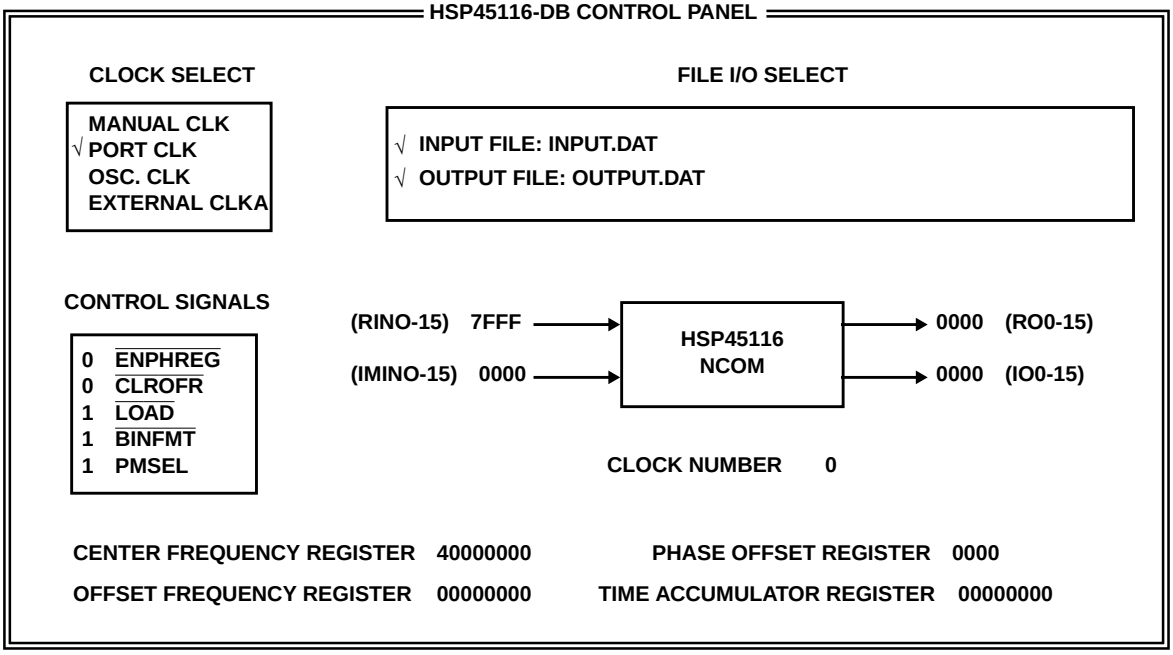


FIGURE 3. CONTROL PANEL SCREEN AS DISPLAYED ON PC

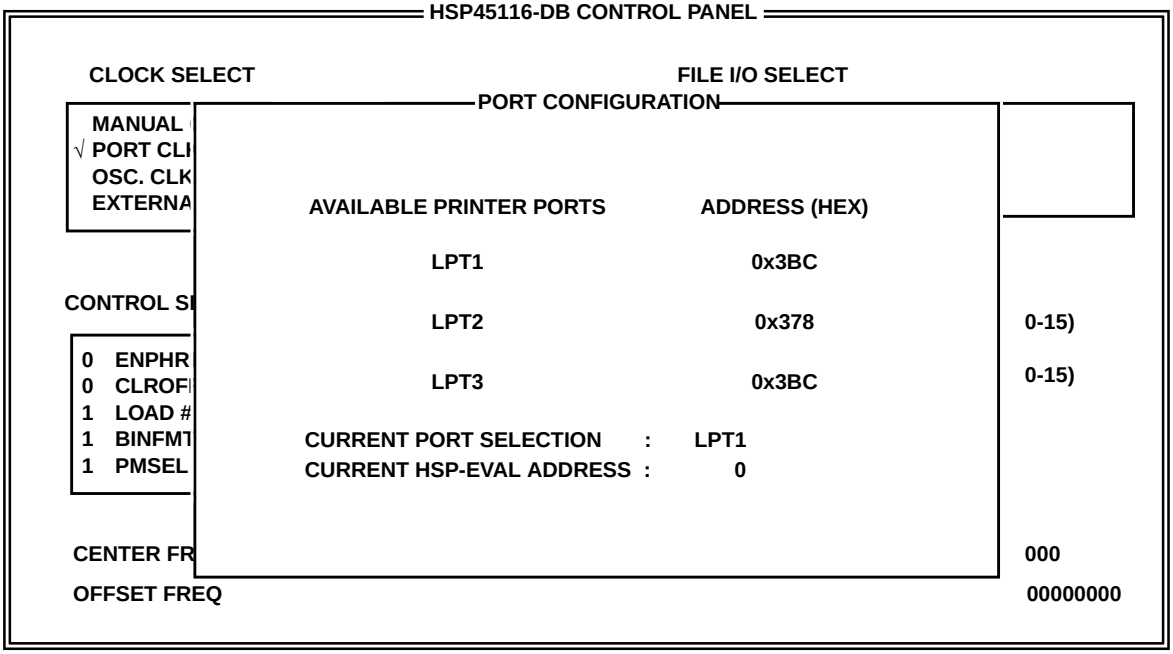


FIGURE 4. PORT CONFIGURATION WINDOW AS DISPLAYED ON PC

The current port and HSP-EVAL address are changed by opening up the Port Configuration Window, using the up/down arrow keys to select the desired parameter, and toggling the space bar to change the selection. Proper operation of the control panel software requires that the HSP-EVAL Board address specified in the port configuration window matches the address jumpered in the Address Selection Section of the HSP-EVAL's J4 jumper field (see HSP-EVAL User's Manual).

Clock Select

The Clock Select portion of the control panel is used to tell the Control Panel software which of four different clock sources is being supplied to the HSP45116-DB. The choices include one of two different software generated clocks (Manual CLK or Port CLK), an oscillator clock provided by the HSP-EVAL (OSC. CLK), or an externally supplied clock (External CLK). The clock mode selected must be consistent with the Clock Select jumper position in the HSP-EVAL's J4 jumper field. If either Manual CLK or Port CLK are specified in the Control Panel, the clock select jumper must be inserted in the CTL0 position. If either OSC. CLK or External CLK is specified, the jumper must be inserted at the OSC_CLK or EXT_CLK position respectively.

In Manual CLK mode, single clock pulses are sent to the HSP45116 by depressing the F2 function key. The clock pulse is software generated by setting and clearing the CTL0 bit of the CTL Control Register on the HSP-EVAL. After each clock, the HSP45116-DB's RO0-15 and IO0-15 outputs are serialized and read into the PC for display in the Control Panel. In this mode, file input and output is supported (see File I/O Select Section).

In Port CLK mode, a free running clock is sent to the HSP45116 by depressing the F2 function key. The clock pulses are software generated by continually setting and clearing the CTL0 bit of the CTL0-15 Register on the HSP-EVAL. After each clock the HSP45116-DB's RO0-15 and IO0-15 outputs are serialized and read into the PC for display in the Control Panel. In this mode, file input and output is supported (See File I/O Select Section).

In OSC. CLK mode, the HSP45116 is supplied with a clock by the oscillator on-board the HSP-EVAL. In this mode, the Control Panel can be used for modifying the various control signal states, the configuration registers, and the complex inputs to the NCOM. However, the software is unable to provide file based I/O to the evaluation board set since the data rate required by the oscillator clock is orders of magnitude greater than that possible through the parallel port of the PC. As a result, the Control Panel disables file based I/O and the display of NCOM output in this mode.

In External CLK mode, the HSP45116 is supplied with a clock through the 96-Pin DIN connector P1 on the HSP-EVAL. In this mode, the Control Panel can be used for modifying control signal states, the various configuration registers, and the complex inputs to the NCOM. However, the software does not support file based I/O to the evaluation board set since the data rate required may be much greater than that capable through the parallel port of the PC. In this mode, the Control Panel disables file based I/O and the display of NCOM output.

The clocking mode used by the control panel is indicated by the position of the "check mark" symbol within the Clock Select portion of the Control Panel. A different clocking mode may be selected by positioning the "check mark" symbol in front of the desired clocking mode. The position of the "check mark" is changed by using the cursor keys to move the active window to the desired position and then toggling the space bar to move the "check mark".

File I/O Select

The File I/O Select portion of the Control Panel allows the user to specify files which can be used as an input data source or an output data sink for the HSP45116-DB. If file based input is selected, Control Panel software down loads data from the specified file to registers on the HSP-EVAL and clocks the data into the RIN0-15 and IMIN0-15 inputs of the HSP45116. If file based output is specified, the software reads the data on the RO0-15 and IO0-15 outputs of the HSP45116 via the HSP-EVAL's output shift register and stores the data in the specified file. The input data is loaded on to the input busses prior to the software generated clock and the output data is read from the output busses following the software generated clock.

File based I/O is activated by using the space bar to toggle the "check mark" symbol in the window proceeding the Input and Output File identifier in the Control Panel's File I/O Section. If either file input or output is activated, the respective file name must be entered in the window to the right of the I/O file identifier. File input or output may be disabled at any time by toggling the respective "check mark". ***Note: file I/O is only valid when either the 'Manual CLK' or 'Port CLK' clocking modes are selected and it is disabled if other clocking modes are specified.***

The input and output data files are ASCII based and have a format as described in Appendix A. There is no limitation to the input and output file size, and care must be taken if file output is specified since data is collected in the file until file output is deactivated or the NCOMCTRL Program is exited.

HSP45116 Complex Data Inputs

The data windows to the left of the HSP45116 icon are used to specify hexadecimal values which drive the part's complex inputs, RIN0-15 and IMIN0-15. Data entered into these windows is down loaded to registers on the HSP-EVAL which drive the HSP45116-DB's complex input busses. ***Note: Jumpers must be inserted into the OE_BUS1 and OE_BUS2 positions of the HSP-EVAL's J4 jumper field to enable the register outputs containing the complex data.***

The complex inputs may be changed by entering hexadecimal values into the data windows. The contents of a particular data window may be edited by depressing the <Enter> key and using the arrow keys to position the cursor on the hexadecimal character to be modified.

If file input is selected, the complex inputs are driven with data from the specified file. On each clock the data windows are updated with the complex sample down loaded from the file. In this mode the complex input data windows may not be manually updated.

Control Signals

The Control Signal portion of the control panel is used to define the state of various control signal inputs to the HSP45116. The logical state of a control signal is set by using the space bar to toggle the signal state in the window preceding the specified control signal. For the control signal states displayed in the Control Panel to be active at the HSP45116, the respective control signals must be jumpered to the HSPEVAL's CTL0-15 Bus via the HSP45116-DB's J3 jumper field as shown in the default jumper configuration displayed in Table 1 (see Jumper Configuration Section). The Control Signal descriptions are contained in the HSP45116 Data Sheet.

Configuration Registers

The bottom of the control panel displays four data windows which contain the hexadecimal values loaded into the HSP45116's Center Frequency, Offset Frequency, Phase Offset, and Time Accumulator Registers. The contents of a particular configuration register may be updated by entering a new hexadecimal value into the data window. The current value in a window may also be edited by depressing the <Enter> key and using the arrow keys to position the cursor on the hexadecimal character to be modified.

The value entered into the data window is down loaded to the HSP45116 after leaving the window via the arrow keys or terminating an edit by the <Enter> key. If the data window is associated with the Phase Offset Register, the 16-Bit hexadecimal value is down loaded into the HSP45116's Phase Input Register. If the data window is one of the three 32-bit windows associated with the Center Frequency, Offset Frequency, of Timer Accumulator Registers, the 32-bit value is loaded into the HSP45116's MS and LS Input Registers and either $\overline{\text{ENCFREG}}$, $\overline{\text{ENOFREG}}$, or $\overline{\text{ENTIREG}}$ is asserted respectively. Then, the enable signal is de-asserted and registered on chip by another software generated clock. In either Manual or Port Clock modes, a PC generated clock is issued to ensure that the corresponding enable signal is registered on chip (see HSP45116 Data Sheet). In either of the other two clock modes, it is assumed that the clock rate is high enough to register the enable signal before another Configuration Register is updated. For proper operation, the register enables, $\overline{\text{WR}}$, and A0-1 inputs must be jumpered to the HSP-EVAL's control bus and inputs via the J3 Control Header as shown in the Default Jumper Configuration (Table 1).

Help

Help windows are provided as a source of information for control panel usage. The help window is activated by the F1 function key, and contains information based on the current active data window.

Command Line Interface

As an alternative to the control panel, a command line interface is provided which allows the user to control the HSP45116-DB by issuing commands from the DOS prompt. The commands perform basic I/O and configuration functions by up or down loading data to the HSP45116 through the HSP-EVAL. The Command Line program has the following usage:

NCOM_CMD [Command] [ARG 1] [ARG 2]

TABLE 2. COMMAND LIST FOR COMMAND LINE INTERFACE SOFTWARE

COMMAND	ARGUMENT #1	ARGUMENT #2	COMMAND DESCRIPTION
CF	32-BIT HEXADECIMAL VALUE		Loads HSP45116's Center Frequency Register with hexadecimal value specified in Argument #1. See Notes 1 and 2.
OF	32-BIT HEXADECIMAL VALUE		Loads HSP45116's Offset Frequency Register with hexadecimal value specified in Argument #1. See Notes 1 and 2.
TI	32-BIT HEXADECIMAL VALUE		Loads HSP45116's Time Accumulator Register with hexadecimal value specified in Argument #1. See Notes 1 and 2.
PO	16-BIT HEXADECIMAL VALUE		Loads HSP45116's Phase Input Register with hexadecimal value specified in Argument #1. See Note 2.
CL	16-BIT HEXADECIMAL VALUE		Loads the HSP-EVAL's CTL Control Register with the 16-bit value specified in Argument #1.
RI	16-BIT HEXADECIMAL VALUE		Loads the specified Hex value into the HSP-EVAL Register (Input Register #2) driving the Real Input bus (RIN0-15) Of The HSP45116-DB. See Note 3.
II	16-BIT HEXADECIMAL VALUE		Loads The Specified Hex Value Into The HSP-EVAL Register (Input Register #1) driving the imaginary Input Bus (IMIN0-15) Of The HSP45116-DB. See Note 3.

TABLE 2. COMMAND LIST FOR COMMAND LINE INTERFACE SOFTWARE (Continued)

COMMAND	ARGUMENT #1	ARGUMENT #2	COMMAND DESCRIPTION
PF	INPUT FILE	OUTPUT FILE	Down loads complex samples stored in the file specified by Argument #1 into the HSP-EVAL Registers driving the Real and Imaginary Input Buses of the HSP45116-DB, clocks the data into the part, and stores the complex output to the file specified by Argument #2. The input and output file formats are specified in Appendix A. See Notes 3, 4 and 5.
CK			Issues software generated clock pulse to HSP45116-DB by toggling the CTL0 bit in the HSP-EVAL's CTL0-15 Register. See Note 4.
RD			Reads data on the HSP45116-DB's RO0-15 and IO0-15 outputs and prints data to screen. See Note 4 and 5.
SM			Displays signal mapping between the CTL Control Register and the HSP45116 control inputs (assumes default jumper configuration shown in Table 1).
CR			Displays current state of CTL Control Register.
PC			Displays the printer port and HSP-EVAL board address that the NCOM_CMD program is using for communication between the PC and the HSP-EVAL. The HSP-EVAL board address is set by inserting a jumper in the ADDR0-7 positions of it's J4 Jumper Field.
P#	PORT NUMBER (1-3)	BOARD ADDRESS (0-7)	Change The Printer Port And HSP-EVAL Board Address that the NCOM_CMD Program is using for communication between the PC and the HSP-EVAL to those specified in Arguments 1 and 2. The HSP-EVAL Board Address is set by inserting a Jumper in the ADDR0-7 positions of it's J4 Jumper Field.
?			List available commands together with a brief description.

NOTES:

1. The CF, OF, TI commands load the specified 32-bit value into the HSP45116's MS and LS input registers. After the configuration data has been loaded into the MS and LS Registers, the corresponding enable, $\overline{\text{ENCFREG}}$, $\overline{\text{ENOFREG}}$, or $\overline{\text{ENTIREG}}$ is asserted. The enable signal is then registered on chip by a single software generated clock provided a jumper is inserted at the CTL0 position of the J4 jumper field on the HSP-EVAL. Otherwise, it is assumed that the selected clock source is fast enough to register the enable signal prior to a subsequent load of one of another 32-bit configuration register. The register enables, $\overline{\text{ENCFREG}}$, $\overline{\text{ENOFREG}}$, and $\overline{\text{ENTIREG}}$ must be jumpered to the CTL Control Bus as in the default configuration shown in Table 1.
2. When commands are issued to load registers internal to the HSP45116, it is assumed that the microprocessor interface signals, $\overline{\text{WR}}$ and A0-1 are jumpered to the CTL0-15 bus as in the default configuration shown in Table 1.
3. If the complex input buses of the HSP45116-DB are to be driven by the HSP-EVAL's Input Registers 1 and 2, their outputs must be enabled by placing jumpers in the OE_BUS1 and OE_BUS2 positions of the J4 jumper field on the HSP-EVAL.
4. This command is only valid if a software generated clock source has been selected by inserting a jumper in the CTL0 position of the HSP-EVAL's J4 jumper field.
5. Commands required to read data on the HSP45116-DB's complex outputs only function properly if the output of the shift register is selected for reading by inserting a jumper in the SR_RD position of the HSP-EVAL's J4 jumper field.

The Command specifies 1 of 14 actions to be taken, and the Arguments (ARG1, ARG2) represent additional data required by the command. For example, the HSP45116's Center Frequency Register would be loaded with a value of 40000000(HEX) by typing:

NCOM_CMD CF 40000000 <Enter>

A summary of the command set is contained in Table 2.

Proper operation of the Command Line software is ensured if the default jumper configurations for the HSP45116-DB and the HSP-EVAL shown in Table 1 and Figure 2 are used. However, modifications to this configuration may be required depending on the clock source and the mode of operation.

The Command Line Interface gives the user the ability to control the evaluation board set via DOS batch files or system calls from a programming language. The NCOM_CHK.BAT file discussed in the System Test Section is an example of how the Command Line program might be used in a DOS batch file.

Signal Headers

The HSP45116-DB maps the NCOM's inputs and outputs to three 50-pin signal headers, J1-J3. The signal headers are used to connect the NCOM's I/O and control pins to the HSP-EVAL's I/O and control busses through three 50 position connectors. The Control Panel and Command Line interface software control the operation of the HSP45116-DB by up or down loading data to registers on-board the HSP-EVAL which drive or monitor the I/O and control busses.

The J1 Input Header maps two 16-bit busses to the real and imaginary inputs of the HSP45116, RIN0-15 and IMIN0-15. In addition, a bidirectional clock line is routed to this header as shown by the signal map in Table 3. When mated with the J1 connector on the HSP-EVAL, the HSP45116's real and imaginary inputs map to the HSP-EVAL's Input Bus 2 and 1, IN2_0-15 and IN1_0-15, respectively.

TABLE 3. SIGNAL ASSIGNMENTS FOR 50 POSITION INPUT CONNECTOR J1

PIN NUMBER	J1A SIGNAL MNEMONIC	J1B SIGNAL MNEMONIC
1	N.C.	GND
2	RIN0	RIN1
3	RIN2	RIN3
4	RIN4	RIN5
5	RIN6	RIN7
6	GND	RIN8
7	RIN9	RIN10
8	RIN11	RIN12
9	RIN134	RIN14
10	RIN15	GND
11	N.C.	IMIN0
12	IMIN1	IMIN2
13	IMIN3	IMIN4
14	IMIN5	IMIN6
15	IMIN7	GND
16	IMIN8	IMIN9
17	IMIN10	IMIN11
18	IMIN12	IMIN13
19	IMIN14	IMIN15
20	GND	CLKIN
21	GND	N.C.
22	GND	V_{CC}
23	GND	V_{CC}
24	GND	V_{CC}
25	GND	V_{CC}

TABLE 4. SIGNAL ASSIGNMENTS FOR 50 POSITION OUTPUT CONNECTOR J2

PIN NUMBER	J2A SIGNAL MNEMONIC	J2B SIGNAL MNEMONIC
1	OER	GND
2	RO0	RO1
3	RO2	RO3
4	RO4	RO5
5	RO6	RO7
6	GND	RO8
7	RO9	RO10
8	RO11	RO12
9	RO13	RO14
10	RO15	GND
11	OEI	IO0
12	IO1	IO2
13	IO3	IO4
14	IO5	IO6
15	IO7	GND
16	IO8	IO9
17	IO10	IO11
18	IO12	IO13
19	IO14	IO15
20	GND	CLKOUT
21	GND	$\overline{TICO}$
22	GND	$\overline{PACO}$
23	GND	N.C.
24	GND	N.C.
25	GND	N.C.

The J2 Output Header maps two 16-bit busses to the real and imaginary outputs of the HSP45116, RO0-15 and IO0-15. In addition, two HSP45116 status outputs, $\overline{PACO}$ and $\overline{TICO}$, two HSP45116 output enables, $\overline{OER}$ and $\overline{OE}$, and a bidirectional clock line are routed to this header as shown by the signal map in Table 4. When mated with the J2 connector on the HSP-EVAL, the HSP45116's real and imaginary outputs map to the HSP-EVAL's Output Bus 2 and 1, OUT2_0-15 and OUT1_0-15, respectively.

The J3 Control Header maps one 16-bit bus to the HSP45116's control input, C0-15, and provides jumper positions for the Configuration Jumper Fields that flank the header. When mated with the HSP-EVAL's J3 Control Connector the HSP45116's Control Inputs, C0-15, are mapped to the HSP-EVAL's Input Bus 3, IN3_0-15, and the jumper positions are mapped the HSP-EVAL's Control Bus, CTL0-15. The signal map for the J3 Control Header is shown in Table 1.

Configuration Jumper Field

The Configuration Jumper Fields A and B flank either side of the Control Header J3 as shown in Table 1. Positions within the Jumper Field's SA and SB signal rows map to various HSP45116 control inputs. The control inputs may be jumpered to ground or the HSP-EVAL's CTL4-15 bus via the J3 Control Header. If a control signal mapped to SA and SB is not jumpered to GND or CTL4-15, the signal is pulled high.

The Configuration Jumper Field A is also used to select whether the HSP45116's clock source is provided through the J1 Input Header or the J2 Output Header. If jumpers are inserted as shown in Figure 5, a clock signal supplied through the CLK_IN pin of the J1 Input Header drives a buffer whose output clocks the HSP45116. The jumper inserted between JA1 and JA2 feeds the buffered clock signal to the CLK_OUT pin of the J2 Output Header. If jumpers are inserted as shown in Figure 6, the CLK_OUT pin of the J2 Output Connector drives the clock buffer which

in turn drives the clock input of the HSP45116. The jumper inserted between JA2 and SA2 allows the Input Header's CLK_IN pin to be driven by the buffer output. ***NOTE: The jumper placement shown in Figure 5 is the standard configuration.***.

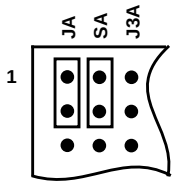


FIGURE 5. JUMPER CONFIGURATION IF CLOCK IS SUPPLIED THROUGH J1 INPUT HEADER

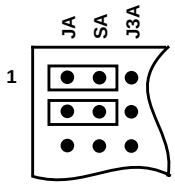


FIGURE 6. JUMPER CONFIGURATION IF CLOCK IS SUPPLIED THROUGH J2 OUTPUT HEADER

The HSP45116-DB is shipped from the factory with the default jumper configuration shown by the overlay of heavy lines onto the signal map in Table 1. For the Control Panel and Command Line Interface software to properly control operation of the HSP45116, it is assumed that the HSP45116 control inputs are jumpered as specified in the default configuration. Also, the system test software, NCOM_CHK, must be run using the default configuration.

Appendix A

Data File Structures

The Input/Output data files used by the HSP45116-DB Control Panel and Command Line Interface software contain complex data samples. The data files consist of a seven line header followed by the data itself. The header section must follow this format:

Line 1: Comment #1

Line 2: Comment #2

Line 3: Comment #3

Line 4: Comment #4

Line 5: Comment #6

Line 7: c 1 n

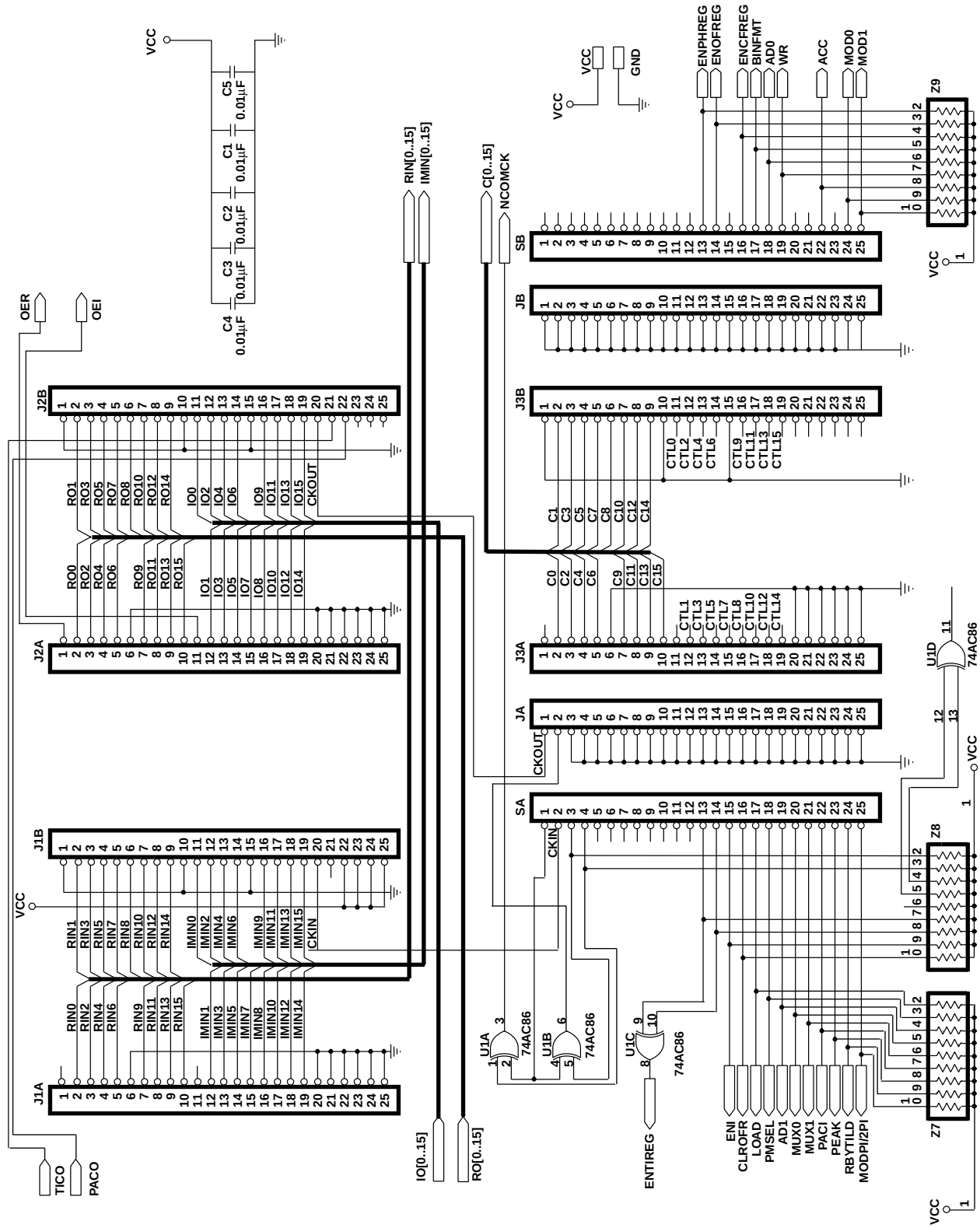
(Real Component) (Imaginary Component)

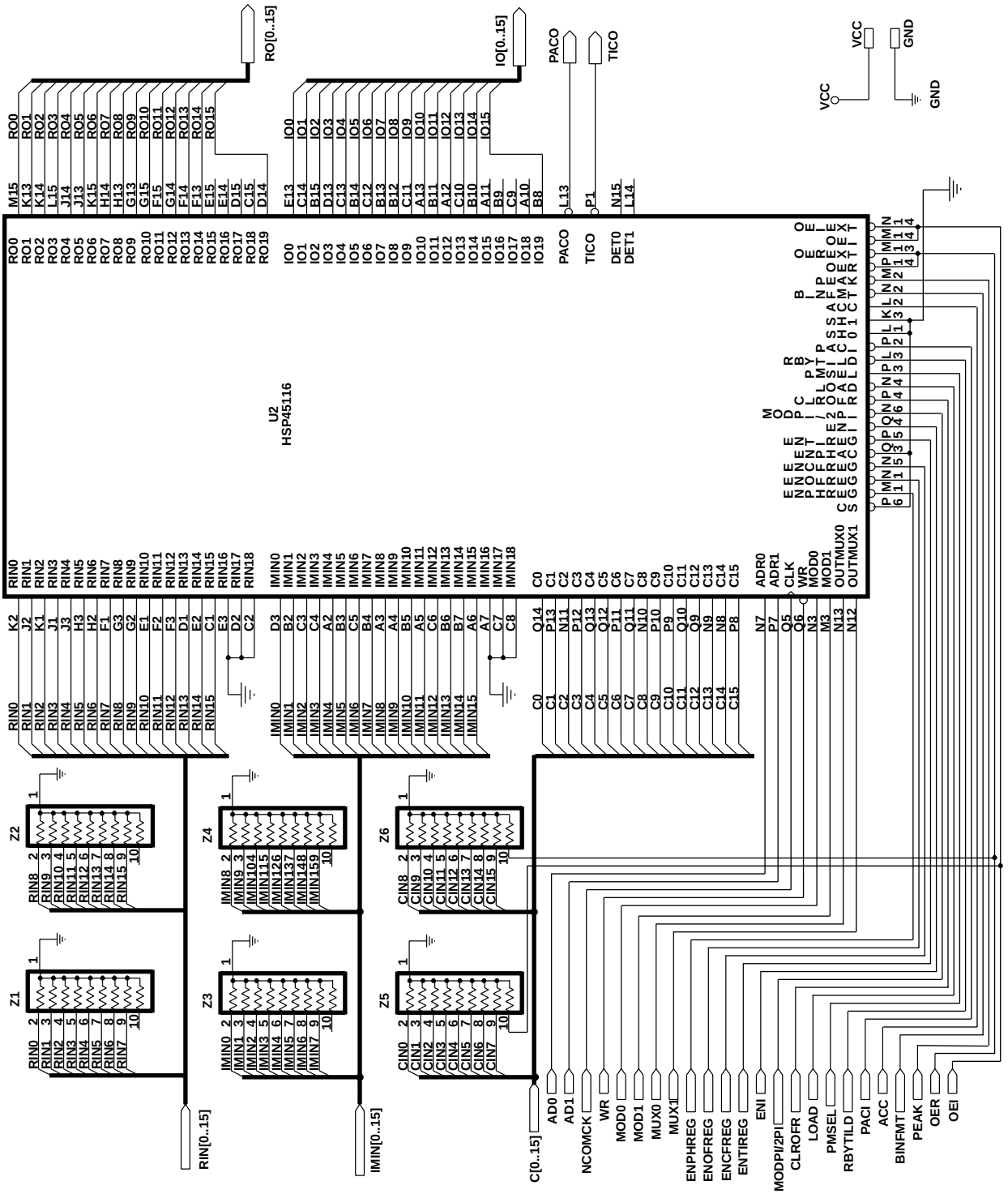
•

•

•

The 'n' on the 7th line of the header should be replaced by the number of complex samples in the file. Following the header, the complex samples are listed one per row with the real part listed first followed by the complex part. The real and imaginary components of the complex data sample are represented as 16-bit two's complement values. As a result, the real and imaginary parts of the data sample are integer values bounded by 32767 and -32768. The CMPRFILE installed in the NCOM_CHK subdirectory is an example of the input data file structure.


VCC
C5 0.01µF
C1 0.01µF
C2 0.01µF
C3 0.01µF
C4 0.01µF
OER
OEI
RIN[0..15]
IMIN[0..15]
C[0..15]
NCOMCK
ENPHREG
ENOFREG
ENCFREG
BINFMT
AD0
WR
ACC
MOD0
MOD1
GND
J2B
J2A
J1B
J1A
J3B
J3A
JB
JA
SB
SA
Z9
Z8
Z7
U1A
U1B
U1C
U1D
74AC86
CKIN
CKOUT
TICO
PACO
IO[0..15]
RO[0..15]
ENTIREG
ENI
CLROFR
LOAD
PMSEL
AD1
MUX0
MUX1
PACI
PEAK
RBYTILD
MODPI/2PI


U2
HSP45116
RO[0..15]
IO[0..15]
PACO
TICO
VCC
GND
RIN[0..15]
IMIN[0..15]
C[0..15]
Z1
Z2
Z3
Z4
Z5
Z6
ADR0
ADR1
CLK
WR
MOD0
MOD1
OUTMUX0
OUTMUX1
AD0
AD1
NCOMCK
MUX0
MUX1
ENPHREG
ENOFREG
ENCFREG
ENTIREG
ENI
MODPI/2PI
CLROFR
LOAD
PMSEL
RBYTILD
PACI
ACC
BINFMT
PEAK
OER
OEI

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029