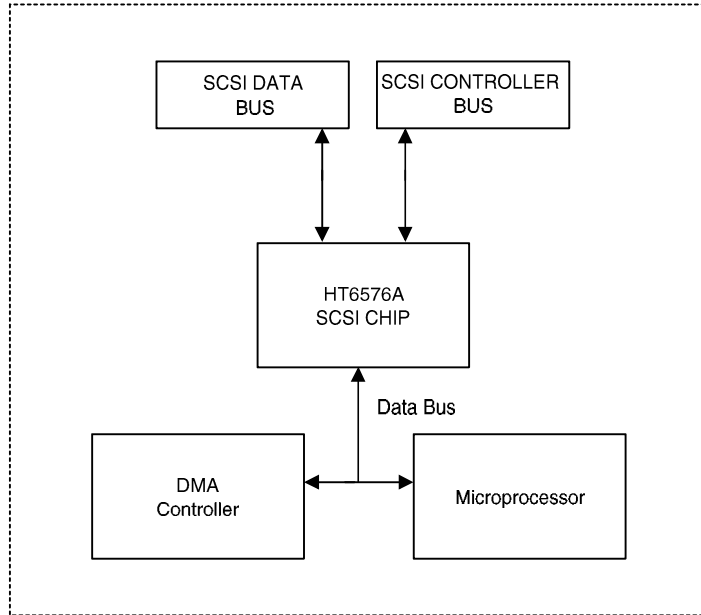


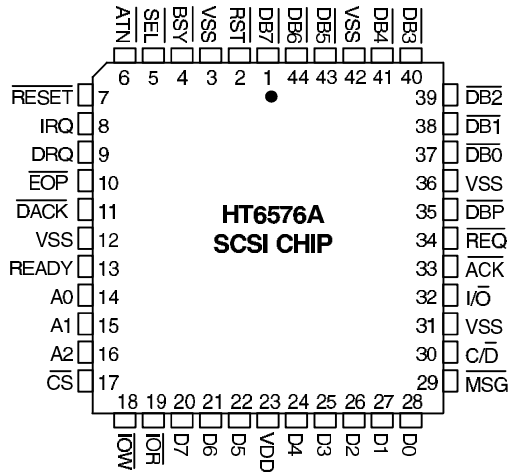
**Features**

- Support the ANSI X3.131-1986 standard
- Asynchronous transfer rate to 5 Mbyte/sec
- Support initiator and target mode
- 0.8um CMOS process
- On chip 48mA single-ended drivers and receivers
- Non internal clock needed
- 44pins PLCC package

**Block Diagram**



**Pin Diagram**



**Pin Description**

**Host Interface Signal**

Pin No	Pin Name	I/O	Description
14~16	A0~A2	I	Address Lines
17	$\overline{CS}$	I	Chip Select, active low
11	$\overline{DACK}$	I	DMA Acknowledge, active low
9	DRQ	O	DMA Request
24~28, 20~22	D0~D7	I/O	Data Lines
10	$\overline{EOP}$	I	End of Process, active low
19	$\overline{IOR}$	I	I/O Read, active low
18	$\overline{IOW}$	I	I/O Write, active low
8	IRQ	O	Interrupt Request
13	READY	O	Ready
7	$\overline{RESET}$	I	Reset, active low

**SCSI Interface Signals**

Pin No	Pin Name	I/O	Description
33	$\overline{\text{ACK}}$	I/O	Acknowledge, active low
6	$\overline{\text{ATN}}$	I/O	Attention, active low
4	$\overline{\text{BSY}}$	I/O	Busy, active low
30	$\overline{\text{C/D}}$	I/O	Control/Data, active low
32	$\overline{\text{I/O}}$	I/O	Input/Output, active low
29	$\overline{\text{MSG}}$	I/O	Message, active low
34	$\overline{\text{REQ}}$	I/O	Request, active low
2	$\overline{\text{RST}}$	I/O	Reset, active low
37~41, 43, 44, 1	$\overline{\text{DB0}}\text{--}\overline{\text{DB7}}$	I/O	SCSI Data Bus, active low
35	$\overline{\text{DBP}}$	I/O	SCSI Parity Bit, active low
5	$\overline{\text{SEL}}$	I/O	Select, active low

**VSS**

3, 12, 31, 36, 42

**VDD**

23

**Registers**
**Address 0**

Current SCSI data register(READ ONLY)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
-----	-----	-----	-----	-----	-----	-----	-----

The SCSI bus parity is checked at the beginning of the read cycle.

Output data register(WRITE ONLY)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
-----	-----	-----	-----	-----	-----	-----	-----

**Address 1: Initiator command register**

WRITE

7	6	5	4	3	2	1	0
ASSERT $\overline{\text{RST}}$	TRI-STATE	RESERVED	ASSERT $\overline{\text{ACK}}$	ASSERT $\overline{\text{BSY}}$	ASSERT $\overline{\text{SEL}}$	ASSERT $\overline{\text{ATN}}$	ASSERT DATA

- BIT 7: ASSERT  $\overline{\text{RST}}$   
WHEN SET, THE  $\overline{\text{RST}}$  SIGNAL IS ASSERTED ON THE SCSI BUS
- BIT 6: TRI-STATE (TEST MODE)
- BIT 5: RESERVED (0)
- BIT 4: ASSERT  $\overline{\text{ACK}}$   
WHEN SET, THE  $\overline{\text{ACK}}$  SIGNAL IS ASSERTED ON THE SCSI BUS
- BIT 3: ASSERT  $\overline{\text{BSY}}$   
WHEN SET, THE  $\overline{\text{BSY}}$  SIGNAL IS ASSERTED ON THE SCSI BUS
- BIT 2: ASSERT  $\overline{\text{SEL}}$   
WHEN SET, THE  $\overline{\text{SEL}}$  SIGNAL IS ASSERTED ON THE SCSI BUS
- BIT 1: ASSERT  $\overline{\text{ATN}}$   
WHEN SET, THE  $\overline{\text{ATN}}$  SIGNAL IS ASSERTED ON THE SCSI BUS
- BIT 0: ASSERT DATA  
WHEN SET, This bit allows the contents of the output data register to be enabled as chip outputs on SCSI signal  $\overline{\text{DB0}}\text{--}\overline{\text{DB7}}$

READ

7	6	5	4	3	2	1	0
RET	ARBIT PROGRESS	LOST ARBIT	ACK	BSY	SEL	ATN	ASSERT DATA

**Address 2: Mode register**

READ/WRITE

7	6	5	4	3	2	1	0
LOCK DMA	TARGET MODE	ENABLE PARITY	ENABLE PARITY	ENABLE EOP	MONITOR CHECK BUSY	DMA IRQ MODE	ARBIT

- BIT 7: BLOCK MODE DMA
- BIT 6: TARGET MODE  
When set, the chip operates as an SCSI bus target device.
- BIT 5: ENABLE PARITY CHECKING  
When set, data received on the SCSI data bus is checked for odd parity.

- **BIT 4: ENABLE PARITY INTERRUPT**  
When set, this bit causes the IRQ signal to be asserted if a parity error is detected.
- **BIT 3: ENABLE EOP INTERRUPT**  
When set, this bit causes the IRQ signal to be asserted if  $\overline{EOP}$  is received from the DMA controller.
- **BIT 2: MONITOR BUSY**  
When set, this bit causes the IRQ signal to be asserted when  $\overline{BSY}$  changes to the inactive state for at least a bus settle delay.
- **BIT 1: DMA MODE**
- **BIT 0: Arbitrate**  
When set, this bit starts the arbitration process.

**Address 3: Target command register**

	7	6	5	4	3	2	1	0
	LAST BYTE	X	X	X	ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C/D}$	ASSERT $\overline{I/O}$
R					R/W	R/W	R/W	R/W

- **BIT 7: LAST BYTE SEND (READ ONLY)**
- **BIT 3: ASSERT  $\overline{REQ}$**   
WHEN SET, THE  $\overline{REQ}$  SIGNAL IS ASSERTED ON THE SCSI BUS (IN TARGET MODE)
- **BIT 2: ASSERT  $\overline{MSG}$**   
WHEN SET, THE  $\overline{MSG}$  SIGNAL IS ASSERTED ON THE SCSI BUS (IN TARGET MODE)
- **BIT 1: ASSERT  $\overline{C/D}$**   
WHEN SET, THE  $\overline{C/D}$  SIGNAL IS ASSERTED ON THE SCSI BUS (IN TARGET MODE)
- **BIT 0: ASSERT  $\overline{I/O}$**   
WHEN SET, THE  $\overline{I/O}$  SIGNAL IS ASSERTED ON THE SCSI BUS (IN TARGET MODE)

**Address 4: Current SCSI Bus Register**

READ

	7	6	5	4	3	2	1	0
	RST	BSY	REQ	MSG	$\overline{C/D}$	$\overline{I/O}$	SEL	DBP

WRITE    -SELECT ENABLE REGISTER

	7	6	5	4	3	2	1	0
	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0

**Address 5: Bus And Status**

READ

7	6	5	4	3	2	1	0
END DMA	DMA REQUEST	PARITY ERROR	IRQ	PHASE MATCH	BUS ERROR	ATN	ACK

WRITE     -START DMA SEND

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

**Address 6: Input Data**

READ

7	6	5	4	3	2	1	0
LDB7	LDB6	LDB5	LDB4	LDB3	LDB2	LDB1	LDB0

LATCH SCSI DATA. The register represent the complement of the active low SCSI data bus.

WRITE     -START DMA TARGET RECEIVE

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

**Address 7:**

READ     -RESET PARITY/INTERRUPT

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

WRITE     -START DMA INITIATOR RECEIVE

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

**Interrupts****SELECTION/RESELECTION**

- $\overline{\text{SEL}}$ = ACTIVE LOW
- $\overline{\text{BSY}}$  IS FALSE FOR AT LEAST 400NS
- HT6576A DEVICE ID (SELECT REGISTER) is active on the SCSI bus will generate IRQ.

**END OF PROCESS (EOP) INTERRUPT**

- $\overline{\text{EOP}}$ = ACTIVE LOW
- $\overline{\text{DACK}}$ = ACTIVE LOW
- $\overline{\text{IOR}}$  OR  $\overline{\text{IOW}}$ = ACTIVE LOW
- DMA MODE
- ENABLE EOP IRQ  $\Rightarrow$  GENERATE EOP IRQ

**SCSI BUS  $\overline{\text{RST}}$ /IRQ**

When An SCSI  $\overline{\text{RST}}$  active low, the IRQ is generated.

**PARITY ERROR IRQ**

An IRQ is generated for a received parity error if enable parity checking bit and the enable parity interrupt bit are set.

**BUS PHASE MISMATCH IRQ**

If the DMA MODE bit is active and a phase mismatch occurs when  $\overline{\text{REQ}}$  from false to true, an interrupt is generated

**LOSS OF BSY/IRQ**

- MONITOR  $\overline{\text{BSY}}$  bit= 1
- $\overline{\text{BSY}}$ = ACTIVE LOW FOR 400ns WILL GENERATE IRQ

**Electrical Characteristics**
**D.C. Characteristics**
**Absolute Maximum Ratings**

(Ta=25°C)

<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
Tstg	Storage Temperature	-55	150	°C
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
V <sub>IN</sub>	Input Voltage	V <sub>SS</sub> -0.5	V <sub>DD</sub> +0.5	V
ESD	Electrostatic Discharge	-5000	5000	V

**Operating Conditions**

(Ta=25°C)

<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
V <sub>DD</sub>	Supply Voltage	4.75	5.25	V
I <sub>DD</sub>	Supply Current	—	20	mA
Ta	Operating Free-Air	0	70	°C

**SCSI Signals**

(Ta=25°C)

<b>Symbol</b>	<b>Characteristic</b>	<b>Condition</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
V <sub>IH</sub>	Input High Voltage	—	2.0	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	—	V <sub>SS</sub> -0.5	0.8	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =48mA	V <sub>SS</sub>	0.5	V
V <sub>HYS</sub>	Hysteresis	—	200	450	mV
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.5	48	—	mA
I <sub>IH</sub>	Input High Leakage	V <sub>IH</sub> = 5.25V	—	50	μA
I <sub>IL</sub>	Input Low Leakage	V <sub>IL</sub> =V <sub>SS</sub>	—	-50	μA



## Microprocessor Data Bus D0-D7

(Ta=25°C)

Symbol	Characteristic	Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	—	2.0	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	—	V <sub>SS</sub> -0.5	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-4.0mA	2.4	V <sub>DD</sub>	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =8.0mA	V <sub>SS</sub>	0.4	V
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =V <sub>DD</sub> -0.5V	-4.0	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8.0	—	mA
I <sub>IH</sub>	Input High Leakage	V <sub>IH</sub> =5.25V	—	10	μA
I <sub>IL</sub>	Input Low Leakage	V <sub>IL</sub> =V <sub>SS</sub>	—	-10	μA
I <sub>TL</sub>	Tri-State Leakage	—	-10	10	μA

 A0~A2,  $\overline{CS}$ ,  $\overline{EOP}$ ,  $\overline{IOR}$ ,  $\overline{IOW}$ ,  $\overline{RESET}$ 

(Ta=25°C)

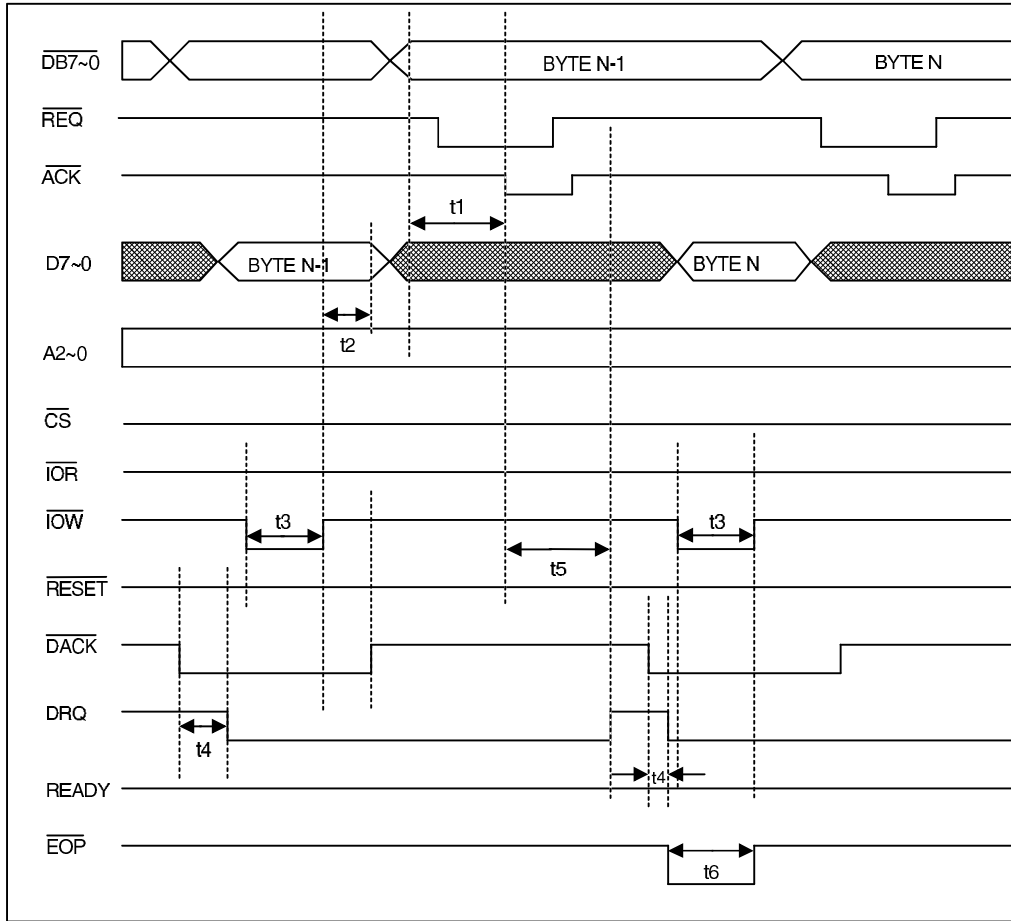
Symbol	Characteristic	Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	—	2.0	V <sub>DD</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	—	V <sub>SS</sub> -0.5	0.8	V
I <sub>IH</sub>	Input High Leakage	V <sub>IH</sub> =5.25V	10	—	μA
I <sub>IL</sub>	Input Low Leakage	V <sub>IL</sub> =V <sub>SS</sub>	-10	—	μA

## DRQ, IRQ, READY,

Symbol	Characteristic	Condition	Min.	Max.	Unit
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-4.0mA	2.4	V <sub>DD</sub>	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =8.0mA	V <sub>SS</sub>	0.4	V
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =V <sub>DD</sub> -0.5V	-4.0	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8.0	—	mA

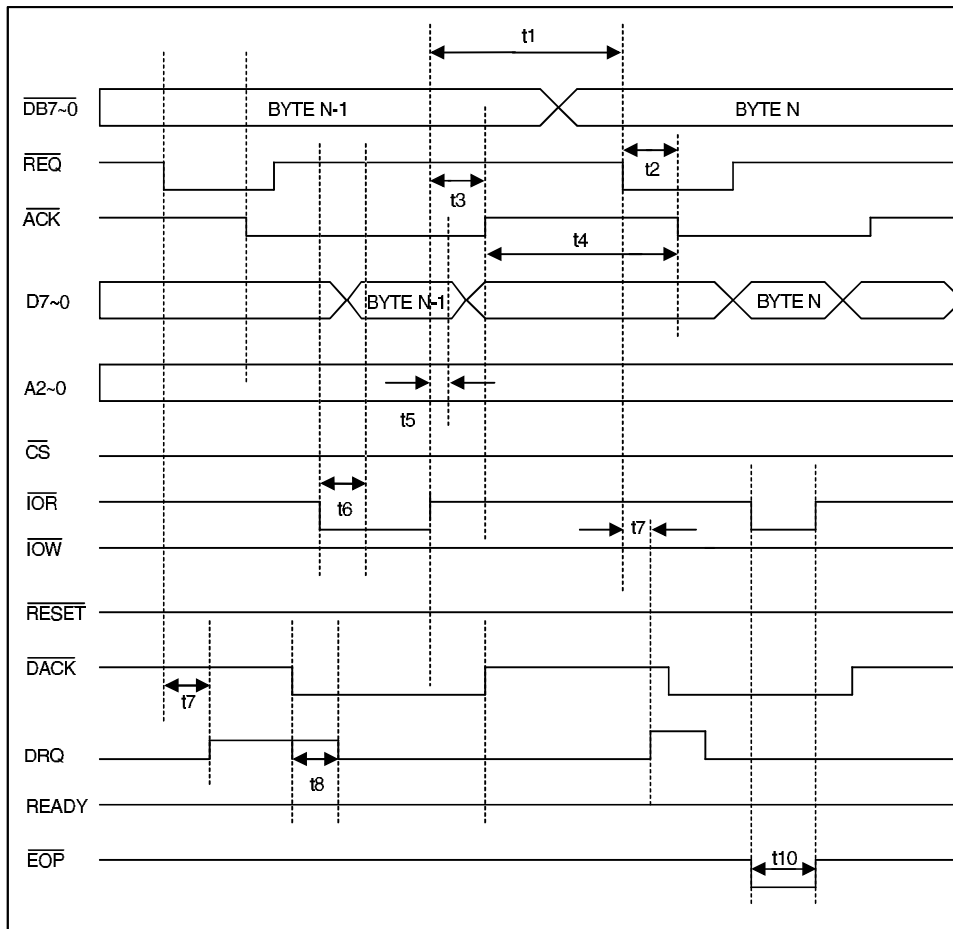
## Timing Diagram

### Initiator Send



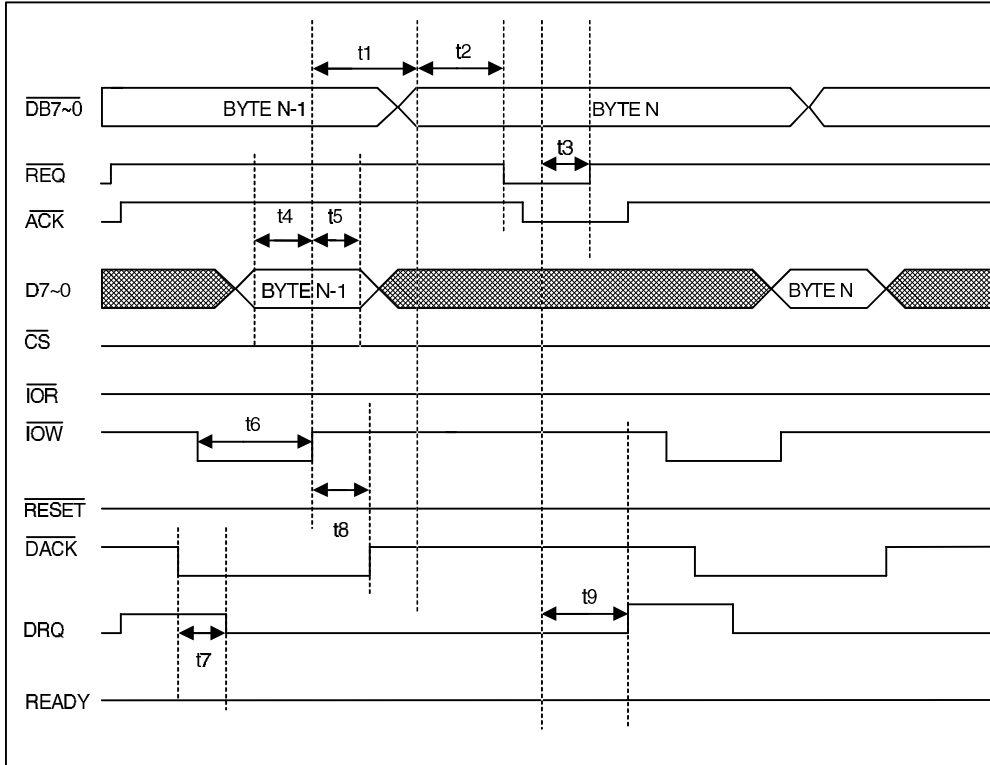
Name	Description	Min.	Max.	Unit
t1	SCSI Data setup time to $\overline{\text{ACK}}$ active	40	—	ns
t2	Data Bus held time from $\overline{\text{IOW}}$ inactive	10	—	ns
t3	$\overline{\text{IOW}}$ active time	30	—	ns
t4	$\overline{\text{DACK}}$ active, to $\overline{\text{DRQ}}$ inactive	—	20	ns
t5	$\overline{\text{ACK}}$ active to next $\overline{\text{DRQ}}$ active	—	45	ns
t6	$\overline{\text{EOP}}$ active time	30	—	ns

Initiator Receive



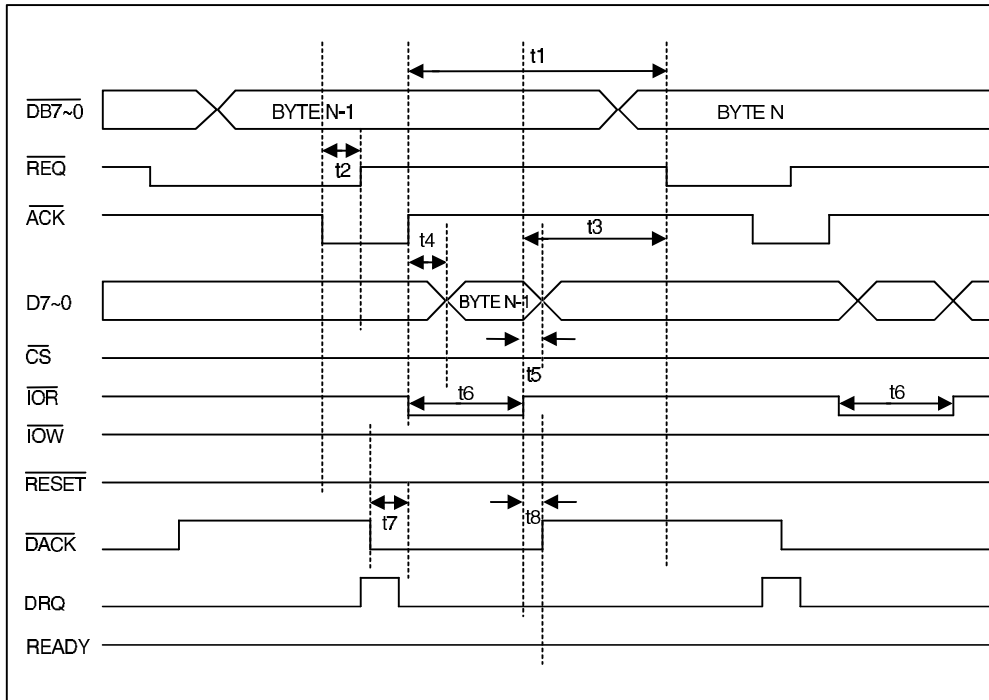
Name	Description	Min.	Max.	Unit
t1	$\overline{IOR}$ inactive to next $\overline{REQ}$ active	50	—	ns
t2	$\overline{REQ}$ active to $\overline{ACK}$ active	50	—	ns
t3	$\overline{IOR}$ inactive to $\overline{ACK}$ inactive	10	—	ns
t4	$\overline{ACK}$ inactive time	50	—	ns
t5	Data Bus hold time from $\overline{IOR}$ inactive	10	—	ns
t6	Data Bus valid time from $\overline{IOR}$ active	—	20	ns
t7	$\overline{REQ}$ active to $\overline{DRQ}$ active	—	25	ns
t8	$\overline{DACK}$ active to $\overline{DRQ}$ inactive	—	20	ns
t9	$\overline{DACK}$ inactive to next $\overline{DRQ}$ active	20	—	ns
t10	$\overline{EOP}$ active time	30	—	ns

Target Send (Non-block mode)



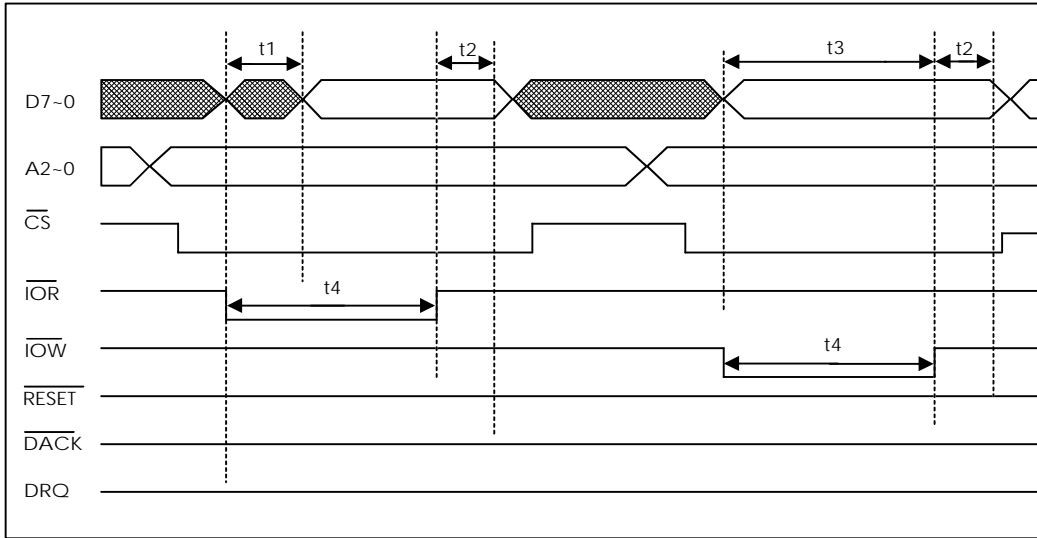
Name	Description	Min.	Max.	Unit
t1	SCSI data hold time from $\overline{IOW}$ inactive	—	30	ns
t2	SCSI data setup time to $\overline{REQ}$ active	40	—	ns
t3	$\overline{ACK}$ active to $\overline{REQ}$ inactive	—	30	ns
t4	Data Bus setup time to $\overline{IOW}$ inactive	10	—	ns
t5	Data Bus hold time from $\overline{IOW}$ inactive	10	—	ns
t6	$\overline{IOW}$ active time	30	—	ns
t7	$\overline{DACK}$ active to DRQ inactive	—	20	ns
t8	$\overline{IOW}$ inactive to $\overline{DACK}$ inactive	0	—	ns
t9	$\overline{ACK}$ active to next DRQ active	—	45	ns

Target Receive (Non-block mode)



Name	Description	Min.	Max.	Unit
t1	$\overline{\text{ACK}}$ inactive to next $\overline{\text{REQ}}$ active	50	—	ns
t2	$\overline{\text{ACK}}$ active to $\overline{\text{REQ}}$ inactive	—	30	ns
t3	$\overline{\text{IOR}}$ inactive to next $\overline{\text{REQ}}$ active	50	—	ns
t4	Data Bus setup time to $\overline{\text{IOR}}$ active	—	20	ns
t5	Data Bus hold time from $\overline{\text{IOR}}$ inactive	10	—	ns
t6	$\overline{\text{IOR}}$ active time	30	—	ns
t7	$\overline{\text{DACK}}$ active to $\overline{\text{DRQ}}$ inactive	—	20	ns
t8	$\overline{\text{IOR}}$ inactive to $\overline{\text{DACK}}$ inactive	0	—	ns

PIO Timing



Name	Description	Min.	Max.	Unit
t1	Data valid time from $\overline{IOR}$ active	—	20	ns
t2	Data hold time from $\overline{IOR}$ inactive	10	—	ns
t3	Data setup time to $\overline{IOW}$ inactive	10	—	ns
t4	$\overline{IOR}$ or $\overline{IOW}$ active time	30	—	ns