HV300 Hot Swap Demo Board

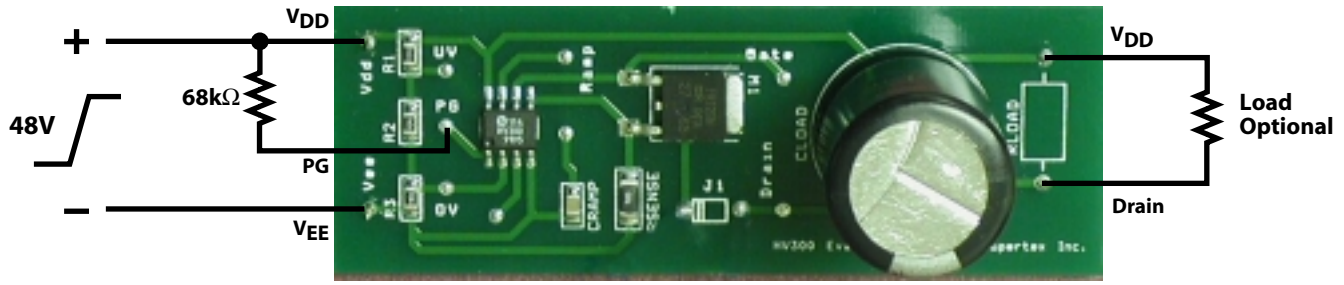
Introduction

The HV300DB1 demonstration board contains all of the circuitry necessary to safely hot-plug a -48V peripheral into a live backplane. The electrolytic capacitor, Cload simulates the input filter capacitor of a DC-to-DC converter. Cload should be removed if an actual DC-to-DC converter is being used as the load.

Specifications

Input voltage range	35V to 65V
Undervoltage lockout	35V
Overvoltage lockout	65V
Maximum continuous load current	1.7A
Switch resistance	0.21Ω
Current sense resistance	0.05Ω

Board Layout and Connections



V_{DD} Input and Output

V_{DD} is the positive power supply terminal. It is also connected to the output load. Resistors, R1, R2, and R3 are chosen to allow for an operating input range of 35V to 65V. The HV300LG is capable of operating up to 90V.

V_{EE} Input

Vee is the negative power supply terminal. MOSFET, M1 is used to connect and disconnect V_{EE} to the drain output.

Drain Output

This is the negative side for the output load. V_{EE} is connected to this pin via MOSFET M1 controlled by the HV300LG.

PG Test Point

PG is the Power Good (PWRGD) test point, which is an open drain N-channel MOSFET with “ok” high logic. An external pull up resistor should be connected to this point. PG can withstand pull up voltages of up to 90V. To examine PG operation, a resistor connected from V_{DD} to PG is acceptable. Normally PG would be connected to an enable input on a DC-to-DC converter power supply.

UV and OV Test Point

Voltages on these test points sets the under voltage and over voltage values. These test points can be probed to examine the divided down values set by R1, R2 and R3. The window comparator works around 1.21V nominally with 100mV of hysteresis.

Ramp Test Point

This test point provides access to the ramp capacitor’s positive terminal, which is used to program the hot swap timing profile.

Gate Test Point

This is the gate voltage on MOSFET M1. The HV300LG modulates the resistance M1 by controlling its gate profile. This test point allows examination of the gate voltage.

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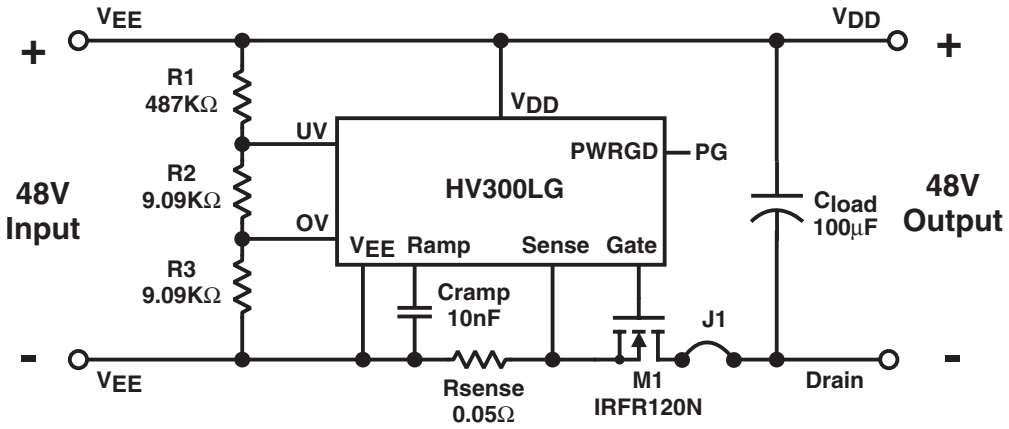
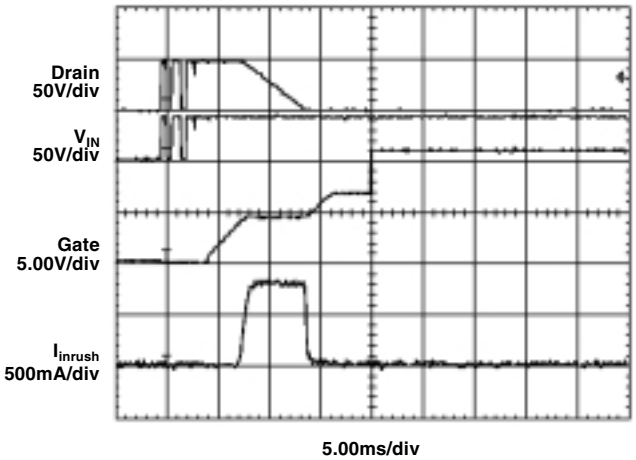
HV300DB1 Schematic



Bill of Materials for HV300DB1 Demo Board

Designator	Description	Value/Rating	Package	Part Number	Manufacturer
J1	Wire Jumper	--	--	--	--
R1	Thick film chip resistor	487K ± 1%	0805	ERJ6ENF487K	Panasonic
R2	Thick film chip resistor	9.09K ± 1%	0805	ERJ6ENF9.09K	Panasonic
R3	Thick film chip resistor	9.09K ± 1%	0805	ERJ6ENF9.09K	Panasonic
RSENSE	Thick film chip resistor	0.05 ± 1%	1206	WSL1206-.05	Dale
CRAMP	Ceramic chip capacitor, X7R	10nF, 50V	0805	ECJ-2VB1H103K	Panasonic
CLOAD	Electrolytic capacitor	100µF, 160V	--	ECA-2CHG101	Panasonic
M1	N-Channel MOSFET	100V, 0.21	Dpak	IRFR120N	International Rectifier
HV300	Hot Swap IC	90V	SO-8	HV300LG	Supertex Inc.

HV300 Typical Waveforms



Notes:

1) Some versions of the HV300DB1 may include a 10nF capacitor from IC pins 5 to 6 (the MOSFET gate to source). This capacitor is used to eliminate ringing at the end of the inrush period.
2) Current can be measured with a current probe on the Vdd line. The current drawn by the load can be measured by replacing J1 with a small resistor and measuring the voltage drop. Alternatively, a current probe can be used by replacing J1 with a wire loop.
3) PG is an open drain output and will have no effect if probed without a pullup.
4. The dual plateau characteristic of the gate response is an intended result of Supertex's closed loop hot swap solution. The steep voltage jump of the gate occurs after the MOSFET is fully on and indicates the point at which the IC goes into sleep mode (PG high).

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