

## 300V, 64-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

### Ordering Information

Device	Recommended Operating $V_{PP}$ Max*	Package Options	
		80-Lead Plastic Gullwing	Die
HV507	300V	HV507PG	HV507X

\* Please consult factory for higher voltage operation.

### Features

- HVCMOS® technology
- Operating output voltage of 300V
- Low power level shifting from 5V to 300V
- Shift register speed 8MHz @  $V_{DD} = 5V$
- 64 latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

### General Description

The HV507 is a low voltage serial to high voltage parallel converter with 64 high voltage push-pull outputs. This device has been designed for use as a printer driver for electrostatic applications. It can also be used in any application requiring multiple high voltage outputs, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded,  $D_{IOA}$  is Data In and  $D_{IOB}$  is Data Out; data is shifted from  $HV_{OUT64}$  to  $HV_{OUT1}$ . When DIR is at logic high,  $D_{IOB}$  is Data In and  $D_{IOA}$  is Data Out; data is then shifted from  $HV_{OUT1}$  to  $HV_{OUT64}$ . Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the LE, BL, or the POL inputs. Transfer of data from the shift register to the latch occurs when the  $\overline{LE}$  is high. The data in the latch is stored during  $\overline{LE}$  transition from high to low.

### Absolute Maximum Ratings<sup>1</sup>

Supply voltage, $V_{DD}$	-0.5V to +6V
Supply voltage, $V_{PP}$	$V_{DD}$ to 320V
Logic input levels	-0.5V to $V_{DD} + 0.5V$
Ground current <sup>3</sup>	0.5A
High voltage supply current <sup>2</sup>	0.5A
Continuous total power dissipation <sup>3</sup>	1200mW
Operating temperature range	0°C to +70°C
Storage temperature range	-65°C to +150°C

#### Notes:

1. All voltages are referenced to GND.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 70°C at 26.7mW/°C.

## Electrical Characteristics (for $V_{DD} = 5V$ , $V_{PP} = 300V$ , $T_A = 25^\circ C$ )

### DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{DD}$	$V_{DD}$ supply current			15	mA	$f_{CLK} = 8MHz$ , $f_{DATA} = 4MHz$ $\overline{LE} = LOW$
$I_{DDQ}$	Quiescent $V_{DD}$ supply current			200	$\mu A$	All $V_{IN} = 0V$ or $V_{DD}$
$I_{PP}$	High voltage supply current			0.50	mA	$V_{PP} = 300V$ All outputs high
				0.50	mA	$V_{PP} = 300V$ All outputs low
$I_{IH}$	High-level logic input current			10	$\mu A$	$V_{IH} = V_{DD}$
$I_{IL}$	Low-level logic input current			-10	$\mu A$	$V_{IL} = 0V$
$V_{OH}$	High-level output	HV <sub>OUT</sub>	265		V	$V_{PP} = 300V$ , IHV <sub>OUT</sub> = -1mA
		Data out	$V_{DD} - 1V$		V	ID <sub>OUT</sub> = -100 $\mu A$
$V_{OL}$	Low-level output	HV <sub>OUT</sub>		35	V	$V_{DD} = 5V$ , IHV <sub>OUT</sub> = 1mA
		Data out		1.0	V	ID <sub>OUT</sub> = 100 $\mu A$
$V_{OC}$	HV <sub>OUT</sub> clamp voltage			$V_{PP} + 1.5$	V	I <sub>OC</sub> = 1mA
				-30	V	I <sub>OC</sub> = -1mA

### AC Characteristics<sup>1</sup> (For $V_{DD} = 5V$ , $V_{PP} = 300V$ , $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$f_{CLK}$	Clock frequency			8	MHz	
$t_W$	Clock width high and low	62			ns	
$t_{SU}$	Data setup time before clock rises	35			ns	
$t_H$	Data hold time after clock rises	30			ns	
$t_{WLE}$	Width of latch enable pulse	80			ns	
$t_{DLE}$	$\overline{LE}$ delay time after rising edge of clock	35			ns	
$t_{SLE}$	$\overline{LE}$ setup time before rising edge of clock	40			ns	
$t_{ON}, t_{OFF}$	Time from latch enable to HV <sub>OUT</sub>			4	$\mu s$	$C_L = 20pF$
$t_{DHL}$	Delay time clock to data out high to low			125	ns	$C_L = 20pF$
$t_{DLH}$	Delay time clock to data out low to high			125	ns	$C_L = 20pF$
$t_r, t_f$	All logic inputs			5	ns	

**Note:**

- Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD}$	Logic supply voltage	4.5	5.0	5.5	V
$V_{PP}$	High voltage supply	60		300	V
$V_{IH}$	High-level input voltage	$V_{DD} - 0.9$		$V_{DD}$	V
$V_{IL}$	Low-level input voltage	0		0.9	V
$T_A$	Operating free-air temperature	0		+70	$^\circ C$

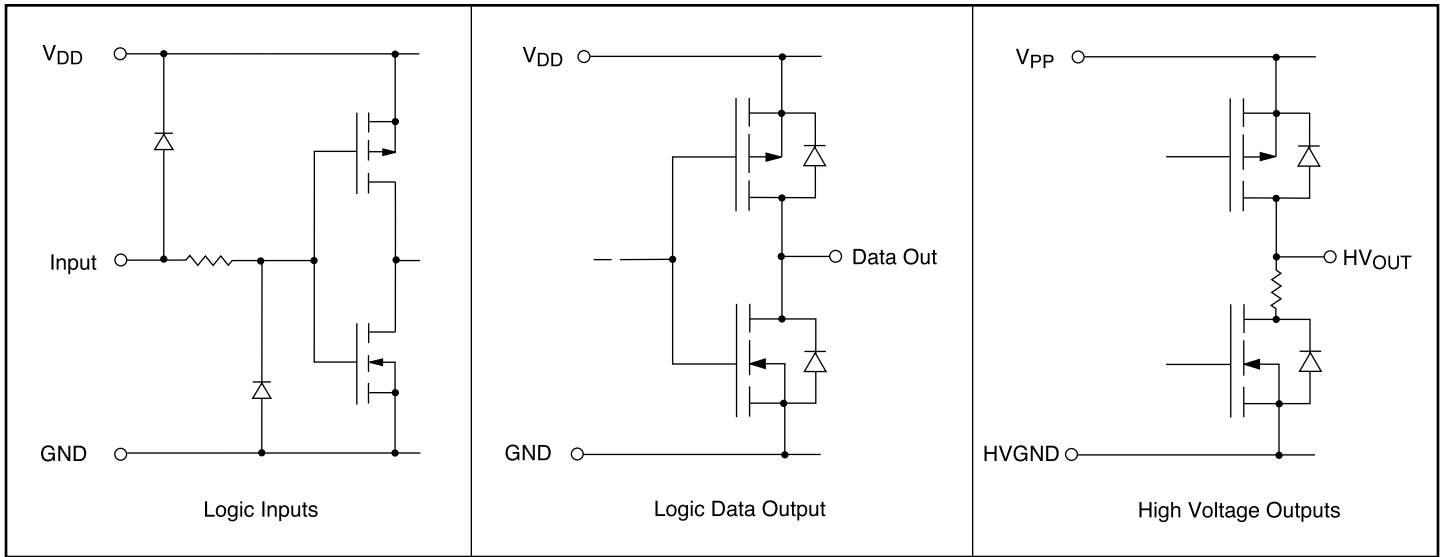
**Notes:**

Power-up sequence should be the following:

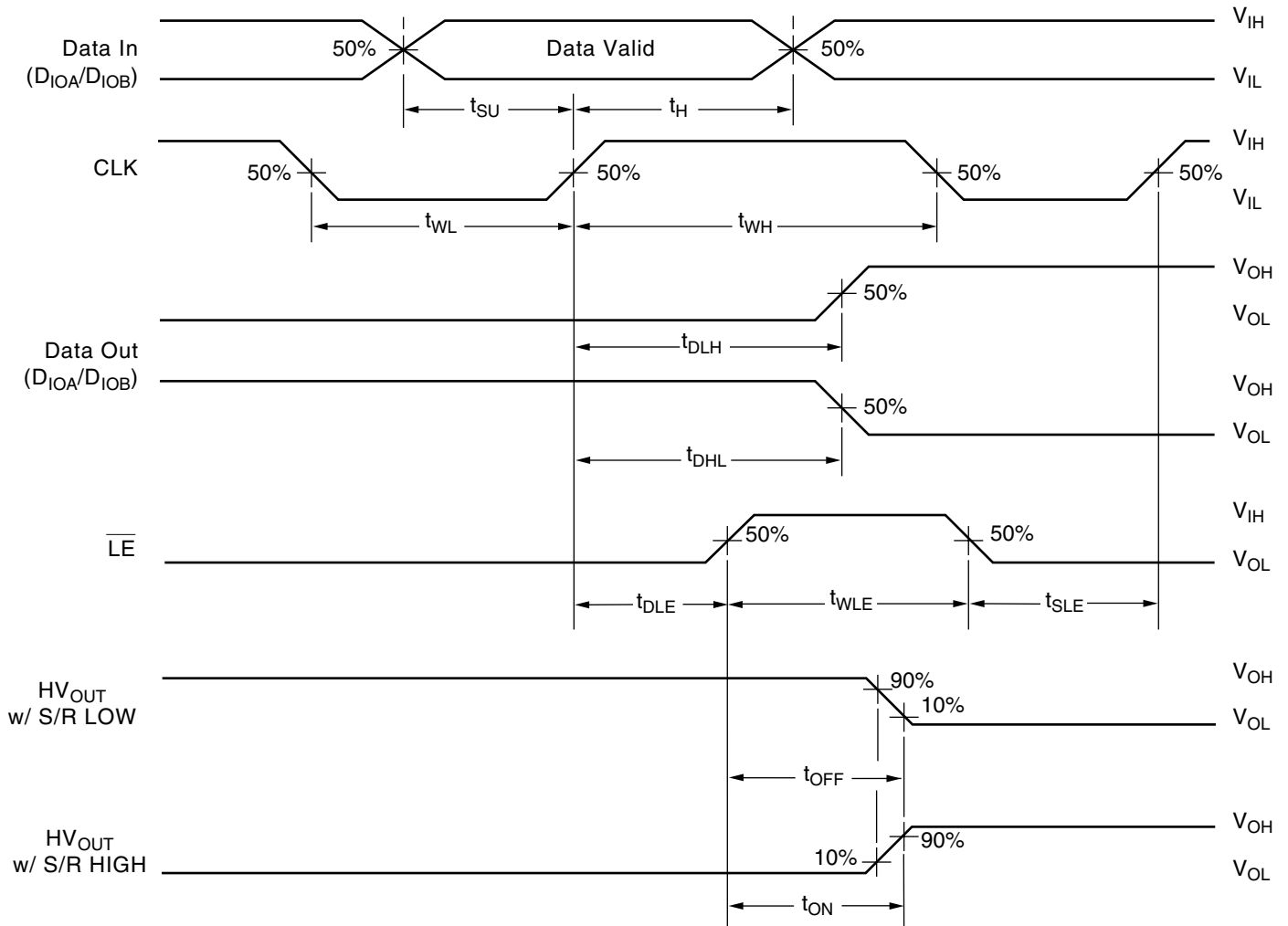
- Connect ground.
- Apply  $V_{DD}$ .
- Set all inputs (Data, CLK, Enable, etc.) to a known state.
- Apply  $V_{PP}$ .
- The  $V_{PP}$  should not drop below  $V_{DD}$  or float during operation.

Power-down sequence should be the reverse of the above.

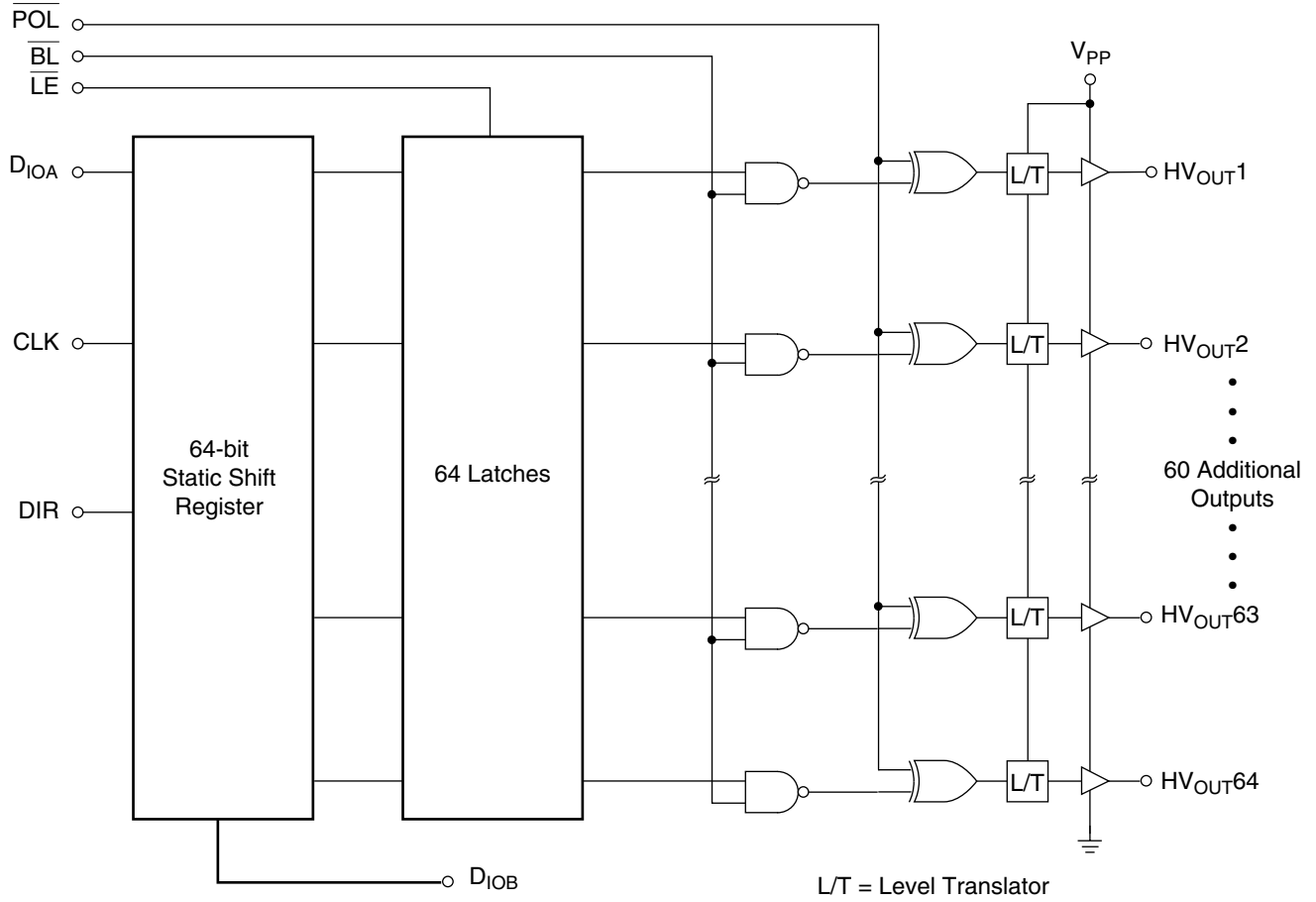
# Input and Output Equivalent Circuits



# Switching Waveforms



# Functional Block Diagram



# Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1 2...64	HV Outputs 1 2...64	Data Out *		
All on	X	X	X	L	L	X	* *...*	H H...H	*		
All off	X	X	X	L	H	X	* *...*	L L...L	*		
Invert mode	X	X	L	H	L	X	* *...*	$\overline{*} \overline{*}... \overline{*}$	*		
Load S/R	H or L	↑	L	H	H	X	H or L *...*	* *...*	*		
Store data in latches	X	X	↓	H	H	X	* *...*	* *...*	*		
	X	X	↓	H	L	X	* *...*	$\overline{*} \overline{*}... \overline{*}$	*		
Transparent latch mode	L	↑	H	H	H	X	L *...*	L *...*	*		
	H	↑	H	H	H	X	H *...*	H *...*	*		
I/O relation	D <sub>IOA</sub>	↑	X	X	X	L	Q <sub>n</sub> → Q <sub>n-1</sub>	—	D <sub>IOB</sub>		
	D <sub>IOB</sub>	↑	X	X	X	H	Q <sub>n</sub> → Q <sub>n+1</sub>	—	D <sub>IOA</sub>		

**Notes:**  
 H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.  
 \* = dependent on previous stage's state before the last CLK or last LE high.

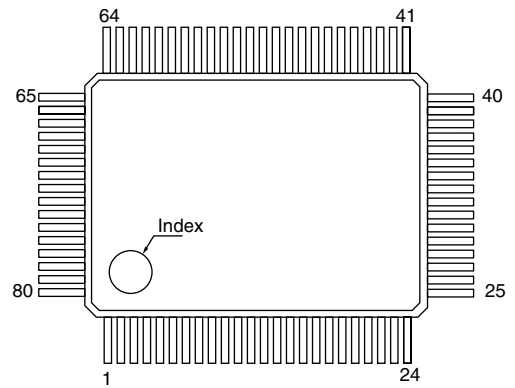
# Pin Configurations

# Package Outline

**HV507**

**80 Pin Gullwing Package**

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 41	41	HV <sub>OUT</sub> 1
2	HV <sub>OUT</sub> 42	42	HV <sub>OUT</sub> 2
3	HV <sub>OUT</sub> 43	43	HV <sub>OUT</sub> 3
4	HV <sub>OUT</sub> 44	44	HV <sub>OUT</sub> 4
5	HV <sub>OUT</sub> 45	45	HV <sub>OUT</sub> 5
6	HV <sub>OUT</sub> 46	46	HV <sub>OUT</sub> 6
7	HV <sub>OUT</sub> 47	47	HV <sub>OUT</sub> 7
8	HV <sub>OUT</sub> 48	48	HV <sub>OUT</sub> 8
9	HV <sub>OUT</sub> 49	49	HV <sub>OUT</sub> 9
10	HV <sub>OUT</sub> 50	50	HV <sub>OUT</sub> 10
11	HV <sub>OUT</sub> 51	51	HV <sub>OUT</sub> 11
12	HV <sub>OUT</sub> 52	52	HV <sub>OUT</sub> 12
13	HV <sub>OUT</sub> 53	53	HV <sub>OUT</sub> 13
14	HV <sub>OUT</sub> 54	54	HV <sub>OUT</sub> 14
15	HV <sub>OUT</sub> 55	55	HV <sub>OUT</sub> 15
16	HV <sub>OUT</sub> 56	56	HV <sub>OUT</sub> 16
17	HV <sub>OUT</sub> 57	57	HV <sub>OUT</sub> 17
18	HV <sub>OUT</sub> 58	58	HV <sub>OUT</sub> 18
19	HV <sub>OUT</sub> 59	59	HV <sub>OUT</sub> 19
20	HV <sub>OUT</sub> 60	60	HV <sub>OUT</sub> 20
21	HV <sub>OUT</sub> 61	61	HV <sub>OUT</sub> 21
22	HV <sub>OUT</sub> 62	62	HV <sub>OUT</sub> 22
23	HV <sub>OUT</sub> 63	63	HV <sub>OUT</sub> 23
24	HV <sub>OUT</sub> 64	64	HV <sub>OUT</sub> 24
25	V <sub>PP</sub>	65	HV <sub>OUT</sub> 25
26	D <sub>IOA</sub>	66	HV <sub>OUT</sub> 26
27	N/C	67	HV <sub>OUT</sub> 27
28	N/C	68	HV <sub>OUT</sub> 28
29	$\overline{BL}$	69	HV <sub>OUT</sub> 29
30	$\overline{POL}$	70	HV <sub>OUT</sub> 30
31	V <sub>DD</sub>	71	HV <sub>OUT</sub> 31
32	DIR	72	HV <sub>OUT</sub> 32
33	GND	73	HV <sub>OUT</sub> 33
34	HVGND	74	HV <sub>OUT</sub> 34
35	N/C	75	HV <sub>OUT</sub> 35
36	N/C	76	HV <sub>OUT</sub> 36
37	CLK	77	HV <sub>OUT</sub> 37
38	$\overline{LE}$	78	HV <sub>OUT</sub> 38
39	D <sub>IOB</sub>	79	HV <sub>OUT</sub> 39
40	V <sub>PP</sub>	80	HV <sub>OUT</sub> 40



top view

80-pin Gullwing Package