

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

| Device | Recommended Operating V_{PP} max | Package Options | | | |
|--------|------------------------------------|-------------------------------------|-------------------------------------|-------------------------------|---------|
| | | 44 J-Lead Quad Ceramic Chip Carrier | 44 J-Lead Quad Plastic Chip Carrier | 44 Lead Quad Plastic Gullwing | Die |
| HV5522 | 220V | HV5522DJ | HV5522PJ | HV5522PG | HV5522X |
| HV5530 | 300V | HV5530DJ | HV5530PJ | HV5530PG | HV5530X |
| HV5622 | 220V | HV5622DJ | HV5622PJ | HV5622PG | HV5622X |
| HV5630 | 300V | HV5630DJ | HV5630PJ | HV5630PG | HV5630X |

Features

- Processed with HVCMOS[®] technology
- Sink current minimum 100mA
- Shift register speed 8MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery
- 44-lead ceramic surface mount package
- Hi-Rel processing available

Absolute Maximum Ratings

| | | |
|---|--------------------------|-----------------|
| Supply voltage, V_{DD}^1 | -0.5V to +15V | |
| Output voltage, V_{PP}^1 | HV5530/HV5630 | -0.5V to +315V |
| | HV5522/HV5622 | -0.5V to +230V |
| Logic input levels ¹ | -0.5V to $V_{DD} + 0.5V$ | |
| Ground current ² | 1.5A | |
| Continuous total power dissipation ³ | Ceramic | 1500mW |
| | Plastic | 1200mW |
| Operating temperature range | Ceramic | -55°C to +125°C |
| | Plastic | -40°C to +85°C |
| Storage temperature range | -65°C to +150°C | |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260°C | |

Notes:

1. All voltages are referenced to V_{SS} .
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20°C for plastic and at 15mW/°C for ceramic.

12/13/01

General Description

The HV55 and HV56 are low-voltage serial to high-voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV55 shifts in the counterclockwise direction when viewed from the top of the package, and the HV56 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} (latch enable) input is high. The data in the latch is stored when \overline{LE} is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions | |
|--------------|-----------------------------------|------------------------|------|---------------|---|------------------------------|
| I_{DD} | V_{DD} supply current | | 15 | mA | $f_{CLK} = 8\text{MHz}$ $F_{DATA} = 4\text{MHz}$ | |
| I_{DDQ} | Quiescent V_{DD} supply current | | 100 | μA | $V_{IN} = 0\text{V}$ | |
| $I_{O(OFF)}$ | Off state output current | | 10 | μA | All outputs high All SWS parallel | |
| I_{IH} | High-level logic input current | | 1 | μA | $V_{IH} = V_{DD}$ | |
| I_{IL} | Low-level logic input current | | -1 | μA | $V_{IL} = 0\text{V}$ | |
| V_{OH} | High-level output data out | $V_{DD} - 1.0\text{V}$ | | V | $I_{Dout} = -100\mu\text{A}$ | |
| V_{OL} | Low-level output voltage | HV _{OUT} | | 15.0 | V | $I_{HVout} = +100\text{mA}$ |
| | | Data out | | 1.0 | V | $I_{Dout} = +100\mu\text{A}$ |
| V_{OC} | HV _{OUT} clamp voltage | | -1.5 | V | $I_{OL} = -100\text{mA}$ | |

AC Characteristics ($V_{DD} = 12\text{V}$, $T_C = 25^\circ\text{C}$)

| Symbol | Parameter | Min | Max | Units | Conditions |
|-----------|---|-----|-----|-------|---|
| f_{CLK} | Clock frequency | | 8 | MHz | |
| t_W | Clock width high or low | 62 | | ns | |
| t_{SU} | Data set-up time before clock falls | 25 | | ns | |
| t_H | Data hold time after clock falls | 10 | | ns | |
| t_{ON} | Turn on time, HV _{OUT} from enable | | 500 | ns | $R_L = 2\text{K}\Omega$ to V_{PP} MAX |
| t_{DHL} | Delay time clock to data high to low | | 100 | ns | $C_L = 15\text{pF}$ |
| t_{DLH} | Delay time clock to data low to high | | 100 | ns | $C_L = 15\text{pF}$ |
| t_{DLE} | Delay time clock to \overline{LE} low to high | 50 | | ns | |
| t_{WLE} | Width of \overline{LE} pulse | 50 | | ns | |
| t_{SLE} | \overline{LE} set-up time before clock falls | 50 | | ns | |

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units | |
|-------------------|--------------------------------|----------------------|----------|-------|------------------|
| V_{DD} | Logic supply voltage | 10.8 | 13.2 | V | |
| HV _{OUT} | High voltage output | HV5530 and HV5630 | -0.3 | +300 | V |
| | | HV5522 and HV5622 | -0.3 | +220 | V |
| V_{IH} | High-level input voltage | $V_{DD} - 2\text{V}$ | V_{DD} | V | |
| V_{IL} | Low-level input voltage | 0 | 2.0 | V | |
| f_{CLK} | Clock frequency | | 8 | MHz | |
| T_A | Operating free-air temperature | Plastic | -40 | +85 | $^\circ\text{C}$ |
| | | Ceramic | -55 | +125 | $^\circ\text{C}$ |

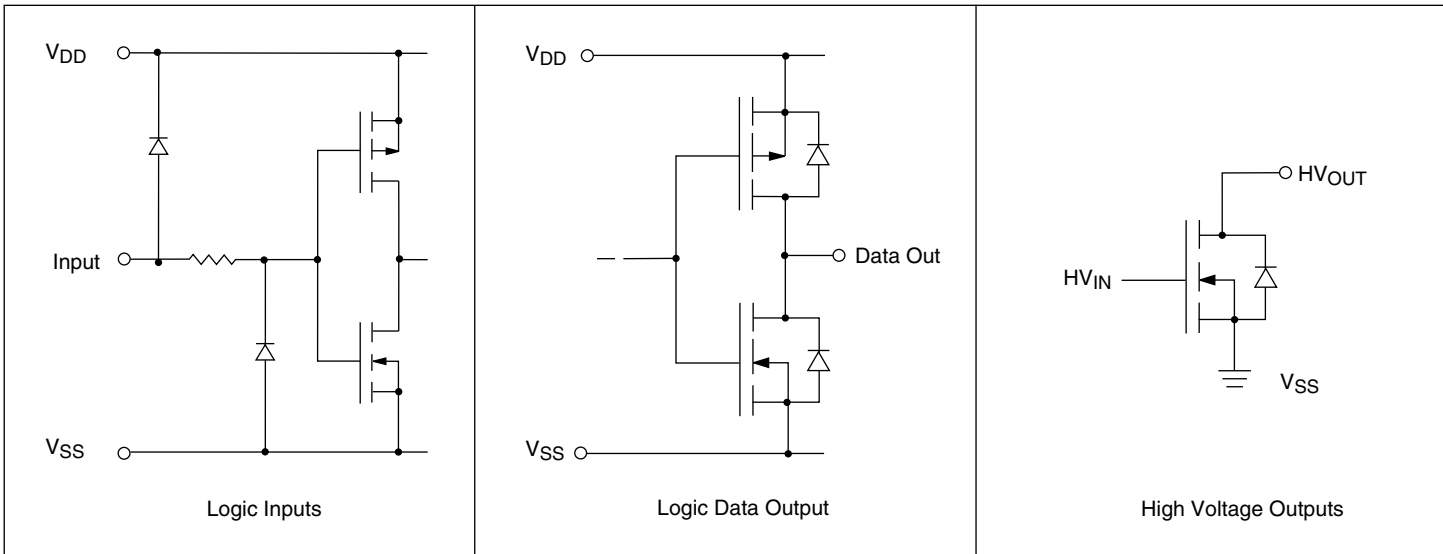
Note:

Power-up sequence should be the following:

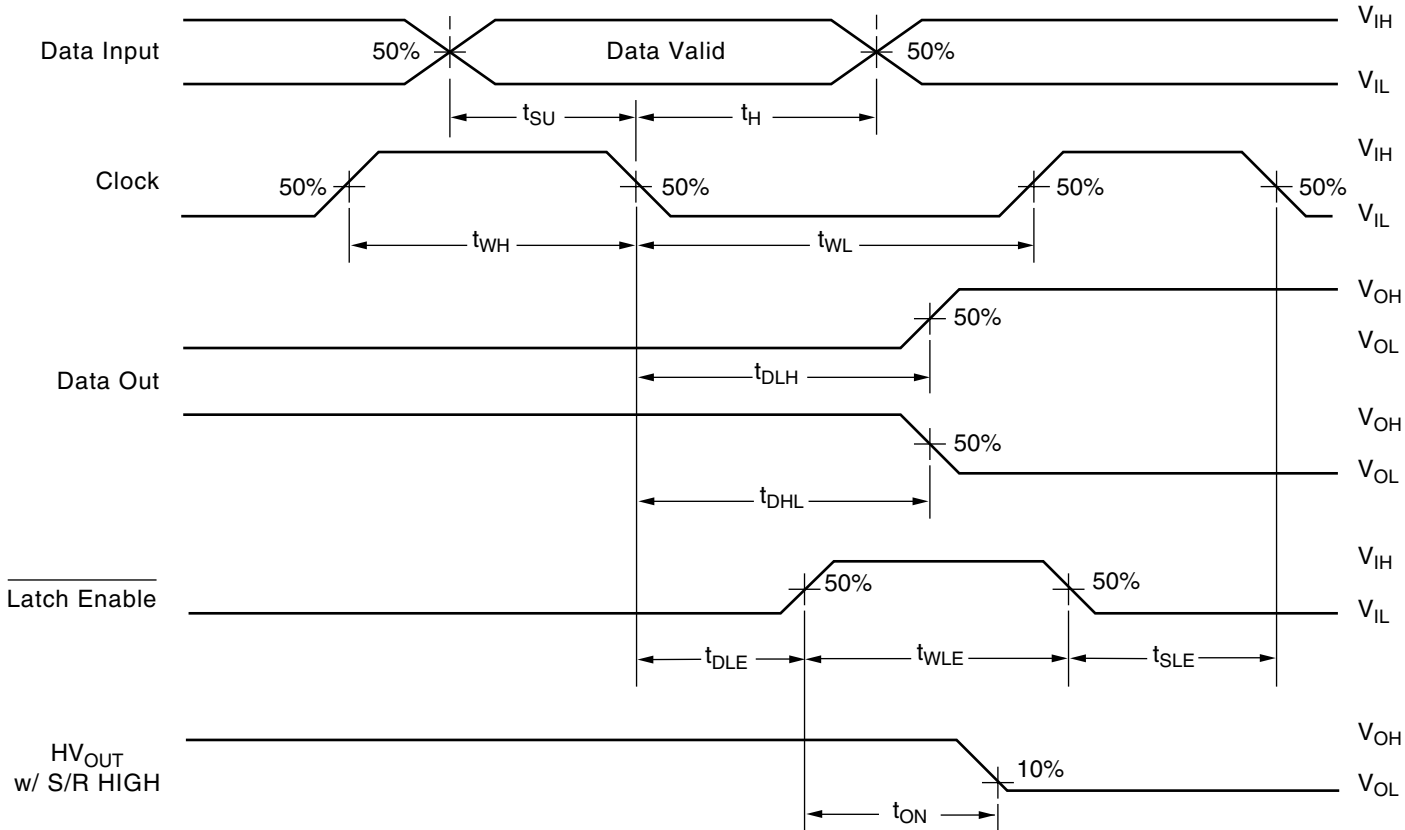
1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

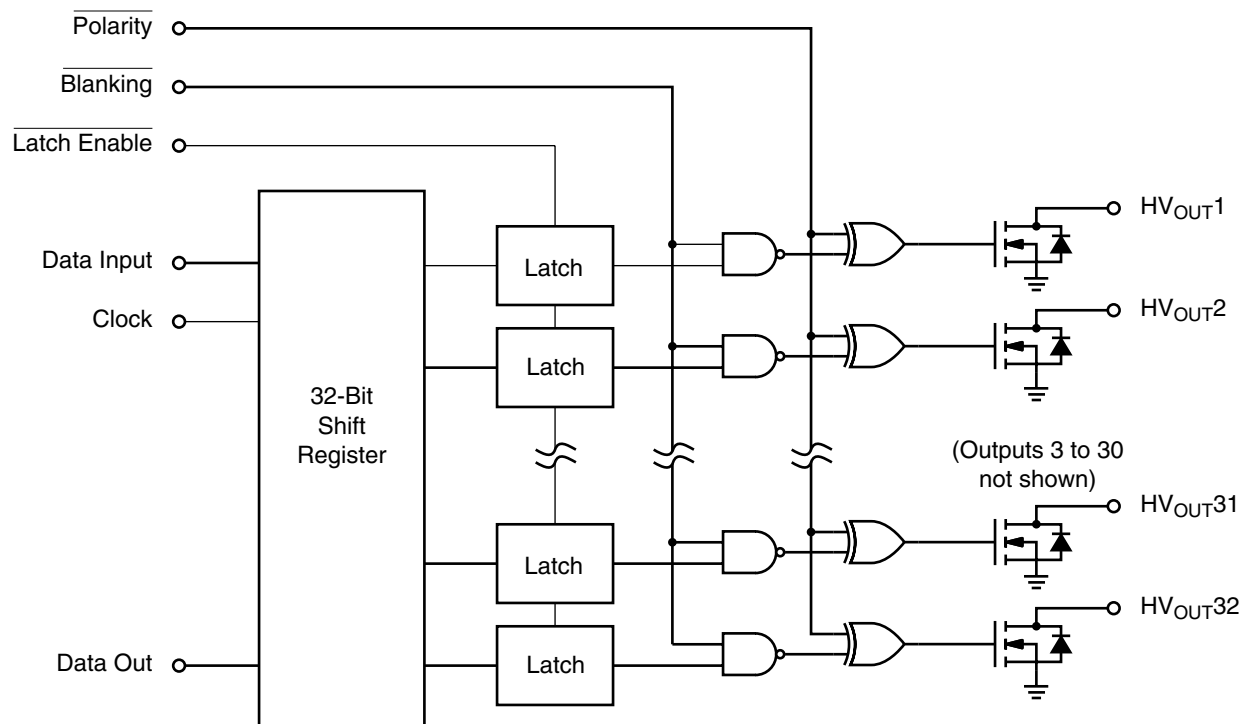
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

| Function | Inputs | | | | | Outputs | | |
|------------------------|--------|--------|-----------------|-----------------|------------------|-----------------------|-----------------------------------|---------------|
| | Data | CLK | \overline{LE} | \overline{BL} | \overline{POL} | Shift Reg 1 2...32 | HV Outputs 1 2...32 | Data Out * |
| All on | X | X | X | L | L | * ...* | On On...On | * |
| All off | X | X | X | L | H | * ...* | Off Off...Off | * |
| Invert mode | X | X | L | H | L | * ...* | $\overline{*}$ $\overline{*}$... | * |
| Load S/R | H or L | ↓ | L | H | H | H or L *...* | * ...* | * |
| Load Latches | X | H or L | ↑ | H | H | * ...* | * ...* | * |
| | X | H or L | ↑ | H | L | * ...* | $\overline{*}$ $\overline{*}$... | * |
| Transparent Latch mode | L | ↓ | H | H | H | L *...* | Off *...* | * |
| | H | ↓ | H | H | H | H *...* | On *...* | * |

Notes:
 H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition.
 * = dependent on previous stage's state before the last CLK ↓ or last \overline{LE} high.

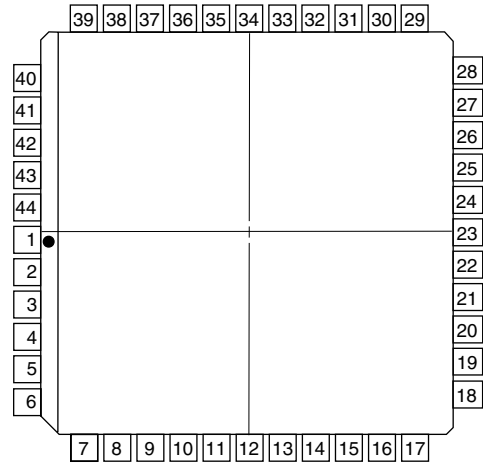
Pin Configurations

Package Outline

HV55

44 Pin J-Lead Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 16 | 23 | Clock |
| 2 | HV _{OUT} 17 | 24 | V _{SS} |
| 3 | HV _{OUT} 18 | 25 | V _{DD} |
| 4 | HV _{OUT} 19 | 26 | Latch Enable |
| 5 | HV _{OUT} 20 | 27 | Data In |
| 6 | HV _{OUT} 21 | 28 | Blanking |
| 7 | HV _{OUT} 22 | 29 | N/C |
| 8 | HV _{OUT} 23 | 30 | HV _{OUT} 1 |
| 9 | HV _{OUT} 24 | 31 | HV _{OUT} 2 |
| 10 | HV _{OUT} 25 | 32 | HV _{OUT} 3 |
| 11 | HV _{OUT} 26 | 33 | HV _{OUT} 4 |
| 12 | HV _{OUT} 27 | 34 | HV _{OUT} 5 |
| 13 | HV _{OUT} 28 | 35 | HV _{OUT} 6 |
| 14 | HV _{OUT} 29 | 36 | HV _{OUT} 7 |
| 15 | HV _{OUT} 30 | 37 | HV _{OUT} 8 |
| 16 | HV _{OUT} 31 | 38 | HV _{OUT} 9 |
| 17 | HV _{OUT} 32 | 39 | HV _{OUT} 10 |
| 18 | Data Out | 40 | HV _{OUT} 11 |
| 19 | N/C | 41 | HV _{OUT} 12 |
| 20 | N/C | 42 | HV _{OUT} 13 |
| 21 | N/C | 43 | HV _{OUT} 14 |
| 22 | Polarity | 44 | HV _{OUT} 15 |



top view
44-pin J-Lead Package

HV56

44 Pin J-Lead Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 17 | 23 | Clock |
| 2 | HV _{OUT} 16 | 24 | V _{SS} |
| 3 | HV _{OUT} 15 | 25 | V _{DD} |
| 4 | HV _{OUT} 14 | 26 | Latch Enable |
| 5 | HV _{OUT} 13 | 27 | Data In |
| 6 | HV _{OUT} 12 | 28 | Blanking |
| 7 | HV _{OUT} 11 | 29 | N/C |
| 8 | HV _{OUT} 10 | 30 | HV _{OUT} 32 |
| 9 | HV _{OUT} 9 | 31 | HV _{OUT} 31 |
| 10 | HV _{OUT} 8 | 32 | HV _{OUT} 30 |
| 11 | HV _{OUT} 7 | 33 | HV _{OUT} 29 |
| 12 | HV _{OUT} 6 | 34 | HV _{OUT} 28 |
| 13 | HV _{OUT} 5 | 35 | HV _{OUT} 27 |
| 14 | HV _{OUT} 4 | 36 | HV _{OUT} 26 |
| 15 | HV _{OUT} 3 | 37 | HV _{OUT} 25 |
| 16 | HV _{OUT} 2 | 38 | HV _{OUT} 24 |
| 17 | HV _{OUT} 1 | 39 | HV _{OUT} 23 |
| 18 | Data Out | 40 | HV _{OUT} 22 |
| 19 | N/C | 41 | HV _{OUT} 21 |
| 20 | N/C | 42 | HV _{OUT} 20 |
| 21 | N/C | 43 | HV _{OUT} 19 |
| 22 | Polarity | 44 | HV _{OUT} 18 |

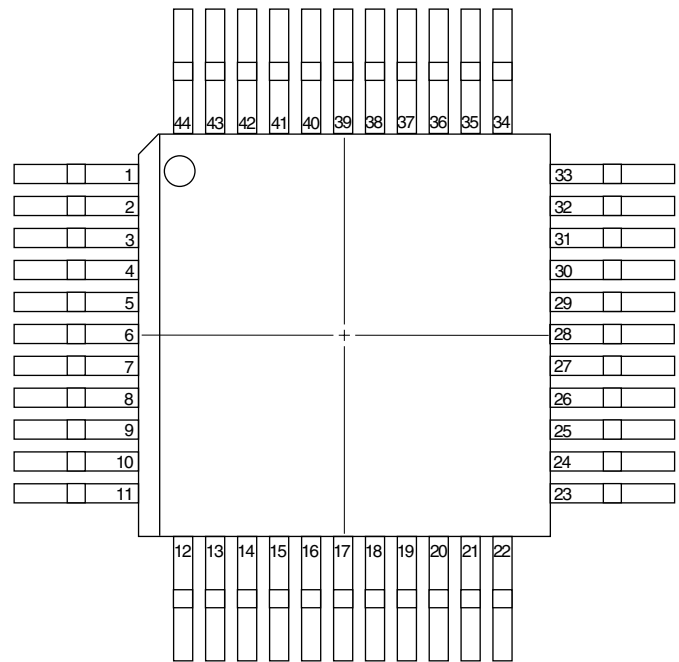
Pin Configurations

HV55

44-Pin Quad Plastic Gullwing Package

| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 11 | 23 | Data Out |
| 2 | HV _{OUT} 12 | 24 | N/C |
| 3 | HV _{OUT} 13 | 25 | N/C |
| 4 | HV _{OUT} 14 | 26 | N/C |
| 5 | HV _{OUT} 15 | 27 | Polarity |
| 6 | HV _{OUT} 16 | 28 | Clock |
| 7 | HV _{OUT} 17 | 29 | V _{SS} |
| 8 | HV _{OUT} 18 | 30 | V _{DD} |
| 9 | HV _{OUT} 19 | 31 | Latch Enable |
| 10 | HV _{OUT} 20 | 32 | Data In |
| 11 | HV _{OUT} 21 | 33 | Blanking |
| 12 | HV _{OUT} 22 | 34 | N/C |
| 13 | HV _{OUT} 23 | 35 | HV _{OUT} 1 |
| 14 | HV _{OUT} 24 | 36 | HV _{OUT} 2 |
| 15 | HV _{OUT} 25 | 37 | HV _{OUT} 3 |
| 16 | HV _{OUT} 26 | 38 | HV _{OUT} 4 |
| 17 | HV _{OUT} 27 | 39 | HV _{OUT} 5 |
| 18 | HV _{OUT} 28 | 40 | HV _{OUT} 6 |
| 19 | HV _{OUT} 29 | 41 | HV _{OUT} 7 |
| 20 | HV _{OUT} 30 | 42 | HV _{OUT} 8 |
| 21 | HV _{OUT} 31 | 43 | HV _{OUT} 9 |
| 22 | HV _{OUT} 32 | 44 | HV _{OUT} 10 |

Package Outline



top view
44-pin Quad Plastic Gullwing Package

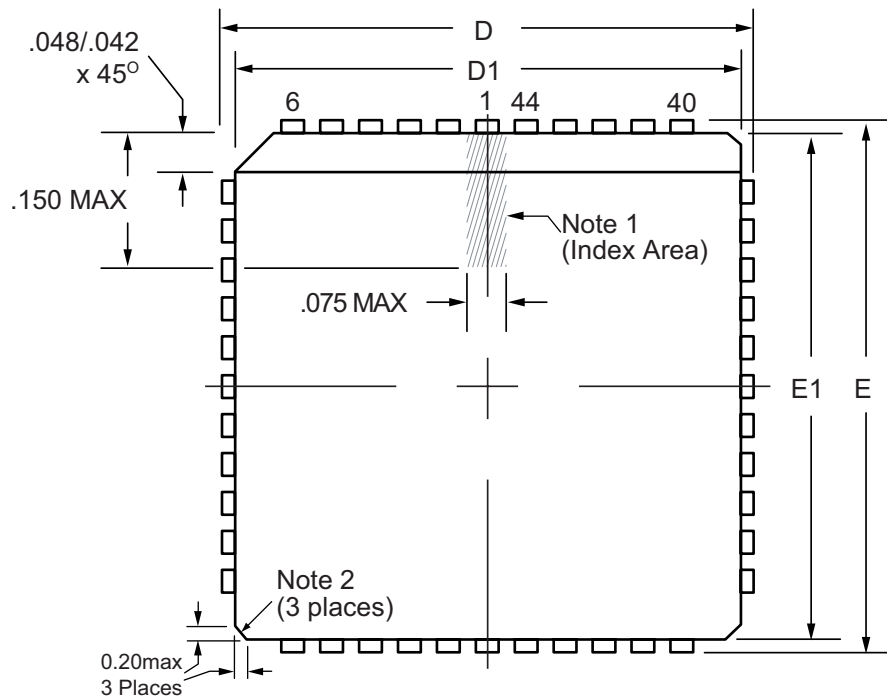
HV56

44-Pin Quad Plastic Gullwing Package

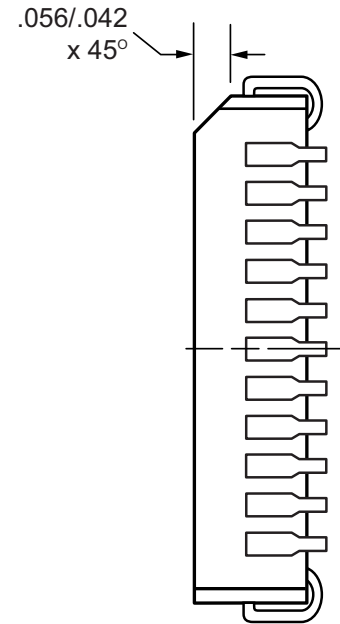
| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HV _{OUT} 22 | 23 | Data Out |
| 2 | HV _{OUT} 21 | 24 | N/C |
| 3 | HV _{OUT} 20 | 25 | N/C |
| 4 | HV _{OUT} 19 | 26 | N/C |
| 5 | HV _{OUT} 18 | 27 | Polarity |
| 6 | HV _{OUT} 17 | 28 | Clock |
| 7 | HV _{OUT} 16 | 29 | V _{SS} |
| 8 | HV _{OUT} 15 | 30 | V _{DD} |
| 9 | HV _{OUT} 14 | 31 | Latch Enable |
| 10 | HV _{OUT} 13 | 32 | Data In |
| 11 | HV _{OUT} 12 | 33 | Blanking |
| 12 | HV _{OUT} 11 | 34 | N/C |
| 13 | HV _{OUT} 10 | 35 | HV _{OUT} 32 |
| 14 | HV _{OUT} 9 | 36 | HV _{OUT} 31 |
| 15 | HV _{OUT} 8 | 37 | HV _{OUT} 30 |
| 16 | HV _{OUT} 7 | 38 | HV _{OUT} 29 |
| 17 | HV _{OUT} 6 | 39 | HV _{OUT} 28 |
| 18 | HV _{OUT} 5 | 40 | HV _{OUT} 27 |
| 19 | HV _{OUT} 4 | 41 | HV _{OUT} 26 |
| 20 | HV _{OUT} 3 | 42 | HV _{OUT} 25 |
| 21 | HV _{OUT} 2 | 43 | HV _{OUT} 24 |
| 22 | HV _{OUT} 1 | 44 | HV _{OUT} 23 |

44-Lead PLCC Package Outline (PJ)

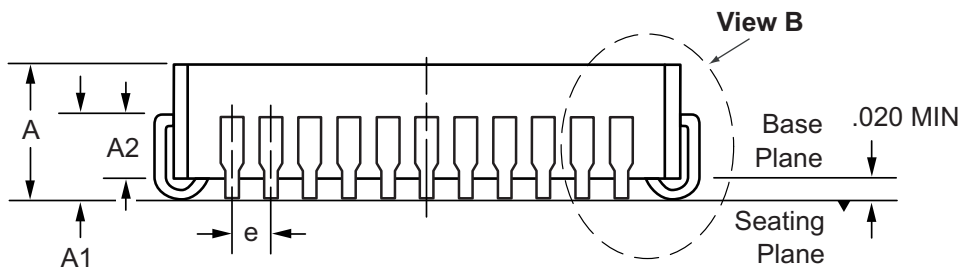
.653x.653in body, .180in height (max.), .050in pitch



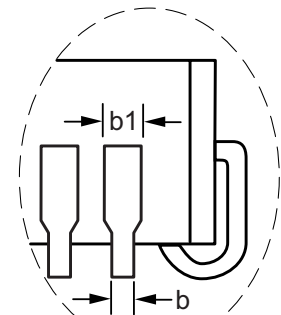
Top View



Side View



Side View



View B

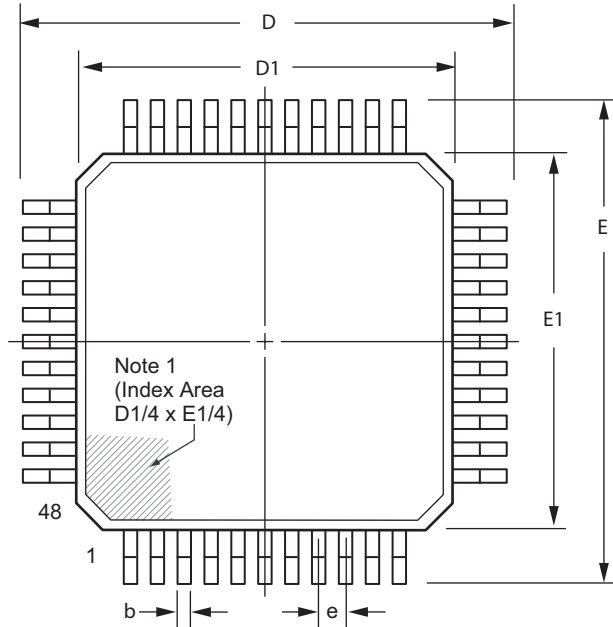
- Note:**
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
 2. Exact shape of this feature is optional.

| Symbol | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | |
|--------------------|-----|------|------|------|------|------|------|------|------|------|-------------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .050 BSC |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | |
| | MAX | .180 | .120 | .083 | .021 | .036 | .695 | .656 | .695 | .656 | |

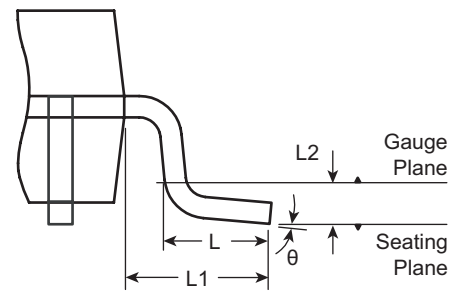
JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
 Drawings are not to scale.

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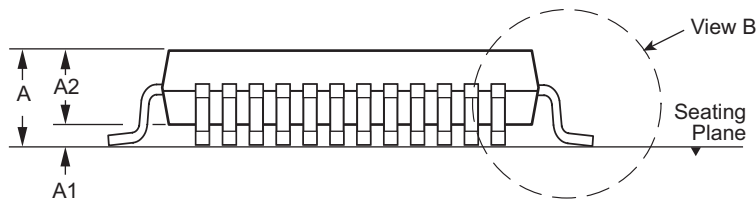
44-Lead PQFP Package Outline (PG)



Top View



View B



Side View

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | $\theta 1$ | |
|----------------|-----|------|------|------|------|-------|-------|-------|-------|----------|------|----------|----------|------------|-----|
| Dimension (mm) | MIN | - | 0.25 | 1.95 | 0.30 | 13.65 | 9.80 | 13.65 | 9.80 | 0.80 BSC | 0.73 | 1.95 REF | 0.25 BSC | 3.5° | 5° |
| | NOM | - | - | 2.00 | - | 13.90 | 10.00 | 13.90 | 10.00 | | 0.88 | | | - | - |
| | MAX | 2.45 | - | 2.10 | 0.45 | 14.15 | 10.20 | 14.15 | 10.20 | | 1.03 | | | 7° | 16° |

JEDEC Registration M0-112, Variation AA-2, Issue B, Sep. 1995.

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