Tri-EL Lamp Driver IC

Features

- Tri-EL lamp driver with common terminal
- Independent brightness control for all 3 lamps
- 1.8V to 6.5V Operating Supply Voltage
- Output voltage regulation
- Two-pin serial data communication for control
- Linear brightness control with seven steps at constant efficiency
- 128kHz Fixed Switching Frequency
- Split supply capability
- Patented high efficiency EL lamp driver
- Single miniature inductor drives all 3 lamps
- Only 4 external components
- Burst mode power converter for best efficiency
- CMOS compatible serial interface with noise rejection
- 150nA max. leakage current when disabled
- Power-on reset causes all outputs to be off when first powered up
- Small 10-pin MSOP package
- 10-pin DFN/MLP package (0.8mm thickness)

Applications

- Mulit-segment, variable displays
- Cell phone keypads and displays
- MP3 players
- Watches

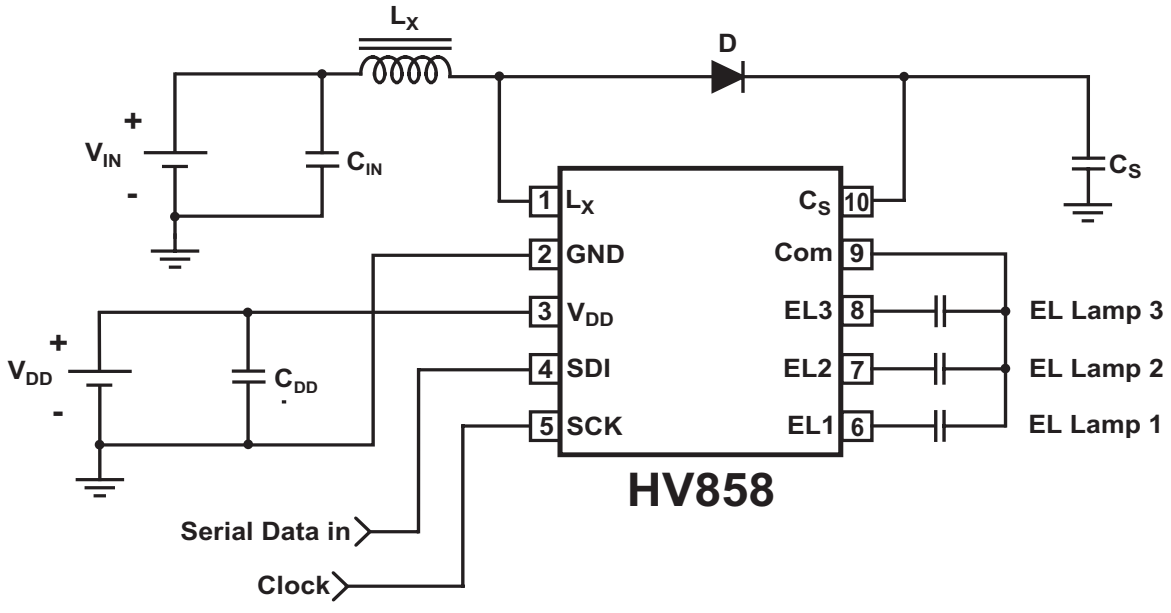
General Description

The Supertex HV858 is a high voltage triple EL lamp driver designed for driving combined EL lamps of up to 3.0 in^2 (1.0 in^2 each). The input supply voltage range is from 1.8V to 6.5V. The device is designed such that the input voltage to the inductor can be different from the input voltage to the device (split supply). The device uses a single inductor and a minimum number of passive components. The nominal regulated output voltage that is applied to the EL lamp is ±95V. The HV858 has two internal oscillators, one for the internal switching MOSFET, and the other for the high voltage EL lamp driver. The EL lamp frequency is fixed internally at 500Hz. The power converter oscillator runs 256 times faster than the EL lamp driver at 128kHz.

An external inductor is connected between the L_X and V_{DD} pins (or between the L_X pin and separate voltage source in the case of a split supply application). A 0.002-0.01µF, 100V capacitor is connected between the C_s pin and ground. The switching MOSFET charges the external inductor and discharges it into the capacitor at the C_s pin. The voltage at C_s will start to increase. Once the voltage at C_s reaches a nominal value of 95V, the switching MOSFET is turned OFF to conserve power.

One side of the 3 EL lamps is connected to the Com pin of HV858 and the other side to the EL1, EL2, and EL3 pins of the HV858. Each EL lamp output may be independently controlled to have one of the 7 brightness levels or can be completely turned OFF by a 10-bit serial data input register. The 10-bit control code has 3 bits to control the brightness level of each EL Lamp and one bit to optionally control the power converter. The 3-bit binary brightness control code controls the number of 500Hz cycles (from 0 to 7) in a group of 7 cycles.

Typical Application Circuit



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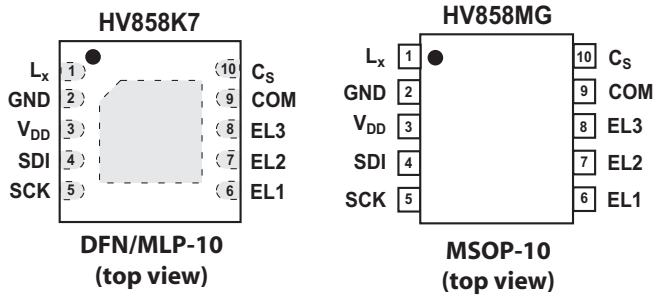
Ordering Information

Device	Package Options		
HV858	DFN/MLP-10	MSOP-10	
	HV858K7-G	HV858MG	HV858MG-G

-G indicates the package is RoHS compliant - "Green"

Pin Configuration



Absolute Maximum Ratings

V_{DD}	-0.5 to +7V
SDI, SCK	-0.5 to +7V
I_{SW}	0.7A peak
V_{CS}	0.5 to +110V
Power dissipation	250mW
Storage temperature	-65ºC to +150ºC
Operating temperature	-40ºC to +85ºC

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	Supply voltage	1.8		6.5	V	
$I_{SW(pk)}$	Peak switch current			0.4	A	
T_A	Operating temperature	-40		85	ºC	

Specifications *(unless otherwise specified: T_A = 25ºC, V_{DD} = 2.6V to 5.5V)*

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
R_{SW}	ON resistance of switching transistor		4	6	Ω	V_{DD} = 1.8 to 6.5V, I_{SW} = 100mA
V_{CS}	Output voltage	85	95	105	V	S1...S9 = 0, V_{DD} = 1.8 to 6.5V, no load
V_{LAMP}	Differential lamp voltage	170	190	210	V	V_{COM} to any EL, no load, code[1] = 111
I_{DD}	V_{DD} supply current	0.01	0.15	0.25	mA	V_{CS} = 20V, no load, PWR_ON = 1
I_{CS}	V_{CS} supply current	10	50	100	µA	V_{CS} = 75V, no load
I_{DDQ}	V_{DD} leakage current when disabled		100	150	nA	S1...S9 = 0, SCK and SDI can be tied to V_{DD} or GROUND
f_{SW}	Inductor switching frequency	108.8	128	147.2	kHz	See Figure 1
f_{EL}	Lamp frequency	425	500	575	Hz	For all codes except code[1] = 000
V_{LOW}	Logic pin input Low level	-0.5	0	0.2 V_{DD}	V	
V_{HIGH}	Logic pin input High level	0.8 V_{DD}	V_{DD}	V_{DD} + 0.5	V	
I_{LOGIC}	Logic pin input current	-0.1	0	0.1	µA	0 < V_{DD}< 7V
I_{DD}	Inductor current		56	70	mA	See Figure 1. V_{DD} = V_{IN} = 3V, total lamp size = 3.0in² (1.0in² each), 10-bit SDI serial code = 1111111111
V_{CS}	Output voltage		82.5		V	
f_{EL}	Lamp frequency		500		Hz	
D_{MAX}	Maximum PWM switch duty cycle	80	88	94	%	V_{CS} = 20V, R_{LOAD} = 20Ω
f_{CLK}	SCK speed			1	MHz	
T_{SU}	SDI setup time before SCK rises	30			ns	
T_H	SDI hold time before SCK rises	30			ns	

Note 1: Code refers to the 3-bit Brightness Control Code for the respective EL Lamp

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Pin Configuration

Pin	Name	Description
1	L_X	Inductor pin
2	GND	Ground pin
3	V_{DD}	Input voltage supply pin. It is common practice to use a bypass capacitor as close as possible to the device on this pin.
4	SDI	Serial data input pin
5	SCK	Serial clock input pin
6	EL1	EL lamp 1 pin
7	EL2	EL lamp 2 pin
8	EL3	EL lamp 3 pin
9	COM	Common pin for one side of all 3 EL lamps
10	C_S	High Voltage capacitor pin

Logic Input Conditions

The serial data input consists of a 10-bit string, 3-bits of brightness control and one bit(10^{th} bit) to optionally control the power converter. The power converter runs if any of the EL lamps has a non-zero brightness value or if the PWR_ON bit is high while the other 9 bits are low.

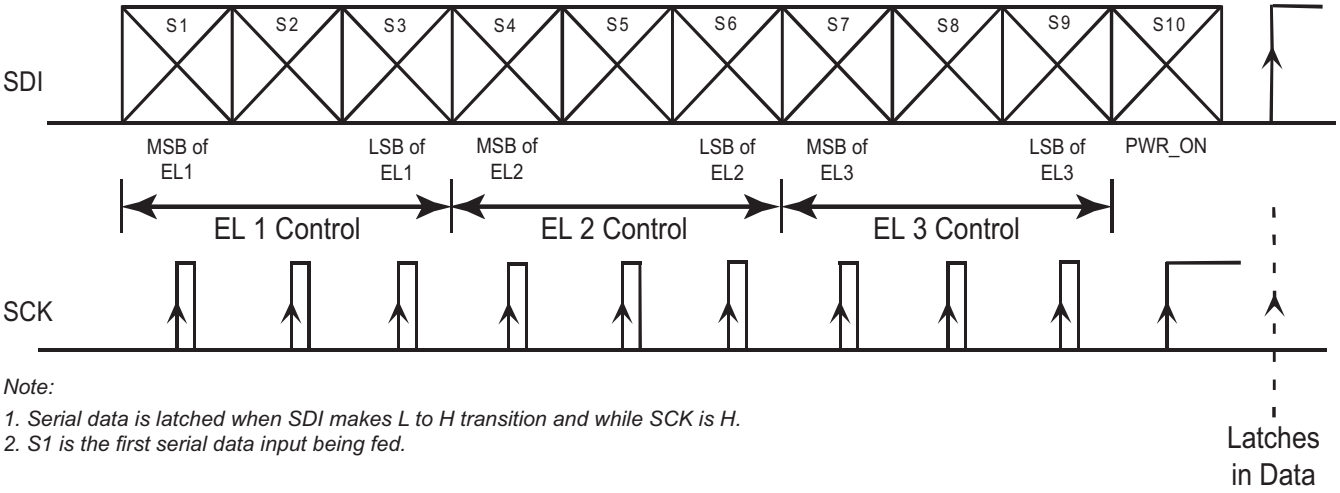
1. SDI may be H or L if SCK is H.
2. SCK may be H or L if SDI is H.
3. While inputting serial data to the shift register, SDI can change value only when SCK is L.
4. The previous 10 bits of serial input will be latched when SDI makes L to H transition while SCK is H.

EL Lamp Brightness Control

The EL Lamp brightness control is a 3-bit binary number stored in a latch, which is provided by a serial to parallel conversion shift register.

1. If all the 3 bits for a designated EL lamp are L, the differential voltage across that lamp will be zero.
2. If any of the 3 bits for a designated EL lamp is H:
   a. The 3-bit value sets the average number of cycles for which the EL lamp voltage is non-zero.
   b. The EL lamp brightness is linearly proportional to the binary lamp control code.

Logic Input Diagram



Note:

1. Serial data is latched when SDI makes L to H transition and while SCK is H.
2. S1 is the first serial data input being fed.

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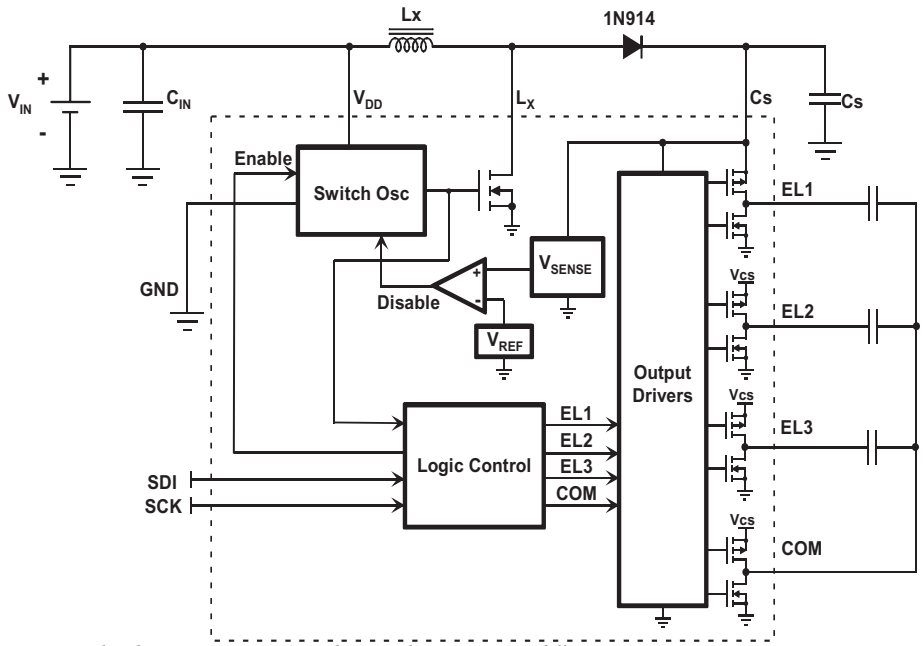
Logic Truth Table

L = Low (L = 0 to L < 20% of V_{DD})
H = High (80% of V_{DD} < H = V_{DD})
NA = Does not control brightness of the designated EL lamp

	Brightness Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
Device disabled	All lamps Off	L	L	L	L	L	L	L	L	L	L
Device enabled		L	L	L	L	L	L	L	L	L	H
EL1	7/7	H	H	H	NA	NA	NA	NA	NA	NA	NA
	6/7	H	H	L	NA	NA	NA	NA	NA	NA	NA
	5/7	H	L	H	NA	NA	NA	NA	NA	NA	NA
	4/7	H	L	L	NA	NA	NA	NA	NA	NA	NA
	3/7	L	H	H	NA	NA	NA	NA	NA	NA	NA
	2/7	L	H	L	NA	NA	NA	NA	NA	NA	NA
	1/7	L	L	H	NA	NA	NA	NA	NA	NA	NA
	Off	L	L	L	NA	NA	NA	NA	NA	NA	NA
EL2	7/7	NA	NA	NA	H	H	H	NA	NA	NA	NA
	6/7	NA	NA	NA	H	H	L	NA	NA	NA	NA
	5/7	NA	NA	NA	H	L	H	NA	NA	NA	NA
	4/7	NA	NA	NA	H	L	L	NA	NA	NA	NA
	3/7	NA	NA	NA	L	H	H	NA	NA	NA	NA
	2/7	NA	NA	NA	L	H	L	NA	NA	NA	NA
	1/7	NA	NA	NA	L	L	H	NA	NA	NA	NA
	Off	NA	NA	NA	L	L	L	NA	NA	NA	NA
EL3	7/7	NA	NA	NA	NA	NA	NA	H	H	H	NA
	6/7	NA	NA	NA	NA	NA	NA	H	H	L	NA
	5/7	NA	NA	NA	NA	NA	NA	H	L	H	NA
	4/7	NA	NA	NA	NA	NA	NA	H	L	L	NA
	3/7	NA	NA	NA	NA	NA	NA	L	H	H	NA
	2/7	NA	NA	NA	NA	NA	NA	L	H	L	NA
	1/7	NA	NA	NA	NA	NA	NA	L	L	H	NA
	Off	NA	NA	NA	NA	NA	NA	L	L	L	NA

Functional Block Diagram



Note: This drawing is a generalized representation. Actual internal circuitry may differ.

Differential Output Waveform

The following is the differential output waveform across the lamp for each 3-bit input code for each lamp.

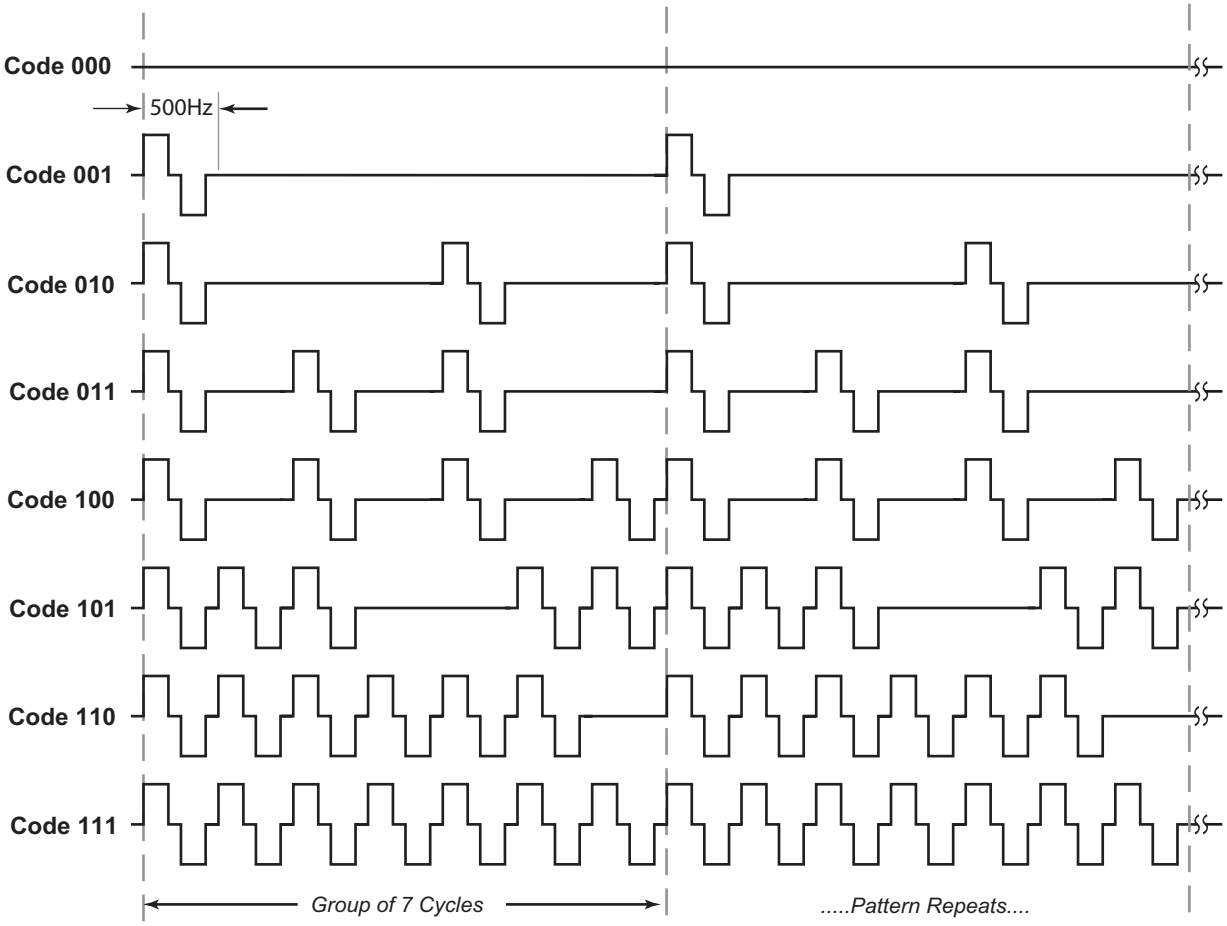


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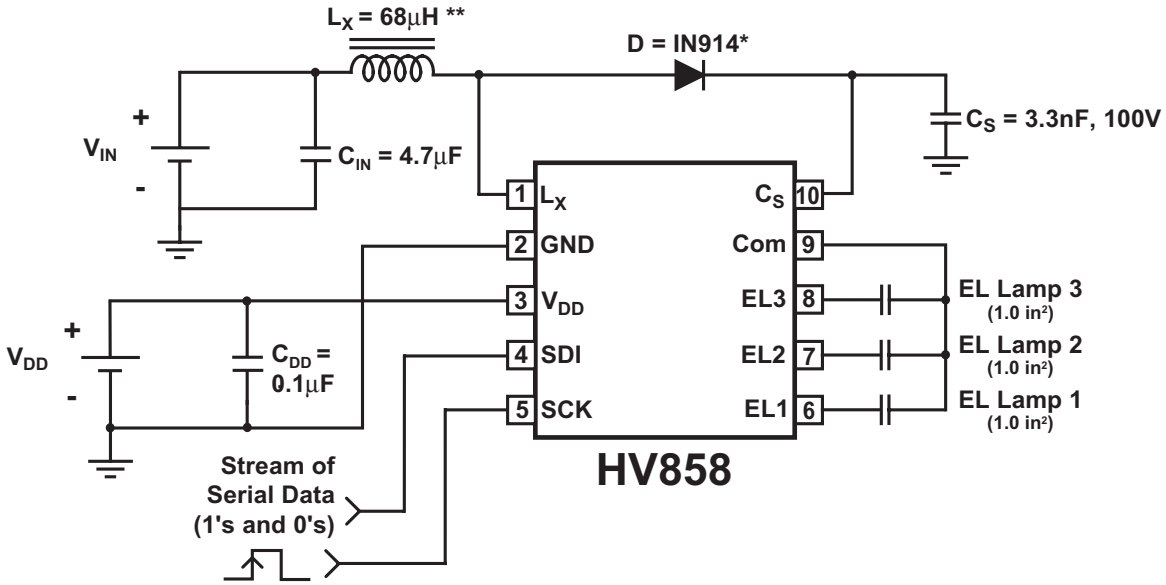
Figure 1 : Test Circuit



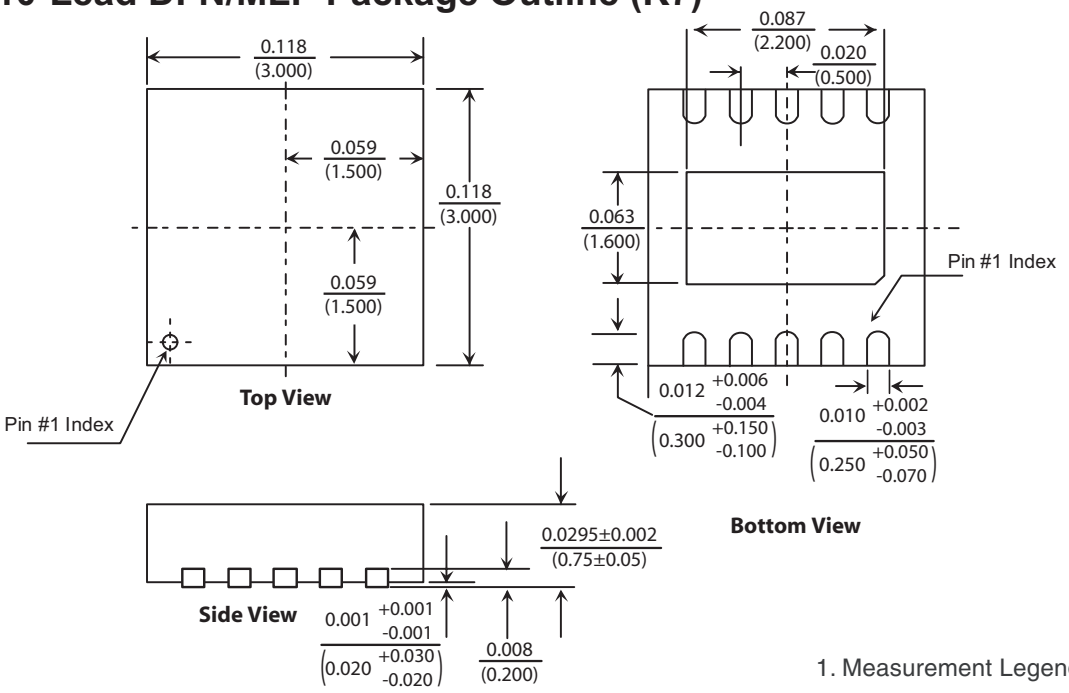
**Any 100V fast reverse recovery diode can be used*

Note: Maximum lamp size for each segment is 1.0 in². To drive larger size lamps, any combination of EL1, EL2 and EL3 can be paralleled. However, the 3-bit serial data input code (for each output) should be such that the paralleled outputs have the same code.

Typical Performance *(V_{DD} = V_{IN} = 3.0V)*

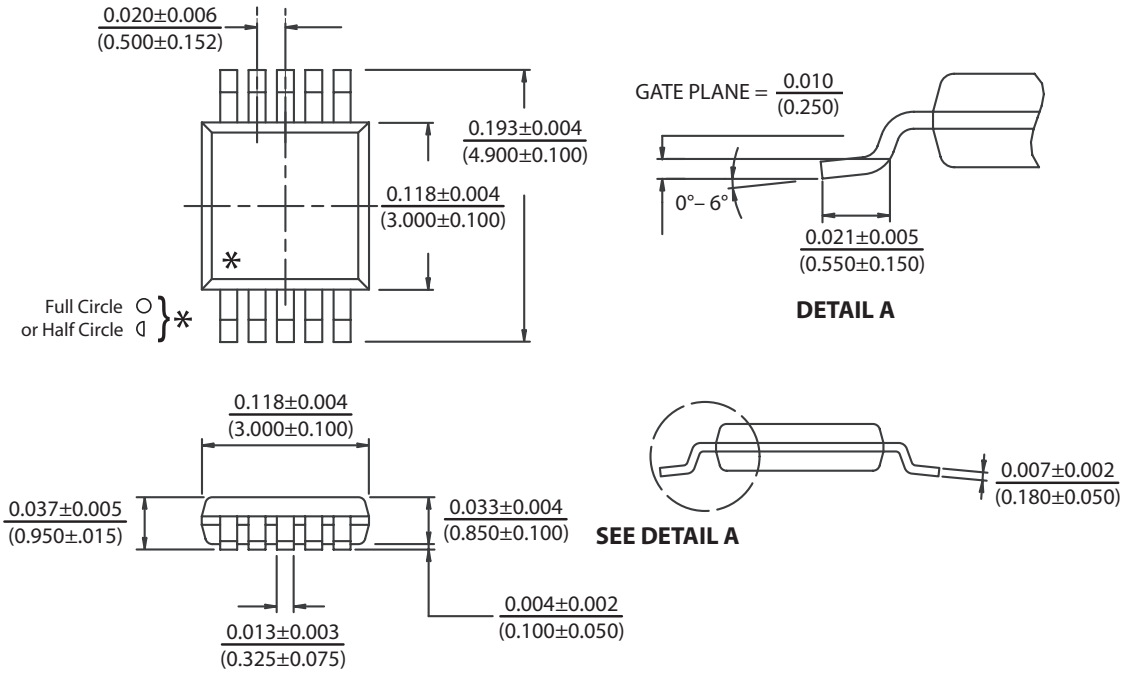
1st 9-bit SDI code	EL1 Brightness			I_{DD} (mA)	V_{CS} (V)
	Level	ft-lm	Cd/m²		
000111111	0/7	0	0	42.6	85.7
001111111	1/7	1.60	5.46	44.7	85.3
010111111	2/7	3.24	11.08	46.9	84.9
011111111	3/7	4.95	16.94	48.9	84.5
100111111	4/7	6.68	22.85	51.2	84.0
101111111	5/7	8.44	28.85	53.3	83.5
110111111	6/7	10.21	34.93	55.0	82.9
111111111	7/7	12.05	41.2	56.2	82.5

10-Lead DFN/MLP Package Outline (K7)



1. Measurement Legend = Dimensions in Inches / (Dimensions in Millimeters)
2. MLP Package dimensions conform to JEDEC MO-229

10-Lead MSOP Package Outline (MG)



Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com