

High-Voltage Current-Mode PWM Controller

Features

- Input Voltage Range of V_{DD} Regulator
 - HV9110: 10V to 120V
 - HV9112: 9V to 80V
 - HV9113: 10V to 120V
- Maximum Duty, Feedback Accuracy
 - HV9110: 49%, 1%
 - HV9112: 49%, 2%
 - HV9113: 99%, 1%
- Current Mode Control
- <1 mA Supply Current
- >1 MHz clock

Applications

- DC/DC Power Converters

General Description

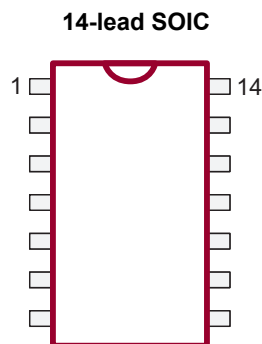
HV9110/HV9112/HV9113 are Switch-Mode Power Supply (SMPS) controllers suitable for the control of a variety of converter topologies, including the flyback converter and the forward converter.

The V_{DD} regulator supports an input voltage as high as 80V or 120V.

HV9110/HV9112/HV9113 controllers include all essentials for a power converter design, such as a bandgap reference, an error amplifier, a ramp generator, a high-speed PWM comparator, and a gate driver. A shutdown latch provides on/off control.

The HV9110 and HV9113 feature an input voltage range of 10V to 120V, and the HV9112 has an input voltage range of 9V to 80V. The HV9110 and HV9112 have a maximum duty of 49%, while the HV9113 has a maximum duty of 99%.

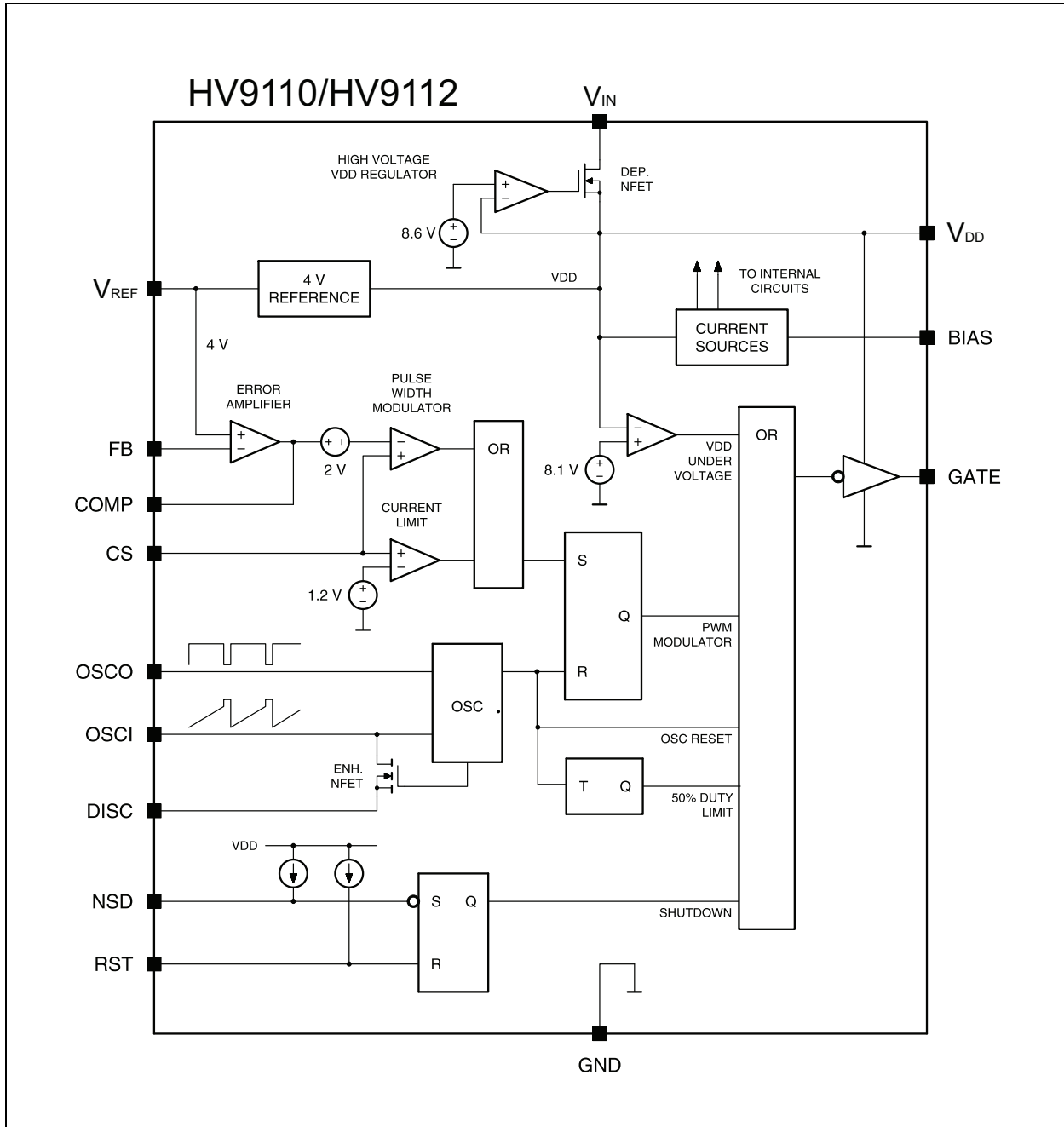
Package Type



See [Table 3-1](#) for pin information.

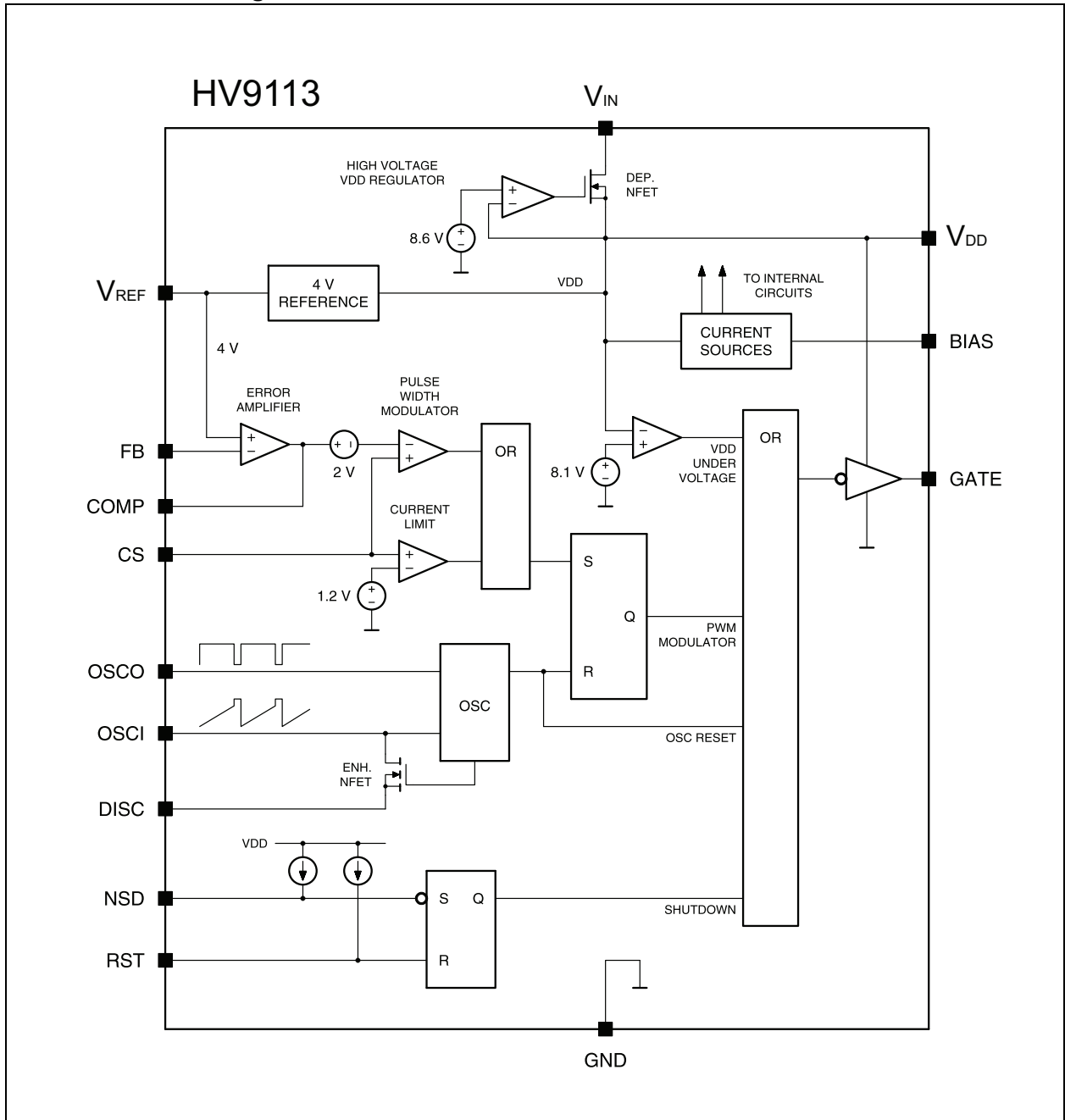
HV9110/HV9112/HV9113

Functional Block Diagram



HV9110/HV9112/HV9113

Functional Block Diagram



HV9110/HV9112/HV9113

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

| | |
|---------------------------------------|--------------------------|
| Input Voltage, V_{IN} | |
| HV9110/HV9113 | 120V |
| HV9112 | 80V |
| Device Supply Voltage, V_{DD} | 15.5V |
| Logic Input Voltage Range | -0.3V to $V_{DD} + 0.3V$ |
| Linear Input Voltage Range | -0.3V to $V_{DD} + 0.3V$ |
| Storage Temperature Range | -65°C to +150°C |
| Operating Temperature Range | -55°C to +125°C |
| Power Dissipation: 14-lead SOIC | 750 mW |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

| Electrical Specifications: $V_{DD} = 10V$, $V_{IN} = 48V$, $V_{DISC} = 0V$, $R_{BIAS} = 390\text{ k}\Omega$, $R_{OSC} = 330\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted. | | | | | | | |
|--|---------------|------------------|------|------|------|-----------------------|--|
| Parameters | | Sym. | Min. | Typ. | Max. | Units | Conditions |
| REFERENCE | | | | | | | |
| Output Voltage | HV9110/13 | V_{REF} | 3.92 | 4 | 4.08 | V | $R_L = 10\text{ M}\Omega$ |
| | HV9112 | | 3.88 | 4 | 4.12 | | |
| | HV9110/13 | | 3.82 | 4 | 4.16 | | $R_L = 10\text{ M}\Omega$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| Output Impedance | | Z_{OUT} | 15 | 30 | 45 | k Ω | (Note 1) |
| Short Circuit Current | | I_{SHORT} | — | 125 | 250 | μA | $V_{REF} = \text{GND}$ |
| Change in V_{REF} with Temperature | | ΔV_{REF} | — | 0.25 | — | mV/ $^\circ\text{C}$ | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (Note 1) |
| OSCILLATOR | | | | | | | |
| Oscillator Frequency | | f_{MAX} | 1 | 3 | — | MHz | $R_{OSC} = 0\Omega$ |
| Initial Accuracy | | f_{OSC} | 80 | 100 | 120 | kHz | $R_{OSC} = 330\text{ k}\Omega$ (Note) |
| | | | 160 | 200 | 240 | | $R_{OSC} = 150\text{ k}\Omega$ (Note) |
| V_{DD} Regulation | | — | — | — | 15 | % | $9.5V < V_{DD} < 13.5V$ |
| Temperature Coefficient | | — | — | 170 | — | ppm/ $^\circ\text{C}$ | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (Note 1) |
| PWM | | | | | | | |
| Maximum Duty Cycle | HV9110/HV9112 | D_{MAX} | 49 | 49.4 | 49.6 | % | (Note 1) |
| | HV9113 | | 95 | 97 | 99 | | |
| Dead Time | HV9113 | D_{MIN} | — | 225 | — | ns | HV9113 only (Note 1) |
| Minimum Duty Cycle | | | — | — | 0 | % | |
| Pulse Width where Pulse drops out | | | — | 80 | 125 | ns | (Note 1) |
| CURRENT LIMIT | | | | | | | |
| Maximum Input Signal | | V_{LIM} | 1 | 1.2 | 1.4 | V | $V_{FB} = 0V$ |
| Delay to Output | | t_D | — | 80 | 120 | ns | $V_{CS} = 1.5V$, $V_{COMP} \leq 2V$ (Note 1) |

HV9110/HV9112/HV9113

ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical Specifications: $V_{DD} = 10V$, $V_{IN} = 48V$, $V_{DISC} = 0V$, $R_{BIAS} = 390\text{ k}\Omega$, $R_{OSC} = 330\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted. | | | | | | | |
|--|--------------|--------------------|---------------|------|---------------|---|--|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
| ERROR AMPLIFIER | | | | | | | |
| Feedback Voltage | HV9110/13 | V_{FB} | 3.96 | 4 | 4.04 | V | V_{FB} shorted to COMP |
| | HV9112 | | 3.92 | 4 | 4.08 | | |
| Input Bias Current | I_{IN} | — | 25 | 500 | nA | $V_{FB} = 4V$ | |
| Input Offset Voltage | V_{OS} | Nulled during trim | | | — | | |
| Open-loop Voltage Gain | A_{VOL} | 60 | 80 | — | dB | (Note 1) | |
| Unity Gain Bandwidth | GB | 1 | 1.3 | — | MHz | (Note 1) | |
| Output Source Current | I_{SOURCE} | -1.4 | -2 | — | mA | $V_{FB} = 3.4V$ | |
| Output Sink Current | I_{SINK} | 0.12 | 0.15 | — | mA | $V_{FB} = 4.5V$ | |
| HIGH-VOLTAGE REGULATOR AND START-UP | | | | | | | |
| Input Voltage | HV9110/13 | V_{IN} | — | — | 120 | V | $I_{IN} < 10\text{ }\mu\text{A}$; $V_{CC} > 9.4V$ |
| | HV9112 | | — | — | 80 | | |
| Input Leakage Current | I_{IN} | — | — | 10 | μA | $V_{DD} > 9.4V$ | |
| Regulator Turn-off Threshold Voltage | V_{TH} | 8 | 8.7 | 9.4 | V | $I_{IN} = 10\text{ }\mu\text{A}$ | |
| Undervoltage Lockout | V_{LOCK} | 7 | 8.1 | 8.9 | V | | |
| SUPPLY | | | | | | | |
| Supply Current | I_{DD} | — | 0.75 | 1 | mA | $C_L < 75\text{ pF}$ | |
| Quiescent Supply Current | I_Q | — | 0.55 | — | mA | $V_{NSD} = 0V$ | |
| Nominal Bias Current | I_{BIAS} | — | 20 | — | μA | | |
| Operating Range | V_{DD} | 9 | — | 13.5 | V | | |
| SHUTDOWN LOGIC | | | | | | | |
| Shutdown Delay | t_{SD} | — | 50 | 100 | ns | $C_L = 500\text{ pF}$, $V_{CS} = 0V$ (Note 1) | |
| NSD Pulse Width | t_{SW} | 50 | — | — | ns | (Note 1) | |
| RST Pulse Width | t_{RW} | 50 | — | — | ns | (Note 1) | |
| Latching Pulse Width | t_{LW} | 25 | — | — | ns | V_{NSD} , $V_{RST} = 0V$ (Note 1) | |
| Input Low Voltage | V_{IL} | — | — | 2 | V | | |
| Input High Voltage | V_{IH} | 7 | — | — | V | | |
| Input Current, Input High Voltage | I_{IH} | — | 1 | 5 | μA | $V_{IN} = V_{DD}$ | |
| Input Current, Input Low Voltage | I_{IL} | — | -25 | -35 | μA | $V_{IN} = 0V$ | |
| OUTPUT | | | | | | | |
| Output High Voltage | HV9110/13 | V_{OH} | $V_{DD}-0.25$ | — | — | V | $I_{OUT} = 10\text{ mA}$ |
| | HV9112 | | $V_{DD}-0.3$ | — | — | | |
| | HV9110/13 | | $V_{DD}-0.3$ | — | — | | |
| Output Low Voltage | All | V_{OL} | — | — | 0.2 | V | $I_{OUT} = -10\text{ mA}$ |
| | HV9110/13 | | — | — | 0.3 | | |
| Output Resistance | Pull up | R_{OUT} | — | 15 | 25 | Ω | $I_{OUT} = \pm 10\text{ mA}$ |
| | Pull down | | — | 8 | 20 | | |
| | Pull up | | — | 20 | 30 | Ω | |
| | Pull down | | — | 10 | 30 | | |
| Rise Time | t_R | — | 30 | 75 | ns | $C_L = 500\text{ pF}$ (Note 1) | |
| Fall Time | t_F | — | 20 | 75 | ns | $C_L = 500\text{ pF}$ (Note 1) | |

Note 1: Design guidance only; Not 100% tested in production.
Note 2: Stray capacitance on OSC input pin must be $\leq 5\text{ pF}$.

HV9110/HV9112/HV9113

TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------|---------------|------|------|------|-------|------------|
| TEMPERATURE RANGES | | | | | | |
| Operating Temperature | — | -55 | — | 125 | °C | |
| Storage Temperature | — | -65 | — | 150 | °C | |
| PACKAGE THERMAL RESISTANCE | | | | | | |
| 14-lead SOIC | θ_{ja} | — | 83 | — | °C/W | |

1.1 Truth Table

TRUTH TABLE

| SHUTDOWN | RESET | OUTPUT |
|----------|-------|-----------------------------|
| H | H | Normal operation |
| H | H → L | Normal operation, no change |
| L | H | Off, not latched |
| L | L | Off, latched |
| L → H | L | Off, latched, no change |

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

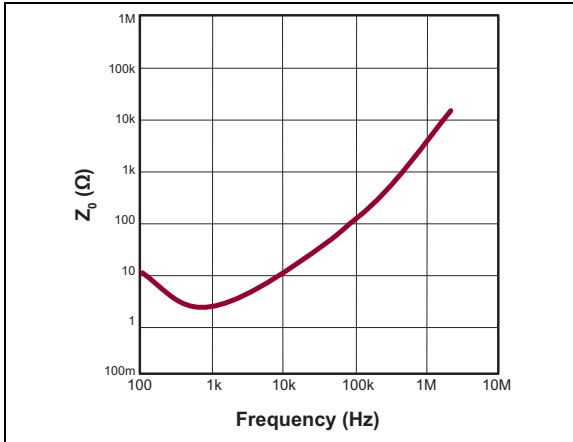


FIGURE 2-1: Error Amplifier Output Impedance (Z_o).

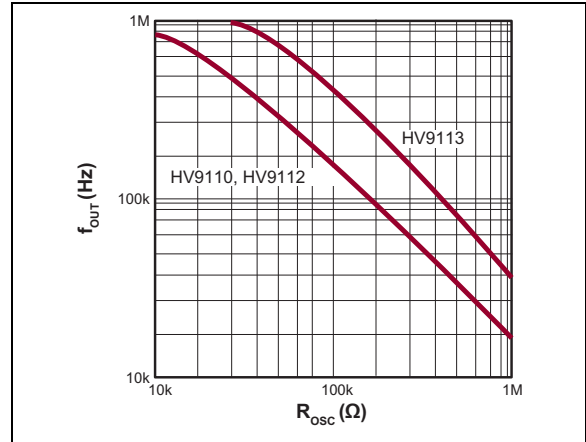


FIGURE 2-4: Output Switching Frequency vs. Oscillator Resistance.

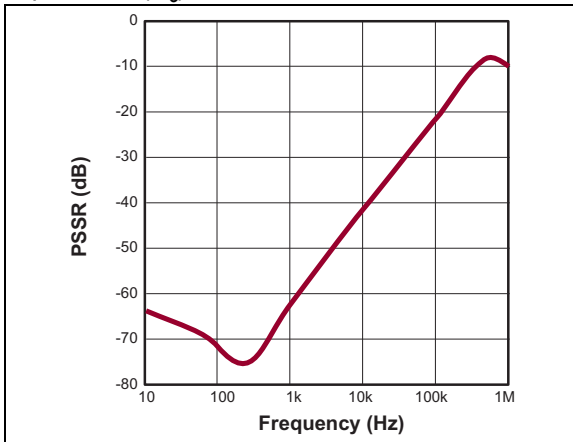


FIGURE 2-2: PSRR - Error Amplifier and Reference.

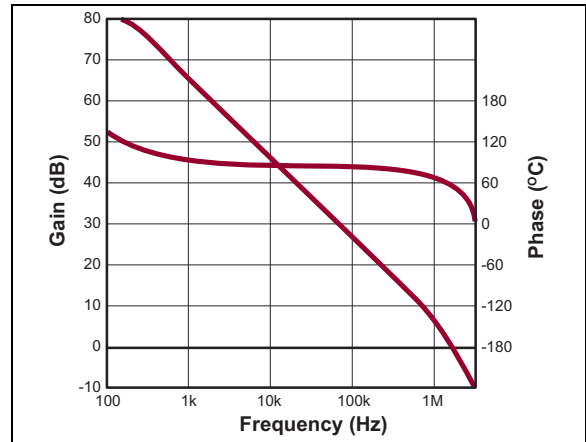


FIGURE 2-5: Error Amplifier Open-loop Gain/Phase.

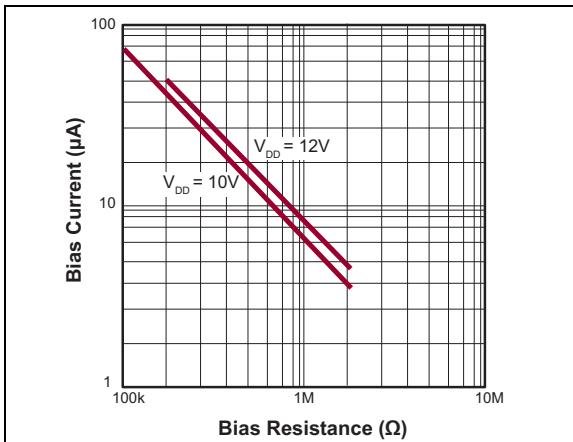


FIGURE 2-3: Bias Current vs. Bias Resistance.

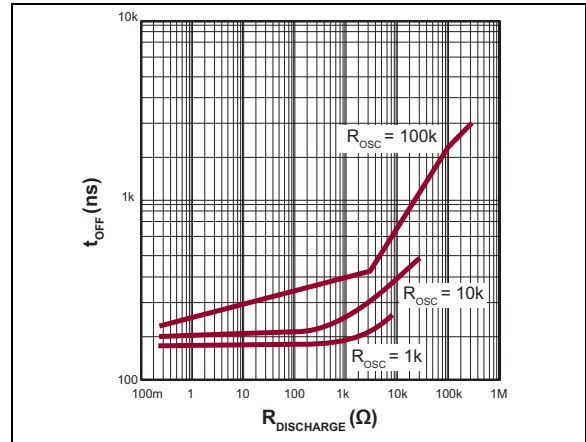


FIGURE 2-6: $R_{DISCHARGE}$ vs. t_{OFF} (HV9113 only).

HV9110/HV9112/HV9113

3.0 PIN DESCRIPTION

Table 3-1 shows the pin description for HV9110/HV9112/HV9113. The locations of the pins are listed in [Features](#).

TABLE 3-1: PIN DESCRIPTION

| Pin Number | HV9110/HV9112/HV9113 Pin Name | Description |
|------------|----------------------------------|---|
| 1 | BIAS | Internal bias, current set |
| 2 | V _{IN} | High-voltage V _{DD} regulator input |
| 3 | CS | Current sense input |
| 4 | GATE | Gate drive output |
| 5 | GND | Ground |
| 6 | V _{DD} | High-voltage V _{DD} regulator output |
| 7 | OSCO | Oscillator output |
| 8 | OSCI | Oscillator input |
| 9 | DISC | Oscillator discharge, current set |
| 10 | V _{REF} | 4V reference output Reference voltage level can be overridden by an externally applied voltage source. |
| 11 | NSD | Active low input to set shutdown latch |
| 12 | RST | Active high input to reset shutdown latch |
| 13 | COMP | Error amplifier output |
| 14 | FB | Feedback voltage input |

4.0 TEST CIRCUITS

The test circuits for characterizing error amplifier output impedance, Z_{OUT} , and error amplifier, power supply rejection ratio, PSRR, are shown in Figure 4-1 and Figure 4-2.

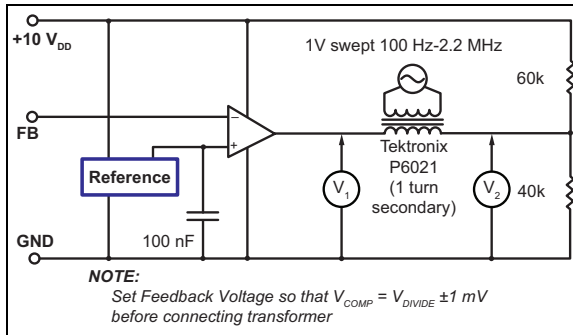


FIGURE 4-1: Error Amp Z_{OUT}

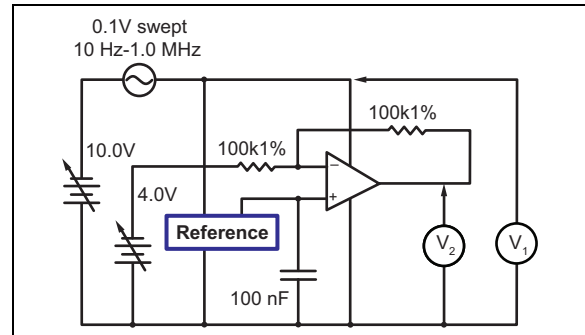


FIGURE 4-2: PSRR.

HV9110/HV9112/HV9113

5.0 DETAILED DESCRIPTION

5.1 High-Voltage Regulator

The high-voltage regulator included in HV9110/HV9112/HV9113 consists of a high-voltage N-channel Depletion-mode DMOS transistor driven by an error amplifier, providing a current path between the V_{IN} terminal and the V_{DD} terminal. The maximum current, about 20 mA, occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off when V_{DD} rises to somewhere between 8V and 9.4V. So, if V_{DD} is held at 10V or 12V by an external source, no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation within the high-voltage regulator.

Use an external capacitor between V_{DD} and GND. This capacitor should have good high-frequency characteristics. Ceramic caps work well.

The device uses a compound resistor divider to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high-voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout releases before the FET shuts off.

5.2 Bias Circuit

HV9110/HV9112/HV9113 require an external bias resistor, connected between the Bias pin and GND, to set currents in a series of current mirrors used by the analog sections of the chip. The nominal external bias current requirement is 15 μ A to 20 μ A, which can be set by a 390 k Ω to 510 k Ω resistor if $V_{DD} = 10$ V, or a 510 k Ω to 680 k Ω resistor if $V_{DD} = 12$ V. A precision resistor is not required, $\pm 5\%$ meets device requirements.

5.3 Clock Oscillator

The clock oscillator of the HV9110/HV9112/HV9113 consists of a ring of CMOS inverters, timing capacitors, and a capacitor-discharge FET. A single external resistor between the OSCI and OSCO sets the oscillator frequency. (See [Figure 2-4](#).)

The HV9110 and HV9112 include a frequency-dividing flip-flop that allows the part to operate with a 50% duty limit. Accordingly, the effective switching frequency of the power converter is half the oscillator frequency. (See [Figure 2-4](#).)

An internal discharge FET resets the oscillator ramp at the end of the oscillator cycle. The discharge FET is externally connected to GND, by way of a resistor. The resistor programs the oscillator dead time at the end of the oscillator period.

The oscillator turns off during shutdown to reduce supply current by about 150 μ A.

5.4 Reference

The reference of the HV9110/HV9112/HV9113 consists of a band-gap reference, followed by a buffer amplifier, which scales the voltage up to 4V. The scaling resistors of the buffer amplifier are trimmed during manufacture so that the output of the error amplifier, when connected in a gain of -1 configuration, is as close to 4V as possible. This nulls out the input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be 4V.

An approximately 50 k Ω resistor is located internally between the output of the reference buffer amplifier and the circuitry it feeds—reference output pin and non-inverting input to the error amplifier. This allows overriding the internal reference with a low impedance voltage source ≤ 6 V. Using an external reference reinstates the input offset voltage of the error amplifier. Overriding the reference should seldom be necessary.

The reference of the HV9110/HV9112/HV9113 is a high-impedance node, and usually there will be significant electrical noise nearby. Therefore, a bypass capacitor between the reference pin and GND is strongly recommended. The reference buffer amplifier is compensated to be stable with a capacitive load of 0.01 μ F to 0.1 μ F.

5.5 Error Amplifier

The error amplifier on HV9110/HV9112/HV9113 is a low-power, differential-input, operational amplifier. A PMOS input stage is used, so the common mode range includes ground and the input impedance is high.

5.6 Current Sense Comparators

The HV9110/HV9112/HV9113 use a dual-comparator system with independent comparators for modulation and current limiting. This provides the designer greater latitude in compensation design, as there are no clamps, except ESD protection, on the compensation pin.

5.7 Remote Shutdown

The NSD and RST pins control the shutdown latch. These pins have internal current-source pull-ups so they can be driven from open drain logic. When not used they should be left open or connected to V_{DD} .

5.8 Output Buffer

The output buffer of HV9110/HV9112/HV9113 is of standard CMOS construction P-channel pull-up and N-channel pull-down. Thus, the body-drain diodes of the output stage can be used for spike clipping. External Schottky diode clamping of the output is not required.

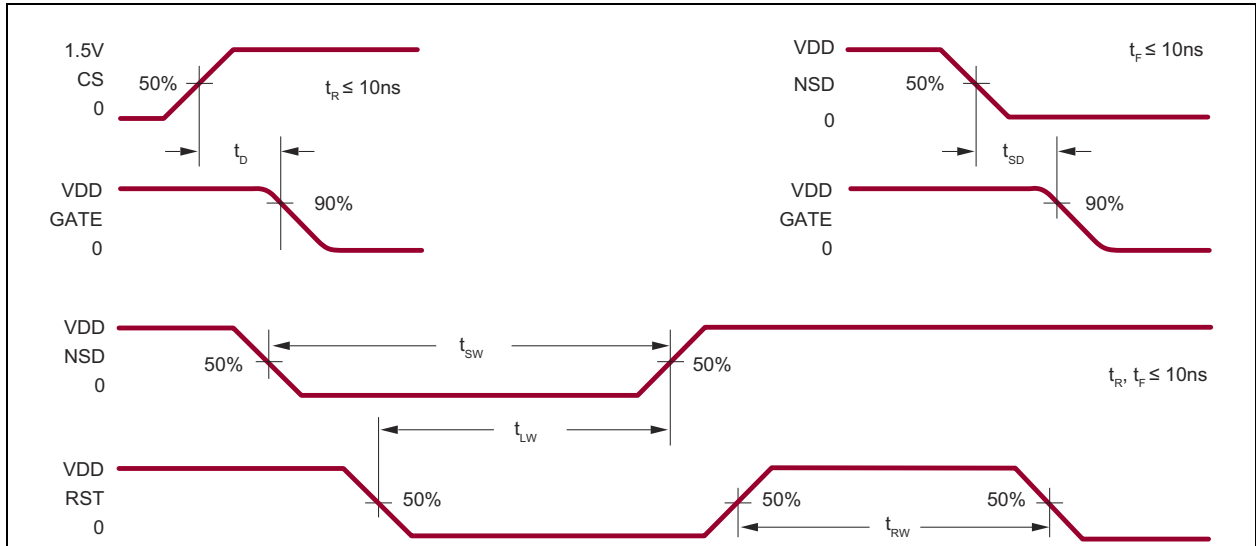
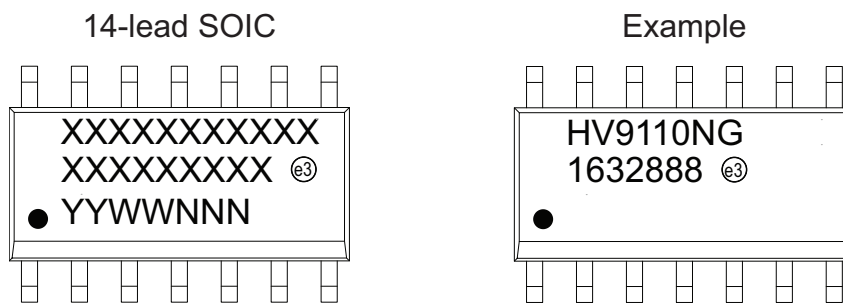


FIGURE 5-1: Shutdown Timing Waveforms.

HV9110/HV9112/HV9113

6.0 PACKAGING INFORMATION

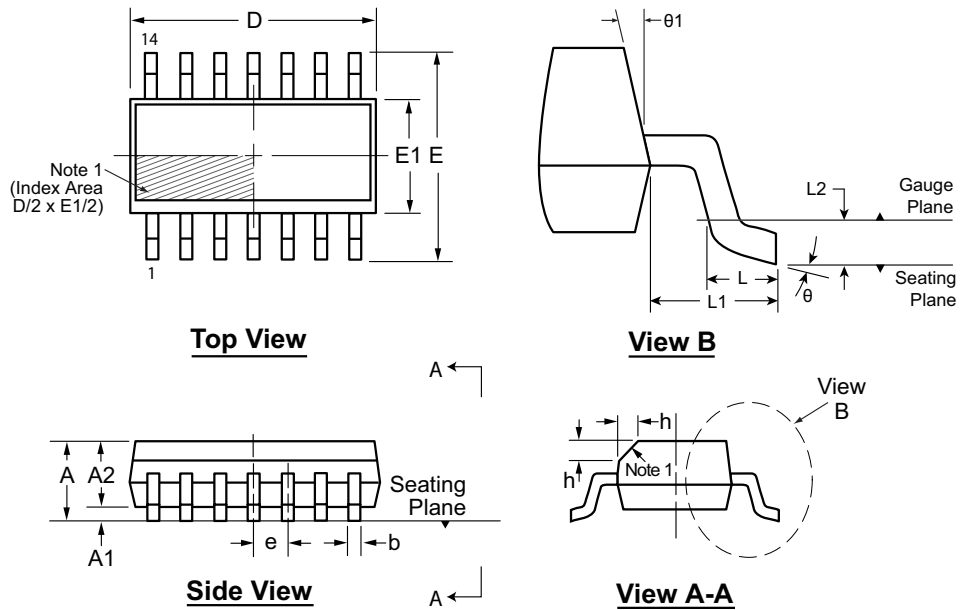
6.1 Package Marking Information



| | | |
|----------------|--------|--|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC [®] designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

14-Lead SOIC (Narrow Body) Package Outline (NG) 8.65x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | $\theta 1$ |
|----------------|-----|-------|------|-------|------|-------|-------|-------|----------|------|----------|----------|----------|------------|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 8.55* | 5.80* | 3.80* | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 8.65 | 6.00 | 3.90 | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 8.75* | 6.20* | 4.00* | 1.27 BSC | 1.27 | | | 8° | 15° |

JEDEC Registration MS-012, Variation AB, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

HV9110/HV9112/HV9113

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2016)

- Merged Supertex Doc #s DSFP-HV9110, DSFP-HV9112 and DSFP-DSFP-HV9113 to Microchip DS20005505A.
- Revised [Electrical Characteristics](#) to accommodate the merged products.
- Updated pin names to reflect new naming convention.
- Significant text changes to [Detailed Description](#).
- Minor text changes throughout.

HV9110/HV9112/HV9113

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>XX</u> | - | <u>X</u> | - | <u>X</u> |
|-----------------|-----------------|---|---|---|------------|
| Device | Package Options | | Environmental | | Media Type |
| Device: | HV9110 = | | High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 49% Duty Cycle | | |
| | HV9112 = | | High-voltage Current-mode PWM Controller, 9V to 80V Input Voltage Range, 49% Duty Cycle | | |
| | HV9113 = | | High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 99% Duty Cycle | | |
| Package: | NG | = | 14-lead SOIC | | |
| Environmental | G | = | Lead (Pb)-free/RoHS-compliant Package | | |
| Media Type: | (blank) | = | 53/Tube for an NG package | | |

Examples:

a) HV9110NG-G: High-voltage Current-mode PWM Controller 10V to 120V Input Voltage Range, 49% Duty Cycle, 14-lead SOIC Package, 53/Tube

b) HV9112NG-G: High-voltage Current-mode PWM Controller, 9V to 80V Input Voltage Range, 49% Duty Cycle, 14-lead SOIC Package, 53/Tube

c) HV9113NG-G: High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 99% Duty Cycle, 14-lead SOIC Package, 53/Tube

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