

## 4M × 32-Bit Dynamic RAM Module SMALL OUTLINE MEMORY MODULE

HYM 324000GD-50/-60

### Preliminary Information

- 4 0194 034 words by 32-bit organization
- Fast access and cycle time
  - 50 ns access time
  - 95 ns cycle time (-50 version)
  - 60 ns access time
  - 110 ns cycle time (-60 version)
- Fast page mode capability with
  - 35 ns cycle time (-50 version)
  - 40 ns cycle time (-60 version)
- Single + 3.3 V ( $\pm 0.3$  V) supply
- Low power dissipation
  - max. 1008 mW active (-50 version)
  - max. 864 mW active (-60 version)

LVC MOS – 1.8 mW standby  
TTL – 14.4 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only-refresh. Self Refresh
- 2 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 72 pin, dual read-out, one bank, Small Outline DIMM Module
- Utilizes two 4M × 16 -DRAMs (HYB 3165160T)
- 4096 refresh cycles / 64 ms
- Gold contact pad

The HYM 324000GD -50/-60 is a 16 MByte DRAM module organized as 4 194 304 words by 32-bit in a 72-pin, dual read-out, small outline package comprising two HYB 3165160T 4M×16 DRAMs in 500 mil wide TSOPII-54 - packages mounted together with two 0.2 μF ceramic decoupling capacitors on a PC board. Each HYB 3165160T is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

### Ordering Information

| Type             | Ordering Code | Package    | Descriptions      |
|------------------|---------------|------------|-------------------|
| HYM 324000GD -50 | on request    | L-DIM-72-1 | 50 ns DRAM module |
| HYM 324000GD -60 | on request    | L-DIM-72-1 | 60 ns DRAM module |

### Pin Names

|             |                       |
|-------------|-----------------------|
| A0-A11      | Row Address Input     |
| A0-A9       | Column Address Inputs |
| DQ0 - DQ31  | Data Input/Output     |
| RAS0, RAS2  | Row Address Strobe    |
| CAS0 - CAS3 | Column Address Strobe |
| WE          | Read / Write Input    |
| Vcc         | Power (+3.3 Volt)     |
| Vss         | Ground                |
| PD1 - PD7   | Presence Detect Pins  |
| N.C.        | No Connection         |

### Presence-Detect and ID-pin Thru Table \*):

| Module           | PD1 | PD2 | PD3 | PD4 | PD5 | PD6 | PD7 |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| HYM 324000GD -50 | NC  | NC  | VSS | NC  | VSS | VSS | NC  |
| HYM 324000GD -60 | NC  | NC  | VSS | NC  | NC  | NC  | NC  |

note: PD1 .. PD4 : configuration  
 PD5 .. PD6 : speed  
 PD7 : refresh mode (NC = normal refresh)

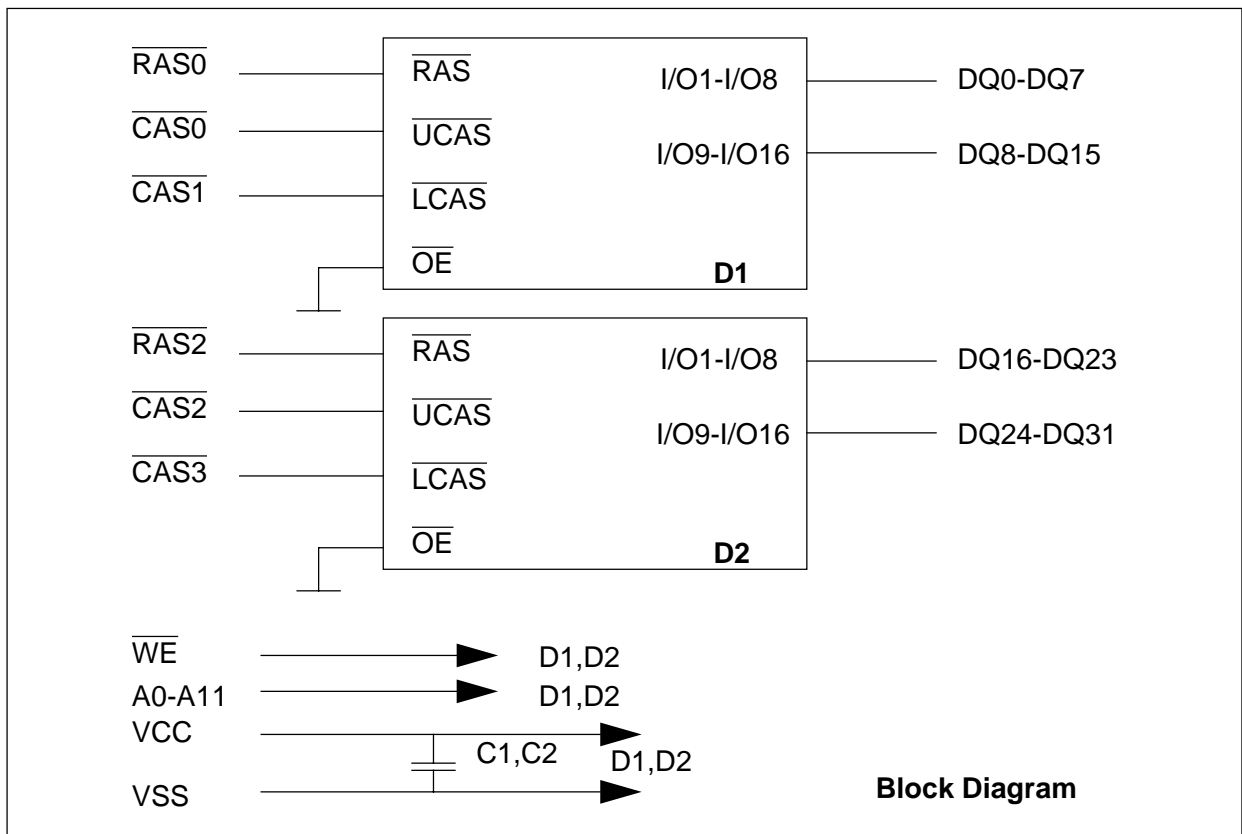
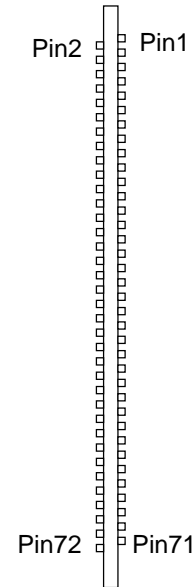
\*) according to JEDEC letter ballot JC-42.5-95 Item #646/651

### Pin Configuration

| PIN | Name | PIN | NAME  | PIN | NAME | PIN | NAME |
|-----|------|-----|-------|-----|------|-----|------|
| 1   | VSS  | 37  | DQ16  | 2   | DQ0  | 38  | DQ17 |
| 3   | DQ1  | 39  | VSS   | 4   | DQ2  | 40  | CAS0 |
| 5   | DQ3  | 41  | CAS2  | 6   | DQ4  | 42  | CAS3 |
| 7   | DQ5  | 43  | CAS1  | 8   | DQ6  | 44  | RAS0 |
| 9   | DQ7  | 45  | NC    | 10  | VCC  | 46  | NC   |
| 11  | PD1  | 47  | WRITE | 12  | A0   | 48  | NC   |
| 13  | A1   | 49  | DQ18  | 14  | A2   | 50  | DQ19 |
| 15  | A3   | 51  | DQ20  | 16  | A4   | 52  | DQ21 |
| 17  | A5   | 53  | DQ22  | 18  | A6   | 54  | DQ23 |
| 19  | A10  | 55  | NC    | 20  | NC   | 56  | DQ24 |
| 21  | DQ8  | 57  | DQ25  | 22  | DQ9  | 58  | DQ26 |
| 23  | DQ10 | 59  | DQ28  | 24  | DQ11 | 60  | DQ27 |
| 25  | DQ12 | 61  | VCC   | 26  | DQ13 | 62  | DQ29 |
| 27  | DQ14 | 63  | DQ30  | 28  | A7   | 64  | DQ31 |
| 29  | A11  | 65  | NC    | 30  | VCC  | 66  | PD2  |
| 31  | A8   | 67  | PD3   | 32  | A9   | 68  | PD4  |
| 33  | NC   | 69  | PD5   | 34  | RAS2 | 70  | PD6  |
| 35  | DQ15 | 71  | PD7   | 36  | NC   | 72  | VSS  |

Front Side

Back Side



Block Diagram

### Absolute Maximum Ratings <sup>1)</sup>

|                                       |  |
|---------------------------------------|--|
| Operating temperature range.....      | 0 to 70 °C                               |
| Storage temperature range.....        | – 55 to 150 °C                           |
| Soldering temperature.....            | 260 °C                                   |
| Soldering time.....                   | 10 s                                     |
| Input/output voltage.....             | -0.5 to min (V <sub>CC</sub> +0.5,4.6) V |
| Power supply voltage.....             | -0.5V to 4.6 V                           |
| Power dissipation.....                | 1.0 W                                    |
| Data out current (short circuit)..... | 50 mA                                    |

### DC Characteristics

$T_A = 0 \text{ to } 70 \text{ °C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $V_{CC} = 3 \text{ V} \pm 0.3 \text{ V}$

| Parameter   | Symbol     | Limit Values |              | Unit     | Note     |
|---|------------|--------------|--------------|----------|----------|
|   |            | min.         | max.         |          |          |
| Input high voltage  | $V_{IH}$   | 2.0          | $V_{CC}+0.3$ | V        | 2)       |
| Input low voltage   | $V_{IL}$   | – 0.3        | 0.8          | V        | 2)       |
| Output high voltage (LVTTL)<br>Output „H“ level voltage (I <sub>out</sub> = -2mA)   | $V_{OH}$   | 2.4          | –            | V        |          |
| Output low voltage (LVTTL)<br>Output „L“ level voltage (I <sub>out</sub> = +2mA)  | $V_{OL}$   | –            | 0.4          | V        |          |
| Output high voltage (LVCMOS)<br>Output „H“ level voltage (I <sub>out</sub> = -100uA)  | $V_{OH}$   | $V_{CC}-0.2$ | -            | V        | 6)       |
| Output low voltage (LVCMOS)<br>Output „L“ level voltage (I <sub>out</sub> = +100uA)   | $V_{OL}$   | -            | 0.2          | V        | 6)       |
| Input leakage current, any input<br>( $0 \text{ V} < V_{in} < V_{CC}$ , all other pins = 0 V)   | $I_{I(L)}$ | – 10         | 10           | μA       |          |
| Output leakage current<br>(DO is disabled, $0 \text{ V} < V_{out} < V_{CC}$ )   | $I_{O(L)}$ | – 10         | 10           | μA       |          |
| Average $V_{CC}$ supply current:<br>-50 ns version<br>-60 ns version<br>( $\overline{RAS}$ , $\overline{CAS}$ , address cycling: $t_{RC} = t_{RC \text{ min.}}$ )                     | $I_{CC1}$  | –            | 280<br>240   | mA<br>mA | 3) 4) 5) |
| Standby $V_{CC}$ supply current<br>( $\overline{RAS}=\overline{CAS}=V_{IH}$ )   | $I_{CC2}$  | –            | 4            | mA       | –        |
| Average $V_{CC}$ supply current, during RAS-only<br>refresh cycles:<br>-50 ns version<br>-60 ns version<br>(RAS cycling: $\overline{CAS} = V_{IH}$ ; $t_{RC} = t_{RC \text{ min.}}$ ) | $I_{CC3}$  | –            | 280<br>240   | mA<br>mA | 3) 5)    |

### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3$  V  $\pm$  0.3 V

| Parameter   | Symbol    | Limit Values |            | Unit     | Note     |
|---|-----------|--------------|------------|----------|----------|
|   |           | min.         | max.       |          |          |
| Average $V_{CC}$ supply current, during fast page mode:<br>-50 ns version<br>-60 ns version<br>( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: $t_{PC}=t_{PC}$ min.)                                  | $I_{CC4}$ | –            | 170<br>150 | mA<br>mA | 3) 4) 5) |
| Standby $V_{CC}$ supply current<br>( $\overline{RAS}=\overline{CAS}= V_{CC}-0.2V$ )   | $I_{CC5}$ | –            | 400        | A        | –        |
| Average $V_{CC}$ supply current, during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode:<br>-50 ns version<br>-60 ns version<br>( $\overline{RAS}$ , $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min.)          | $I_{CC6}$ | –            | 280<br>240 | mA<br>mA | 3) 4)    |
| Self Refresh Current<br>Average Power Supply Current during Self Refresh.<br>(CBR cycle with $t_{RAS}>TRASS_{min}$ , $\overline{CAS}$ held low, $\overline{WE} = V_{CC}-0.2V$ , Address and Din= $V_{CC}-0.2V$ or 0.2V) | $I_{CC7}$ | –            | 400        | A        |          |

## SO-DIMM PACKAGE OUTLINES

