

## 2M x 36-Bit Dynamic RAM Module

## HYM 362140S/GS-60/-70

### Advanced Information

- 2 097 152 words by 36-bit organization (alternative 4 194 304 words by 18-bit)
- Fast access and cycle time  
60 ns access time  
110 ns cycle time (-60 version)  
70 ns access time  
130 ns cycle time (-70 version)
- Fast page mode capability with  
40 ns cycle time (-60 version)  
45 ns cycle time (-70 version)
- Single + 5 V ( $\pm 10\%$ ) supply
- Low power dissipation  
max. 6952 mW active (-60 version)  
max. 6292 mW active (-70 version)  
CMOS – 132 mW standby  
TTL – 264 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh  
 $\overline{\text{RAS}}$ -only-refresh  
Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module with 31.75 mm height
- Utilizes eight 1M  $\times$  1-DRAMs and sixteen 1M  $\times$  4 DRAMs in 300 mil SOJ-packages
- 1024 refresh cycles / 16 ms
- Tin-Lead contact pads (S - version)
- Gold contact pads (GS - version)

### Ordering Information

Type	Ordering Code	Package	Description
HYM 362140S-60	Q67100-Q955	L-SIM-72-8	DRAM Module (access time 60 ns)
HYM 362140S-70	Q67100-Q954	L-SIM-72-8	DRAM Module (access time 70 ns)
HYM 362140GS-60	Q67100-Q957	L-SIM-72-8	DRAM Module (access time 60 ns)
HYM 362140GS-70	Q67100-Q956	L-SIM-72-8	DRAM Module (access time 70 ns)

The HYM 362140S/GS-60/-70 is a 8 M Byte DRAM module organized as 2 097 152 words by 36-bit in a 72-pin single-in-line package comprising eight HYB 511000BJ 1M × 1 DRAMs and sixteen HYB 514400BJ 1M × 4 DRAMs in 300 mil wide SOJ-packages mounted together with twelve 0.2 μF ceramic decoupling capacitors on a PC board.

The HYM 362140S/GS-60/-70 can also be used as a 4 194 304 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

Each HYB 511000BJ and HYB 514400BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 362140S/GS-60/-70 dictates the use of early write cycles.

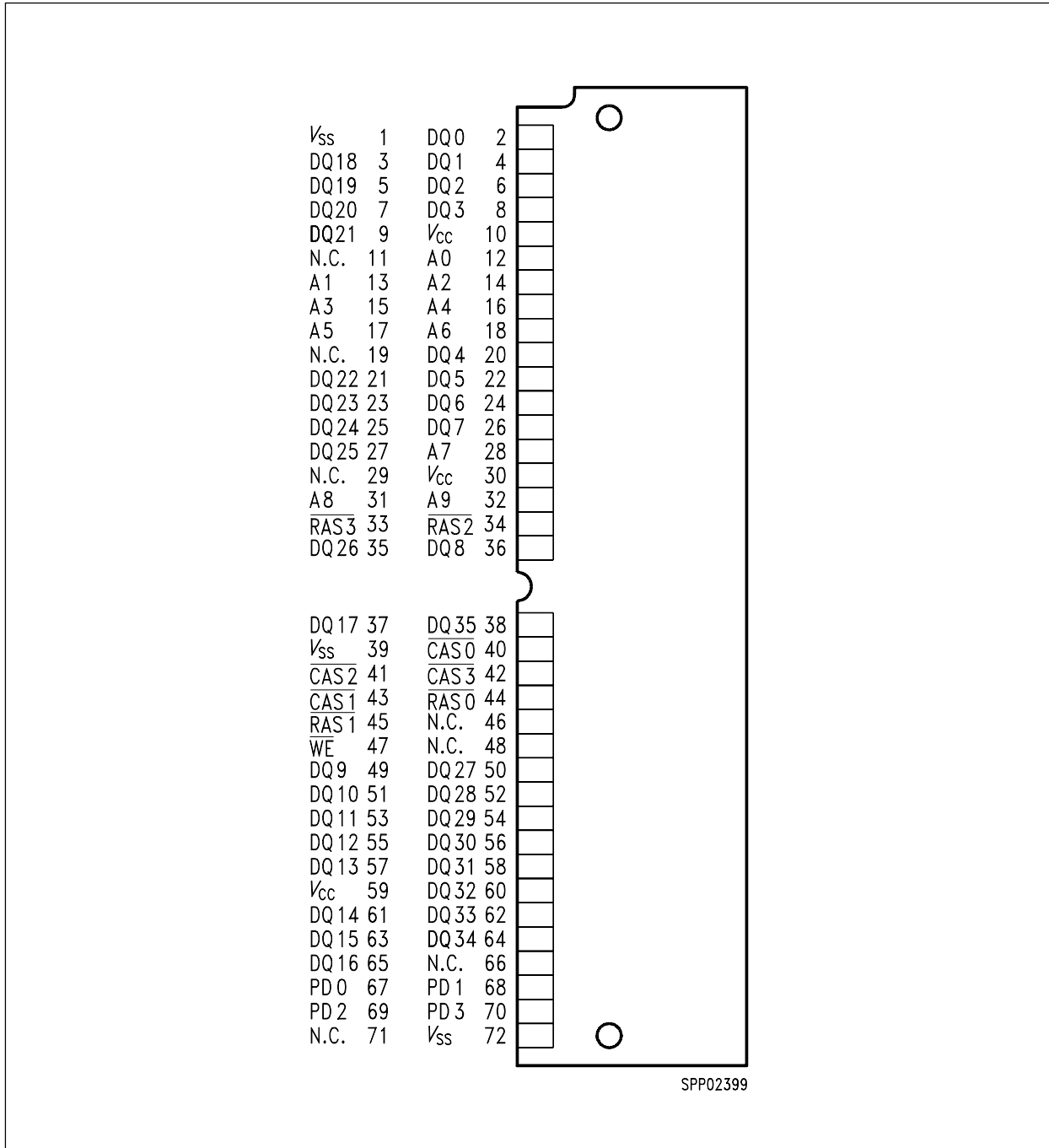
### Pin Definitions and Functions

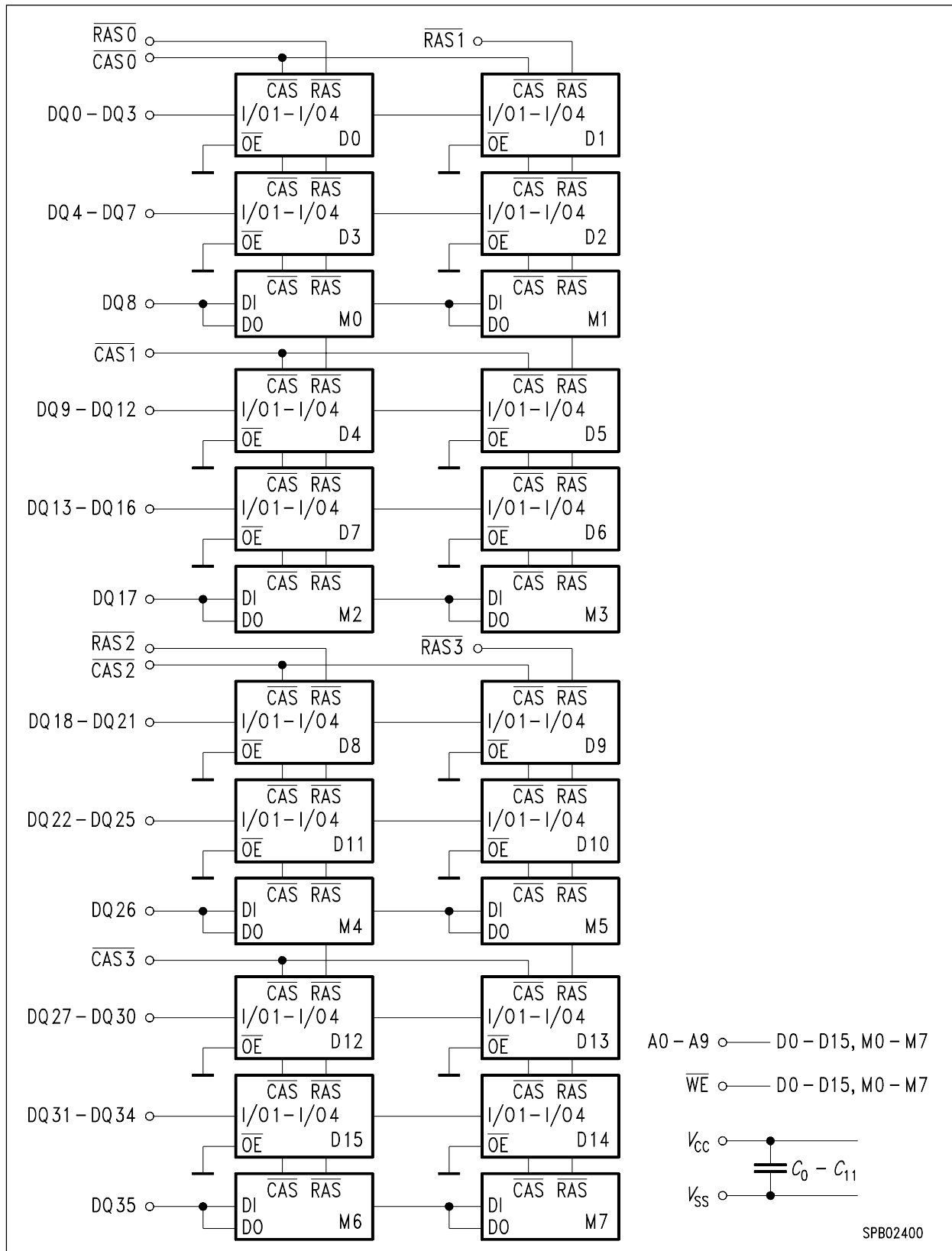
Pin No.	Function
A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}} - \overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$V_{\text{CC}}$	Power (+ 5 V)
$V_{\text{SS}}$	Ground
PD	Presence Detect Pin
N.C.	No Connection

### Presence Detect Pins

	-60	-70
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	$V_{\text{SS}}$
PD3	N.C.	N.C.

**Pin Configuration**  
(top view)





**Block Diagram**

### Absolute Maximum Ratings

Operation temperature range .....	0 to + 70 °C
Storage temperature range.....	– 55 to 125 °C
Soldering temperature .....	260 °C
Soldering time .....	10 s
Input/output voltage .....	– 1 to + 7 V
Power supply voltage.....	– 1 to + 7 V
Power dissipation.....	8.9 W
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics<sup>1)</sup>

$T_A = 0$  to 70 °C,  $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.4	5.5	V	
Input low voltage	$V_{IL}$	– 1.0	0.8	V	
Output high voltage ( $I_{OUT} = -5\text{ mA}$ )	$V_{OH}$	2.4	–	V	
Output low voltage ( $I_{OUT} = 4.2\text{ mA}$ )	$V_{OL}$	–	0.4	V	
Input leakage current ( $0\text{ V} < V_{IN} < 6.5\text{ V}$ , all other pins = 0 V)	$I_{I(L)}$	– 20	20	μA	
Output leakage current (DO is disabled, $0\text{ V} < V_{OUT} < 5.5\text{ V}$ )	$I_{O(L)}$	– 20	20	μA	
Average $V_{CC}$ supply current (RAS, CAS, address cycling, $t_{RC} = t_{RC\text{ min}}$ ) -60 version -70 version	$I_{CC1}$	–	1264 1144	mA mA	<sup>2)</sup> <sup>3)</sup>
Standby $V_{CC}$ supply current (RAS = CAS = $V_{IH}$ )	$I_{CC2}$	–	48	mA	
Average $V_{CC}$ supply current during RAS only refresh cycles (RAS cycling, CAS = $V_{IH}$ , $t_{RC} = t_{RC\text{ min}}$ ) -60 version -70 version	$I_{CC3}$	–	1264 1144	mA mA	<sup>2)</sup>

### DC Characteristics<sup>1)</sup> (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during fast page mode ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling, $t_{PC} = t_{PC\ min}$ ) -60 version -70 version	$I_{CC4}$	– –	864 744	mA mA	<sup>2)</sup> <sup>3)</sup>
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2\ V$ )	$I_{CC5}$	–	24	mA	
Average $V_{CC}$ supply current during CAS-before-RAS refresh mode ( $\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = t_{RC\ min}$ ) -60 version -70 version	$I_{CC6}$	– –	1264 1144	mA mA	<sup>2)</sup>

### Capacitance

$T_A = 0\ to\ 70\ ^\circ C$ ,  $V_{CC} = 5\ V \pm 10\ \%$ ,  $f = 1\ MHz$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, WE)	$C_{11}$	–	180	pF
Input capacitance ( $\overline{RAS0}$ - $\overline{RAS3}$ , $\overline{CAS0}$ - $\overline{CAS3}$ )	$C_{12}$	–	45	pF
I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34)	$C_{101}$	–	25	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{102}$	–	35	pF

### AC Characteristics <sup>4) 5)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit
		HYM 362140S/GS-60		HYM 362140S/GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	$t_{RC}$	110	–	130	–	ns
Fast page mode cycle time	$t_{PC}$	40	–	45	–	ns
Access time from $\overline{RAS}$ <sup>6) 11) 12)</sup>	$t_{RAC}$	–	60	–	70	ns
Access time from $\overline{CAS}$ <sup>6) 11)</sup>	$t_{CAC}$	–	15	–	20	ns
Access time from column address <sup>6) 12)</sup>	$t_{AA}$	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge <sup>6)</sup>	$t_{CPA}$	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z <sup>6)</sup>	$t_{CLZ}$	0	–	0	–	ns
Output buffer turn-off delay <sup>7)</sup>	$t_{OFF}$	0	20	0	20	ns
Transition time (rise and fall) <sup>5)</sup>	$t_T$	3	50	3	50	ns
$\overline{RAS}$ precharge time	$t_{RP}$	40	–	50	–	ns
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	$t_{RASP}$	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	$t_{RHCP}$	35	–	40	–	ns
$\overline{RAS}$ hold time	$t_{RSH}$	15	–	20	–	ns
$\overline{CAS}$ hold time	$t_{CSH}$	60	–	70	–	ns
$\overline{CAS}$ pulse width	$t_{CAS}$	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time <sup>11)</sup>	$t_{RCD}$	20	45	20	50	ns
$\overline{RAS}$ to column address delay time <sup>12)</sup>	$t_{RAD}$	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	$t_{CP}$	10	–	10	–	ns
Row address setup time	$t_{ASR}$	0	–	0	–	ns
Row address hold time	$t_{RAH}$	10	–	10	–	ns
Column address setup time	$t_{ASC}$	0	–	0	–	ns
Column address hold time	$t_{CAH}$	15	–	15	–	ns

### AC Characteristics<sup>4) 5)</sup> (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit
		HYM 362140S/GS-60		HYM 362140S/GS-70		
		min.	max.	min.	max.	
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	–	35	–	ns
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	ns
Read command hold time <sup>8)</sup>	$t_{\text{RCH}}$	0	–	0	–	ns
Read command hold time ref. to $\overline{\text{RAS}}$ <sup>8)</sup>	$t_{\text{RRH}}$	0	–	0	–	ns
Write command hold time	$t_{\text{WCH}}$	10	–	15	–	ns
Write command pulse width	$t_{\text{WCP}}$	10	–	15	–	ns
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	–	20	–	ns
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	–	20	–	ns
Data setup time <sup>9)</sup>	$t_{\text{DS}}$	0	–	0	–	ns
Data hold time <sup>9)</sup>	$t_{\text{DH}}$	15	–	15	–	ns
Refresh period	$t_{\text{REF}}$	–	16	–	16	ms
Write command setup time <sup>10)</sup>	$t_{\text{WCS}}$	0	–	0	–	ns
$\overline{\text{CAS}}$ setup time <sup>13)</sup>	$t_{\text{CSR}}$	5	–	5	–	ns
$\overline{\text{CAS}}$ hold time <sup>13)</sup>	$t_{\text{CHR}}$	15	–	15	–	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{\text{RPC}}$	0	–	0	–	ns
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	10	–	10	–	ns
Write to $\overline{\text{RAS}}$ precharge time <sup>13)</sup>	$t_{\text{WRP}}$	10	–	10	–	ns
Write hold time ref. to $\overline{\text{RAS}}$ <sup>13)</sup>	$t_{\text{WRH}}$	10	–	10	–	ns



**Notes:**

- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading.  
Specified values are measured with the output open.
- 4) An initial pause of 200  $\mu$ s is required after power-up followed by 8 RAS cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 5)  $V_{IH(max)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals.  
Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 6) Measured with a load equivalent of 2 TTL loads and 100 pF.
- 7)  $t_{OFF(max)}$  defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
- 8) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 9) These parameters are referenced to the CAS leading edge.
- 10)  $t_{WCS}$  is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only.  
If  $t_{WCS} > t_{WCS(min)}$ , the cycle is an early write cycle and data out pin will remain open (high impedance).
- 11) Operation within the  $t_{RCD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled by  $t_{CAS}$ .
- 12) Operation within the  $t_{RAD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled by  $t_{AA}$ .
- 13) For CAS-before-RAS cycles only.