

- SIMM modules with 4 194 304 words by 36-Bit organization for PC main memory applications
- Fast access and cycle time
  - 50 ns access time
  - 84 ns cycle time (-50 version)
  - 60 ns access time
  - 104 ns cycle time (-60 version)
- Hyper Page Mode (EDO) capability
  - 20 ns cycle time (-50 version)
  - 25 ns cycle time (-60 version)
- Single + 5 V ( $\pm 10\%$ ) supply
- Low power dissipation
  - max. 6820 mW active (-50 version)
  - max. 6160 mW active (-60 version)
  - CMOS – 66 mW standby
  - TTL – 132 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - $\overline{\text{RAS}}$ -only-refresh
  - Hidden-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-12) with 22.9 mm (900 mil) height
- Utilizes eight 4Mx4-EDO-DRAMs and four 4Mx1-EDO-DRAMs in SOJ packages
- 2048 refresh cycles / 32 ms
- Optimized for use in byte-write parity applications
- Tin-Lead contact pads (S-version)
- Gold contact pads (GS - version)

The HYM 364025S/GS-50/-60 is a 16 MByte DRAM module organized as 4 194 304 words by 36-Bit in a 72-pin single-in-line package comprising eight HYB 5117405BJ 4M × 4 EDO-DRAMs and four HYB 514105BJ 4M x 1 EDO-DRAMs in 300 mil wide SOJ-packages mounted together with ceramic decoupling capacitors on a PC board.

Each HYB 5117405BJ and HYB 514105BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

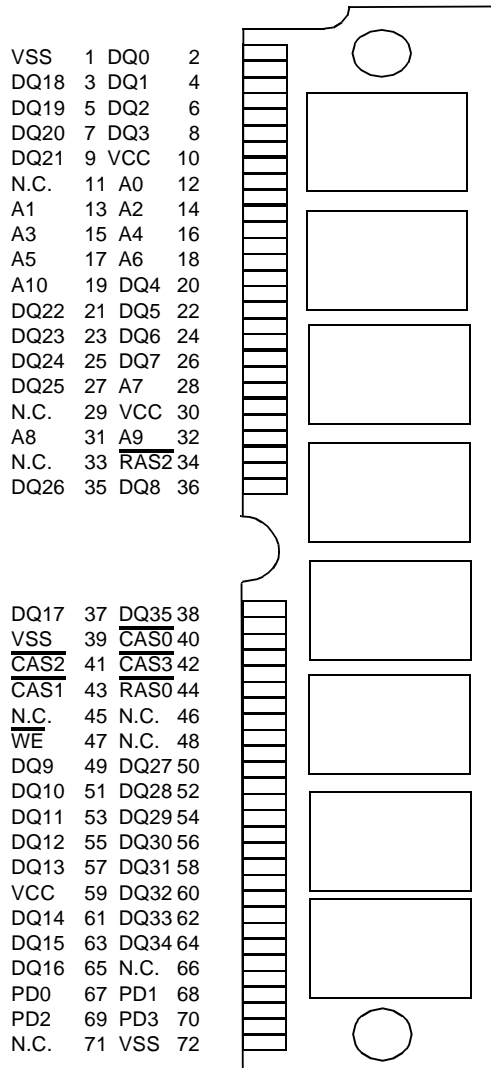
The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 364025S/GS-50/-60 dictates the use of early write cycles.

### Ordering Information

Type	Ordering Code	Package	Description
HYM 364025S-50	on request	L-SIM-72-12	EDO-DRAM Module (access time 50 ns)
HYM 364025S-60	Q67100-Q2366	L-SIM-72-12	EDO-DRAM Module (access time 60 ns)
HYM 364025GS-50	on request	L-SIM-72-12	EDO-DRAM Module (access time 50 ns)
HYM 364025GS-60	Q67100-Q2367	L-SIM-72-12	EDO-DRAM Module (access time 60 ns)

### Pin Configuration

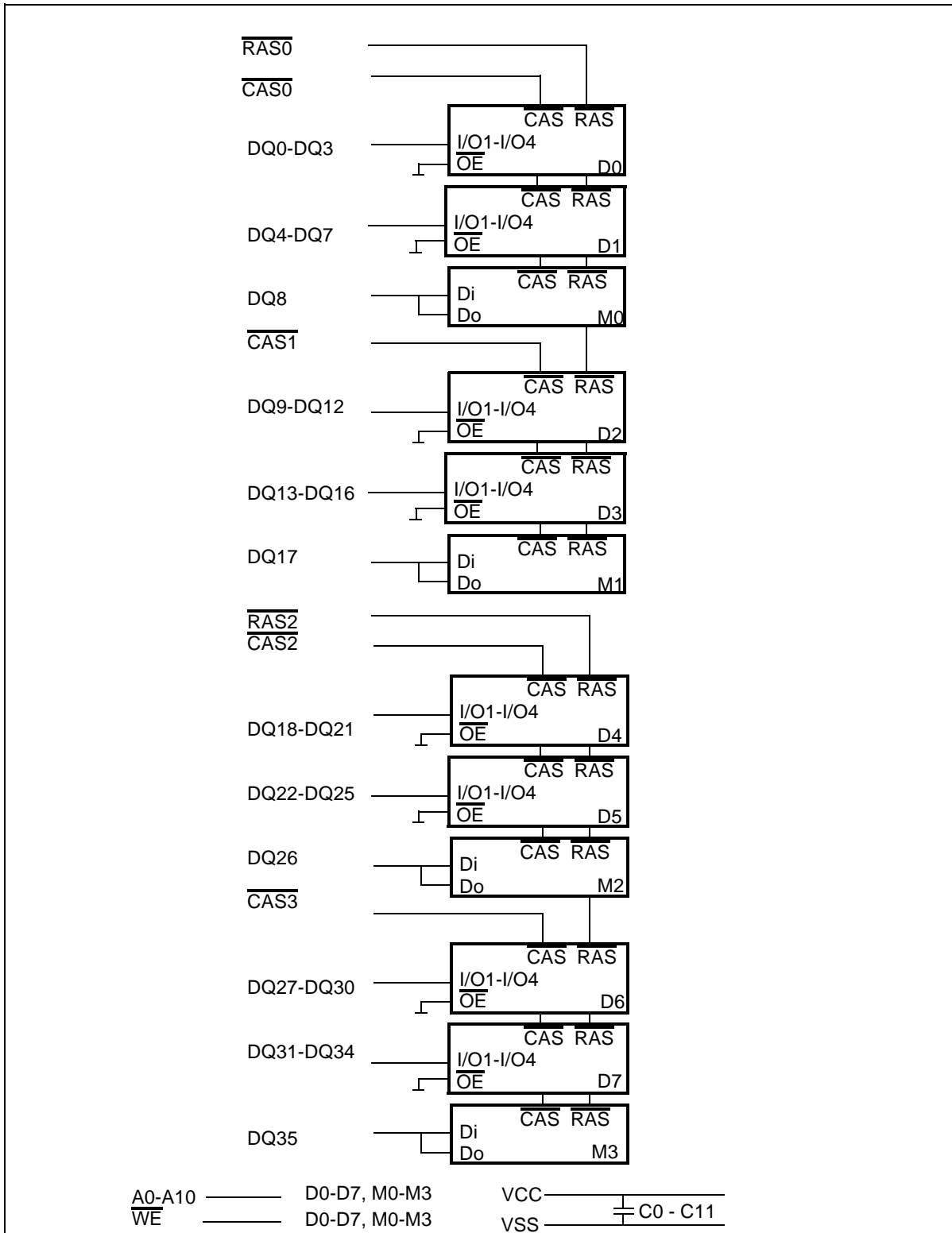


### Pin Names

A0-A10	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}}$ , $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$V_{\text{CC}}$	Power (+ 5 V)
$V_{\text{SS}}$	Ground
PD	Presence Detect Pin
N.C.	No Connection

### Presence Detect Pins

	-50	-60
PD0	$V_{\text{SS}}$	$V_{\text{SS}}$
PD1	N.C.	N.C.
PD2	$V_{\text{SS}}$	N.C.
PD3	$V_{\text{SS}}$	N.C.



**Block Diagram**

### Absolute Maximum Ratings

Operation temperature range .....	0 to + 70 °C
Storage temperature range.....	- 55 to 125 °C
Input/output voltage .....	-0.5V to min (V <sub>CC</sub> +0.5, 7.0) V
Power supply voltage.....	- 1 to + 7 V
Power dissipation.....	8.7 W
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

T<sub>A</sub> = 0 to 70 °C, V<sub>CC</sub> = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V <sub>IH</sub>	2.4	V <sub>CC</sub> +0.5	V	1)
Input low voltage	V <sub>IL</sub>	- 0.5	0.8	V	1)
Output high voltage (I <sub>OUT</sub> = - 5 mA)	V <sub>OH</sub>	2.4	-	V	1)
Output low voltage (I <sub>OUT</sub> = 4.2 mA)	V <sub>OL</sub>	-	0.4	V	1)
Input leakage current (0 V < V <sub>IN</sub> < 6.5 V, all other pins = 0 V)	I <sub>I(L)</sub>	- 20	20	μA	1)
Output leakage current (DO is disabled, 0 V < V <sub>OUT</sub> < 5.5 V)	I <sub>O(L)</sub>	- 10	10	μA	1)
Average V <sub>CC</sub> supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , address cycling, t <sub>RC</sub> = t <sub>RC</sub> min) 50 ns - Version 60 ns - Version	I <sub>CC1</sub>	-	1240 1120	mA mA	2) 3) 4)
Standby V <sub>CC</sub> supply current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	I <sub>CC2</sub>	-	16	mA	
Average V <sub>CC</sub> supply current during $\overline{\text{RAS}}$ only refresh cycles ( $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , t <sub>RC</sub> = t <sub>RC</sub> min) 50 ns - Version 60 ns - Version	I <sub>CC3</sub>	-	1240 1120	mA mA	2) 4)

### DC Characteristics<sup>1)</sup> (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during hyper page mode (EDO) ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling, $t_{HPC} = t_{HPC} \text{ min}$ ) 50 ns - Version 60 ns - Version	$I_{CC4}$	–	840 680	mA mA	2) 3) 4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$ )	$I_{CC5}$	–	8	mA	1)
Average $V_{CC}$ supply current during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode ( $\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = t_{RC} \text{ min}$ ) 50 ns - Version 60 ns - Version	$I_{CC6}$	–	1240 1120	mA mA	2) 4)

### Capacitance

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V} \pm 10 \%$ ,  $f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, $\overline{WE}$ )	$C_{11}$	–	75	pF
Input capacitance ( $\overline{RAS0}$ , $\overline{RAS2}$ )	$C_{12}$	–	45	pF
Input capacitance ( $\overline{CAS0}$ - $\overline{CAS3}$ )	$C_{13}$	–	25	pF
I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34)	$C_{IO1}$	–	15	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{IO2}$	–	25	pF

### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

#### *common parameters*

Random read or write cycle time	$t_{RC}$	84	–	104	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	–	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	8	10k	10	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	12	37	14	45	ns	
$\overline{RAS}$ to column address delay time	$t_{RAD}$	10	25	12	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13		15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	40		50	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	ns	7
Refresh period	$t_{REF}$	–	32	–	32	ms	

#### *Read Cycle*

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	ns	12

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

#### Early Write Cycle

Write command hold time	$t_{WCH}$	8	–	10	–	ns	
Write command pulse width	$t_{WP}$	8	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	ns	13
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	13	–	15	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	ns	14
Data hold time	$t_{DH}$	8	–	10	–	ns	14

#### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{HPC}$	20	–	25	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	8	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	–	27	–	32	ns	7
Output data hold time	$t_{COH}$	5	–	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	$t_{RAS}$	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	$t_{RHCP}$	27	–	32	–	ns	

#### $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

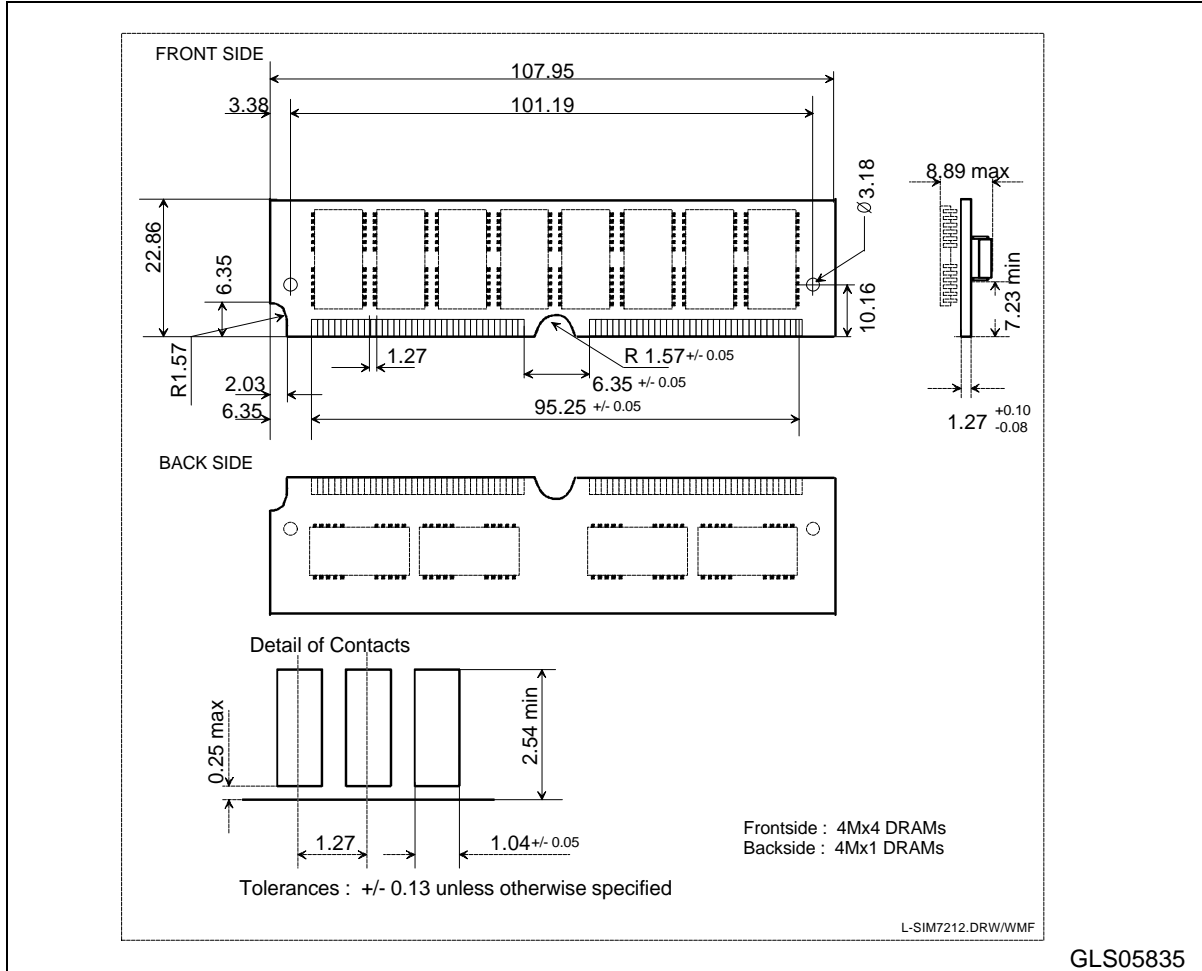
$\overline{CAS}$ setup time	$t_{CSR}$	10	–	10	–	ns	
$\overline{CAS}$ hold time	$t_{CHR}$	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	10	–	10	–	ns	



### Notes:

- 1) All voltages are referenced to  $V_{SS}$ .  
Vil may undershoot to -2.0 V for pulse width of less than or equal to 4 ns. Pulse width is measured at 50% points with amplitude measured peak to the DC reference.
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while RAS = Vil. In case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle.
- 5) An initial pause of 200  $\mu$ s is required after power-up followed by 8  $\overline{\text{RAS}}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at Vol = 0.8 V and Voh = 2.0 V. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ .  $t_{CAC}$  is measured from tristate.
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.
- 13)  $t_{WCS}$  is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only.  
If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge.

**Package Outline**



**Module Package, L-SIM-72-12  
(Single in-Line Memory Module)**