SIEMENS

4M x 36-Bit Dynamic RAM Module — HYM 364020S/GS-60

- SIMM modules with 4 194 304 words by 36-Bit organization
  for PC main memory applications
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
- Fast page mode capability
  40 ns cycle time (-60 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 7260 mW active (-60 version)
  CMOS – 66 mW standby
  TTL –132 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-12) with 22.9 mm (900 mil) height
- Utilizes eight 4Mx4-DRAMs and four 4Mx1-DRAMs in SOJ packages
- 2048 refresh cycles / 32 ms
- Optimized for use in byte-write parity applications
- Tin-Lead contact pads (S-version)
- Gold contact pads (GS - version)

The HYM 364020S/GS-60 is a 16 MByte DRAM module organized as 4 194 304 words by 36-Bit in a 72-pin single-in-line package comprising eight HYB 5117400BJ 4M × 4 DRAMs and four HYB 514100BJ 4M x 1 DRAMS in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 364020S/GS-60 can also be used as a 8 388 608 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, … , DQ17 and DQ35, respectively.

Each HYB 5117400BJ and HYB 514100BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

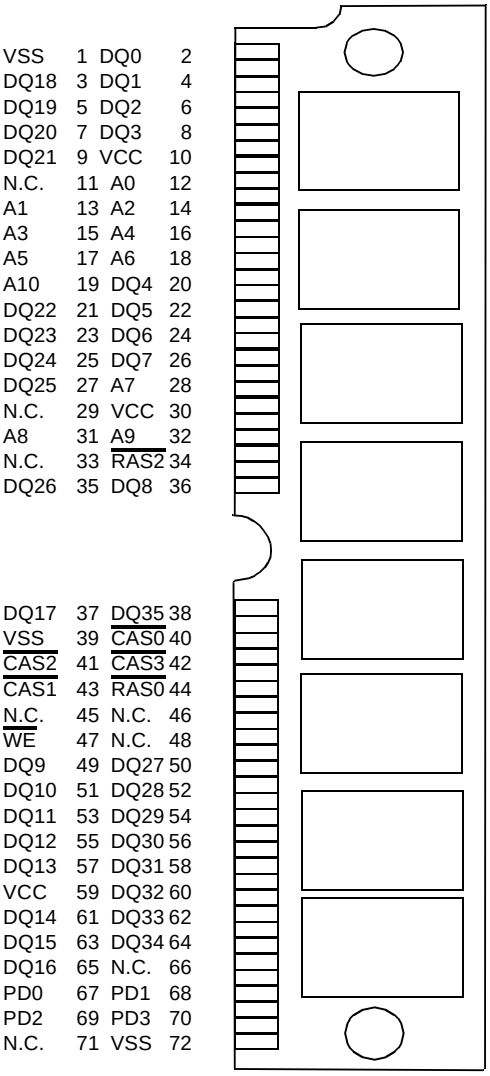
The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 364020S/GS-60 dictates the use of early write cycles.

Ordering Information

Type	Ordering Code	Package	Description
HYM 364020S-60	Q67100-Q2006	L-SIM-72-12	DRAM Module (access time 60 ns)
HYM 364020GS-60	Q67100-Q982	L-SIM-72-12	DRAM Module (access time 60 ns)

Pin Configuration

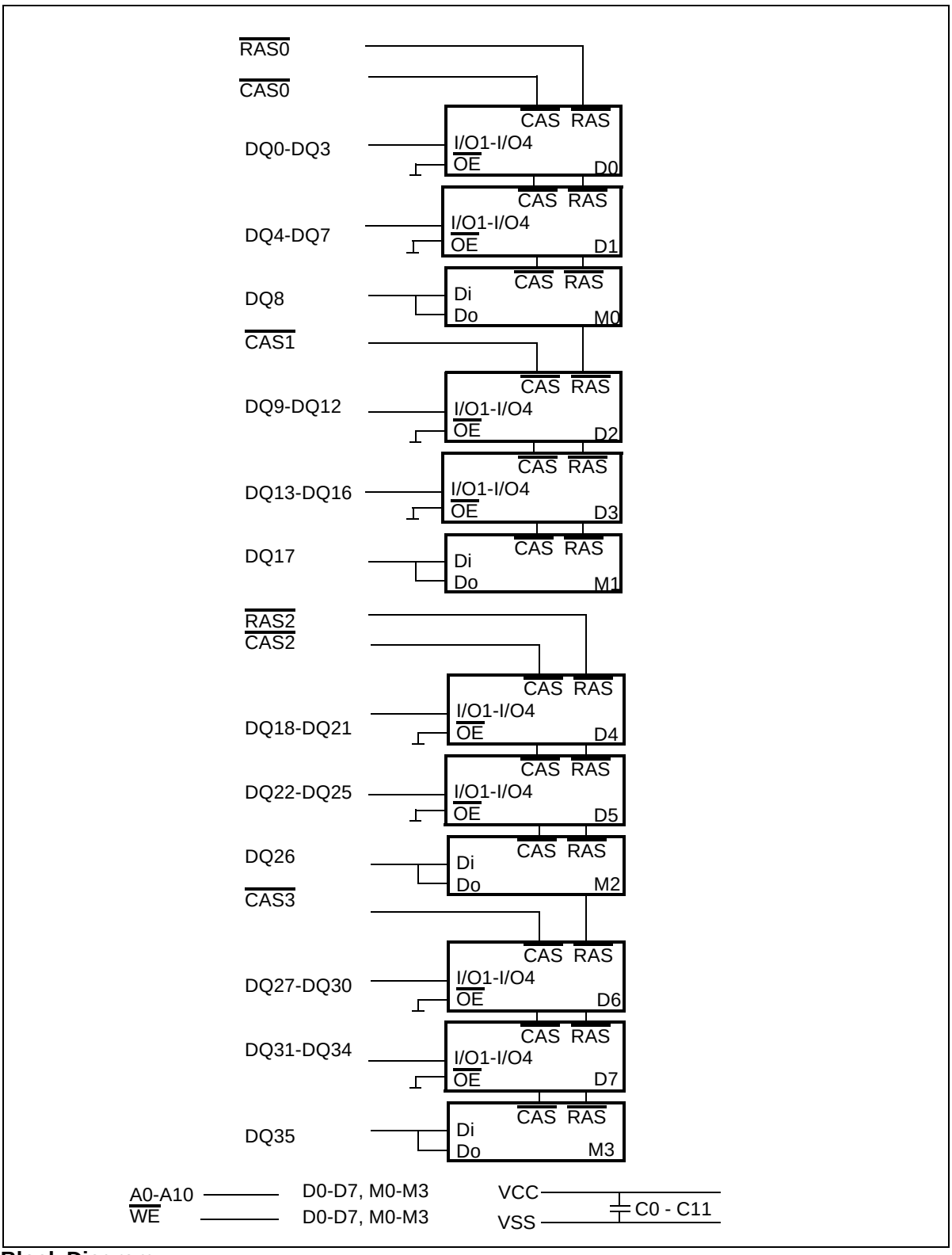


Pin Names

A0-A10	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-60
PD0	V_{SS}
PD1	N.C.
PD2	N.C.
PD3	N.C.



Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to 125 °C
Input/output voltage ..... –0.5V to min (Vcc+0.5, 7.0) V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 9.3 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min) -60 version	I_{CC1}	–	1320	mA	2),3),4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	24	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min) -60 version	I_{CC3}	–	1320	mA	2),4)

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min) -60 version	I_{CC4}	– –	920 –	mA mA	[2],[3],[4]
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	12	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min) -60 version	I_{CC6}	– –			[2],[4]

Capacitance
T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, $\overline{WE}$)	C_{I1}	–	75	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	25	pF
I/O capacitance (DQ0-DQ7,DQ9-DQ16,DQ18-DQ25,DQ27-DQ34)	C_{IO1}	–	15	pF
I/O capacitance (DQ8,DQ17,DQ26,DQ35)	C_{IO2}	–	25	pF

AC Characteristics [5)6)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Note
		-60			
		min.	max.		
common parameters					
Random read or write cycle time	t_{RC}	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	ns	
Row address setup time	t_{ASR}	0	–	ns	
Row address hold time	t_{RAH}	10	–	ns	
Column address setup time	t_{ASC}	0	–	ns	
Column address hold time	t_{CAH}	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45		
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	ns	
Transition time (rise and fall)	t_T	3	50	ns	7
Refresh period	t_{REF}	–	32	ms	
Read Cycle					
Access time from $\overline{RAS}$	t_{RAC}	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	15	ns	8, 9
Access time from column address	t_{AA}	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	ns	
Read command setup time	t_{RCS}	0	–	ns	
Read command hold time	t_{RCH}	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	15	ns	12

AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Note
		-60			
		min.	max.		
Early Write Cycle					
Write command hold time	t_{WCH}	10	–	ns	
Write command pulse width	t_{WP}	10	–	ns	
Write command setup time	t_{WCS}	0	–	ns	13
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	ns	
Data setup time	t_{DS}	0	–	ns	14
Data hold time	t_{DH}	10	–	ns	14
Fast Page Mode Cycle					
Fast page mode cycle time	t_{PC}	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	35	ns	7
$\overline{RAS}$ pulse width	t_{RAS}	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	35	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle					
$\overline{CAS}$ setup time	t_{CSR}	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	ns	

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 5 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with a load equivalent to 2 TTL loads and 100 pF.

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels

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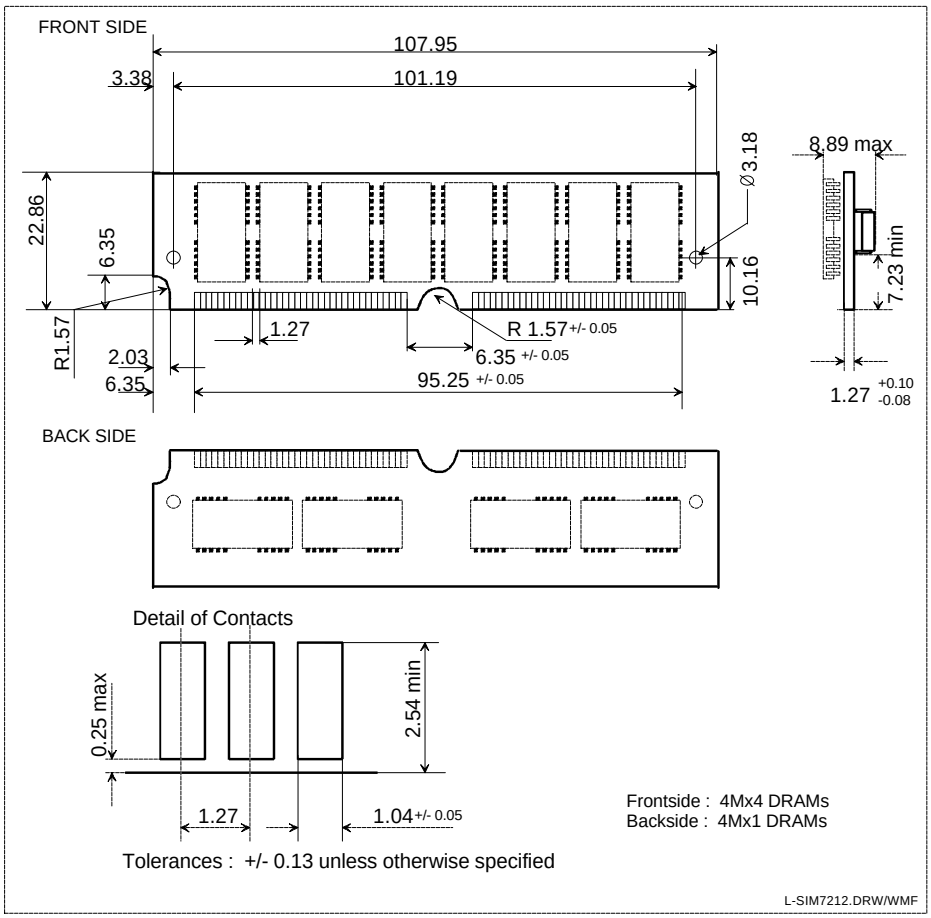
13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.

14) These parameters are referenced to the $\overline{CAS}$ leading edge.

Package Outline



GLS05835

Module Package, L-SIM-72-12

(Single in-Line Memory Module)