

### Advanced Information

- 4 194 304 words by 36-Bit organization
- Fast access and cycle time
  - 60 ns  $\overline{\text{RAS}}$  access time
  - 15 ns  $\overline{\text{CAS}}$  access time
  - 104 ns cycle time
- Hyper page mode (EDO) capability
  - 25 ns cycle time
- Single + 5 V ( $\pm 10\%$ ) supply
- Low power dissipation
  - max. 7260 mW active
  - CMOS – 66 mW standby
  - TTL – 132 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - $\overline{\text{RAS}}$ -only-refresh
  - Hidden-refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72) with 22.9 mm (900 mil) height
- Utilizes 12 4M x 3 DRAM's in 300 mil SOJ packages
- 2048 refresh cycles / 32 ms
- Optimized for use in byte-write parity applications
- Tin-Lead contact pads (HYM 364035S-60)
- Gold contact pads (HYM 364035GS-60)

The HYM 364035S/GS-60 is a 16 MByte EDO-DRAM module organized as 4 194 304 words by 36-Bit in a 72-pin single-in-line package comprising twelve HYB 5117305BJ 4M × 3 DRAMs in 300 mil wide SOJ-packages mounted together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYB 5117305BJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

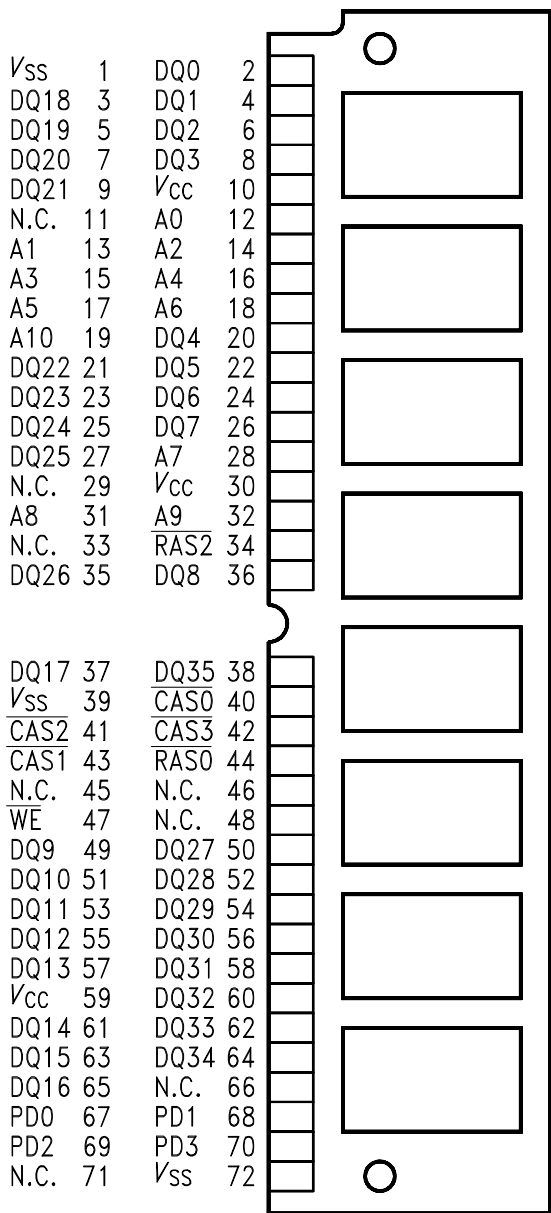
The speed of the module can be detected by the use of four presence detect pins.

The common I/O feature on the HYM 364035S-60 dictates the use of early write cycles.

**Ordering Information**

Type	Ordering Code	Package	Description
HYM 364035S-60	Q67100-Q3016	L-SIM-72-13	DRAM Module (access time 60 ns)
HYM 364035GS-60	Q67100-Q3017	L-SIM-72-13	DRAM Module (access time 60 ns)

### Pin Configuration (top view)



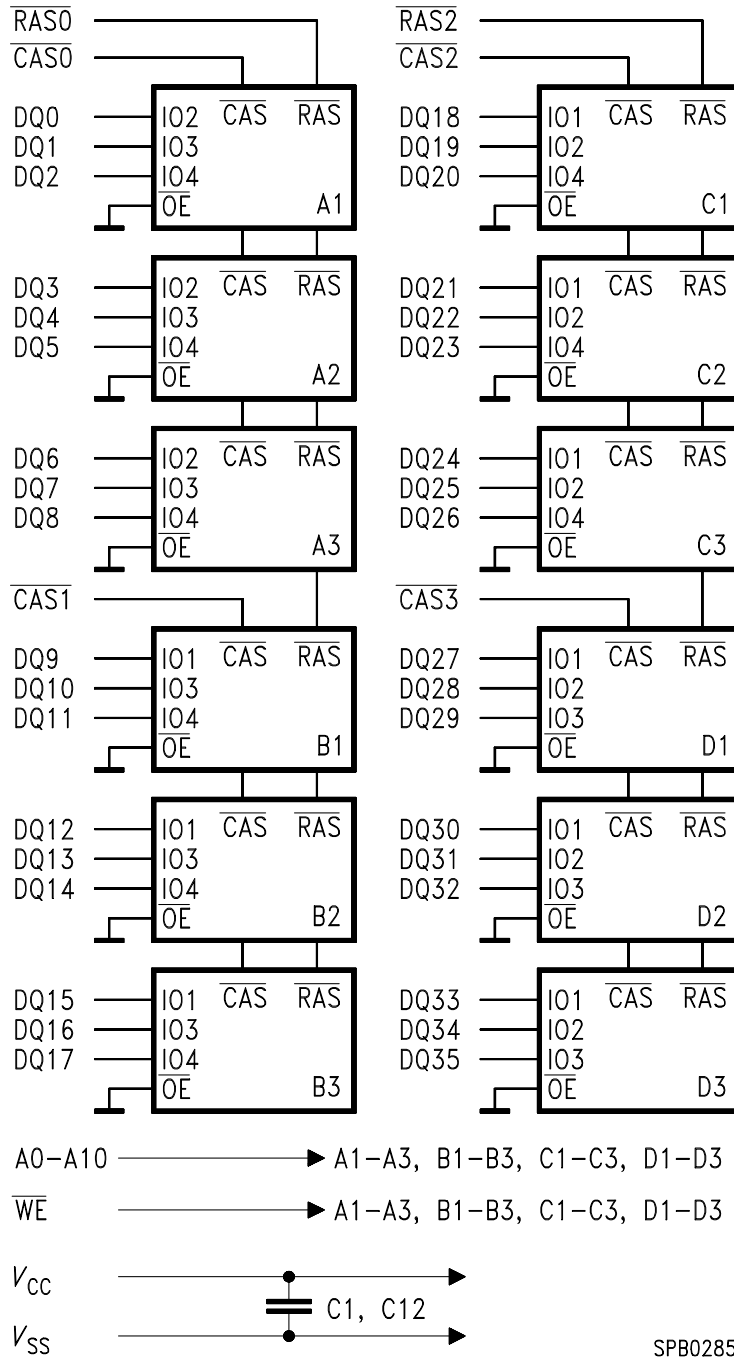
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### Pin Names

A0-A10	Address Inputs for HYM 364035S/GS
DQ0-DQ35	Data Input/Output
CAS0 - CAS3	Column Address Strobe
RAS0, RAS2	Row Address Strobe
WE	Read/Write Input
$V_{CC}$	Power (+ 5 V)
$V_{SS}$	Ground
PD	Presence Detect Pin
N.C.	No Connection

### Presence Detect Pins

	-60
PD0	$V_{SS}$
PD1	N.C.
PD2	N.C.
PD3	N.C.



### Block Diagram

### Absolute Maximum Ratings

Operation temperature range .....	0 to + 70 °C
Storage temperature range.....	– 55 to 125 °C
Input/output voltage .....	– 0.5 V to min ( $V_{CC} + 0.5, 7.0$ ) V
Power supply voltage.....	– 1 to + 7 V
Power dissipation.....	9.24 W
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.4	$V_{CC} + 0.5$	V	1)
Input low voltage	$V_{IL}$	– 0.5	0.8	V	1)
Output high voltage ( $I_{OUT} = -5$ mA)	$V_{OH}$	2.4	–	V	1)
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	–	0.4	V	1)
Input leakage current ( $0$ V < $V_{IN} < 6.5$ V, all other pins = 0 V)	$I_{I(L)}$	– 80	80	μA	1)
Output leakage current (DO is disabled, $0$ V < $V_{OUT} < 5.5$ V)	$I_{O(L)}$	– 10	10	μA	1)
Average $V_{CC}$ supply current ( $\overline{RAS}$ , $\overline{CAS}$ , address cycling, $t_{RC} = t_{RC}$ min) -60 ns version	$I_{CC1}$	–	1320	mA	2),3),4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	–	24	mA	
Average $V_{CC}$ supply current during $\overline{RAS}$ only refresh cycles ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = t_{RC}$ min) -60 ns version	$I_{CC3}$	–	1320	mA	2),4)

### DC Characteristics<sup>1)</sup> (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during hyper page mode (EDO) (RAS = $V_{IL}$ , CAS, address cycling, $t_{PC} = t_{PC\ min}$ ) -60 ns version	$I_{CC4}$	–	660	mA	2),3),4)
Standby $V_{CC}$ supply current (RAS = CAS = $V_{CC} - 0.2\ V$ )	$I_{CC5}$	–	12	mA	1)
Average $V_{CC}$ supply current during CAS-before-RAS refresh mode (RAS, CAS cycling, $t_{RC} = t_{RC\ min}$ ) -60 ns version	$I_{CC6}$	–	1320	mA	2),4)

### Capacitance

$T_A = 0\ to\ 70\ ^\circ C$ ,  $V_{CC} = 5\ V \pm 10\ \%$ ,  $f = 1\ MHz$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	$C_{I1}$	–	90	pF
Input capacitance ( $\overline{RAS0}$ , $\overline{RAS2}$ )	$C_{I2}$	–	45	pF
Input capacitance ( $\overline{CAS0}$ - $\overline{CAS3}$ )	$C_{I3}$	–	40	pF
Input capacitance ( $\overline{WE}$ )	$C_{I4}$	–	90	pF
I/O capacitance(DQ0-DQ35)	$C_{IO1}$	–	20	pF

### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol			Unit	Note
		-60			
		min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	104	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10k	ns	
CAS pulse width	$t_{CAS}$	10	10k	ns	
Row address setup time	$t_{ASR}$	0	–	ns	
Row address hold time	$t_{RAH}$	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	14	45	ns	
$\overline{RAS}$ to column address delay time	$t_{RAD}$	12	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	ns	7
Refresh period	$t_{REF}$	–	32	ms	

### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	60	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	ns	11
$\overline{CAS}$ to output in low-Z	$t_{CLZ}$	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	15	ns	12

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol			Unit	Note
		-60			
		min.	max.		

#### **Early Write Cycle**

Write command hold time	$t_{WCH}$	10	–	ns	
Write command pulse width	$t_{WP}$	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	ns	13
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	15	–	ns	
Data setup time	$t_{DS}$	0	–	ns	14
Data hold time	$t_{DH}$	10	–	ns	14

#### **Hyper Page Mode (EDO) Cycle**

Hyper page mode (EDO) cycle time	$t_{HPC}$	25	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	10	–	ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	–	32	ns	7
Output data hold time	$t_{COH}$	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	$t_{RAS}$	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	$t_{RHCP}$	32	–	ns	

#### **$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle**

$\overline{CAS}$ setup time	$t_{CSR}$	10	–	ns	
$\overline{CAS}$ hold time	$t_{CHR}$	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	10	–	ns	
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	10	–	ns	

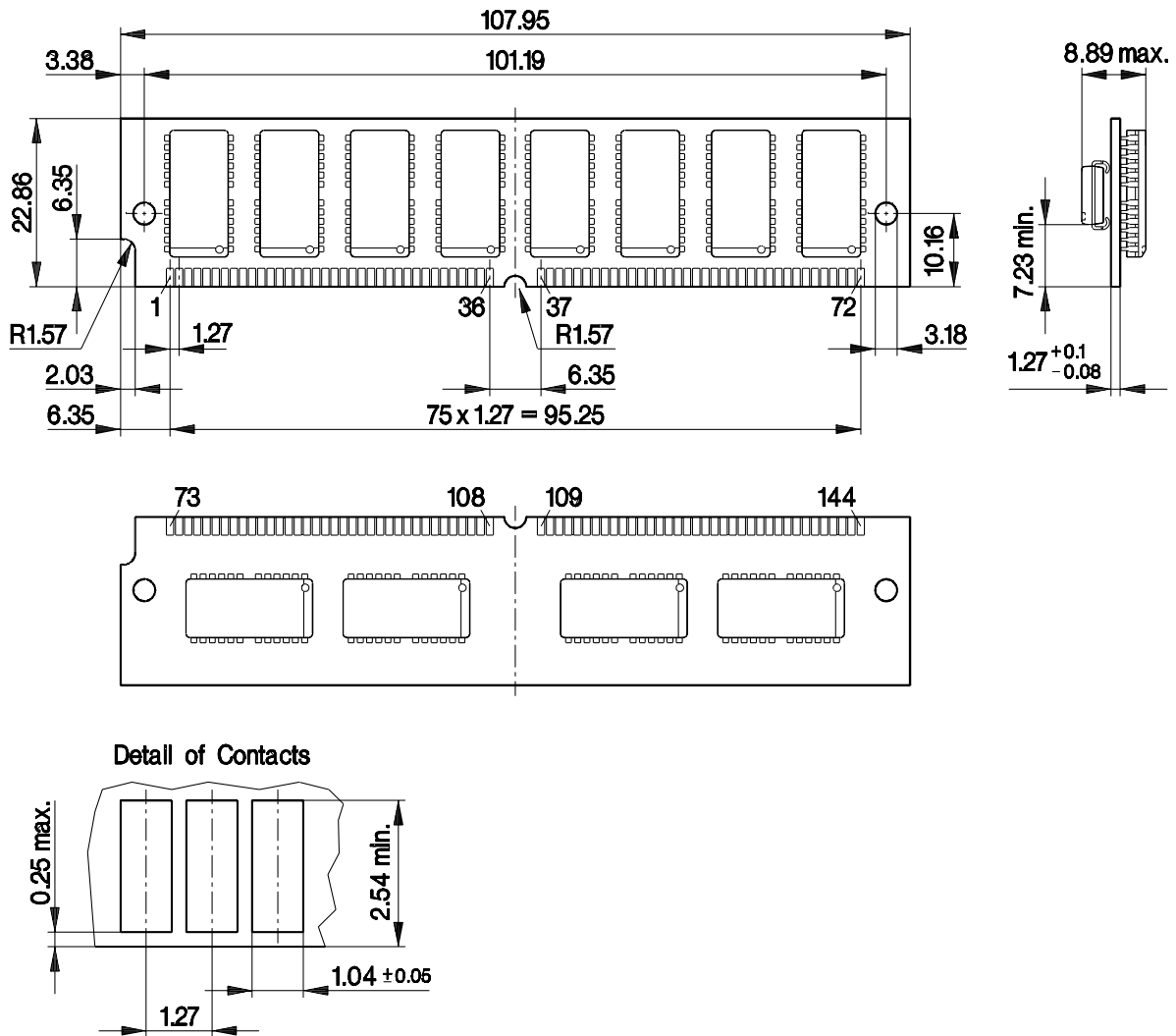


### Notes:

- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while  $RAS = V_{IL}$ . In case of  $I_{CC4}$  it can be changed once or less during a hyper page mode (EDO) cycle.
- 5) An initial pause of 200  $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at  $V_{OL} = 0.8$  V and  $V_{OH} = 2.0$  V. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ .  $t_{CAC}$  is measured from tristate.
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $RAS$  or  $CAS$ , whichever occurs last.
- 13)  $t_{WCS}$  is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the  $\overline{CAS}$  leading edge.

## Package Outline

**L-SIM-72-13**  
(Single In-line Module)



Tolerances: ± 0.13 unless otherwise specified

GLS05967

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm