

Low-Power Mobile VGA EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Generates a low EMI spread spectrum clock of the input frequency.
- Optimized for frequency range from 60 to 175MHz.
- Internal loop filter minimizes external components and board space.
- Four selectable spread ranges.
- Low inherent cycle-to-cycle jitter.
- 3.3V operating voltage range.
- TTL or CMOS compatible inputs and outputs.
- Ultra-low power CMOS design.
- 3.17mA @3.3V, 10MHz | 6.20mA @5.0V, 10MHz
- 4.28mA @3.3V, 14MHz | 7.50mA @5.0V, 14MHz
- 5.50mA @3.3V, 20MHz | 9.50mA @5.0V, 20MHz
- Supports notebook VGA and other LCD timing controller applications.
- SSON/SBM pin for Spread Spectrum On/Off and Standby Mode controls.
- Available in 8-pin SOIC and TSSOP.

down stream clock and data dependent signals. The P1817 allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The P1817 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

The P1817 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

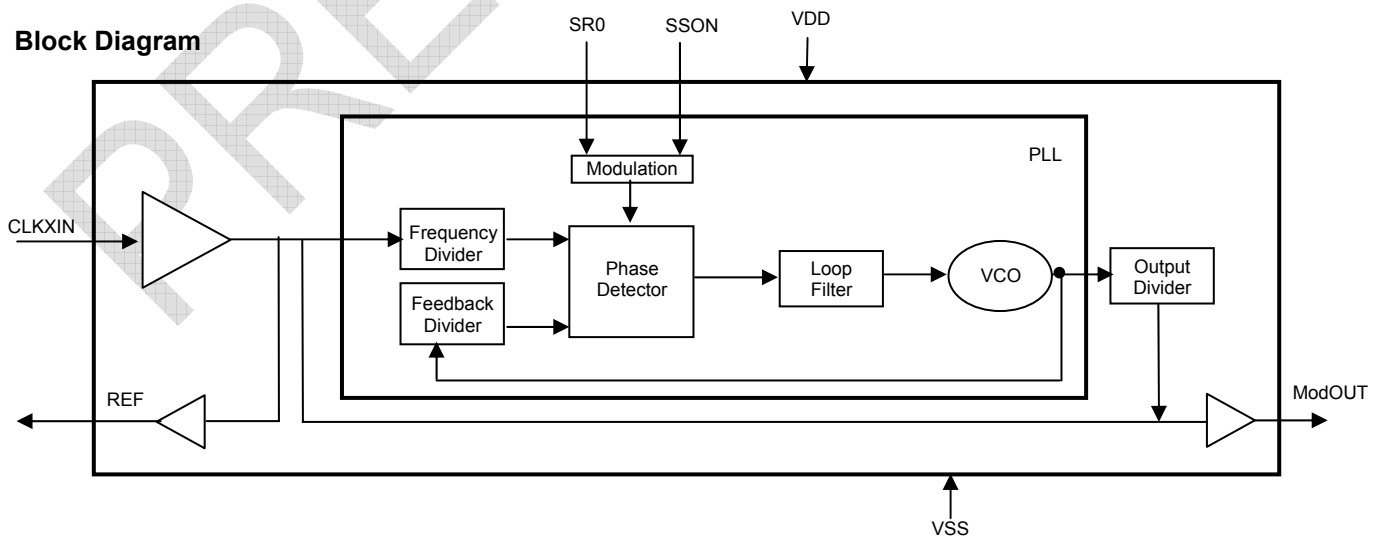
Applications

The P1817 is targeted towards notebook LCD displays, and other displays using an LVDS interface, PC peripheral devices, and embedded systems.

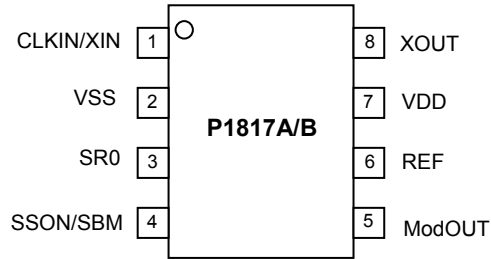
Product Description

The P1817 is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies. The P1817 reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	Connect to externally generated clock signal. To put the part into standby mode, disable the input clock signal to this pin and pull SSON/SBM (pin 5) low. Refer <i>Standby Mode Selection Table</i> .
2	VSS	P	Ground Connection. Connect to system ground.
3	SR0	I	Digital logic input used to select Spreading Range. Refer <i>Spread Spectrum Selection Table</i> . This pin has an internal pull-up resistor.
4	SSON/SBM	I	Spread Spectrum On/Off and standby mode control. Refer <i>Standby Mode Selection Table</i> . This pin has an internal pull-up resistor.
5	ModOUT	O	Spread spectrum clock output or Reference output. Refer <i>Standby Mode Selection Table</i> .
6	REF	O	Reference Output.
7	VDD	P	Connect to +3.3V or 5.0V.
8	XOUT	O	Connect to crystal. No connect if externally generated clock signal is used.

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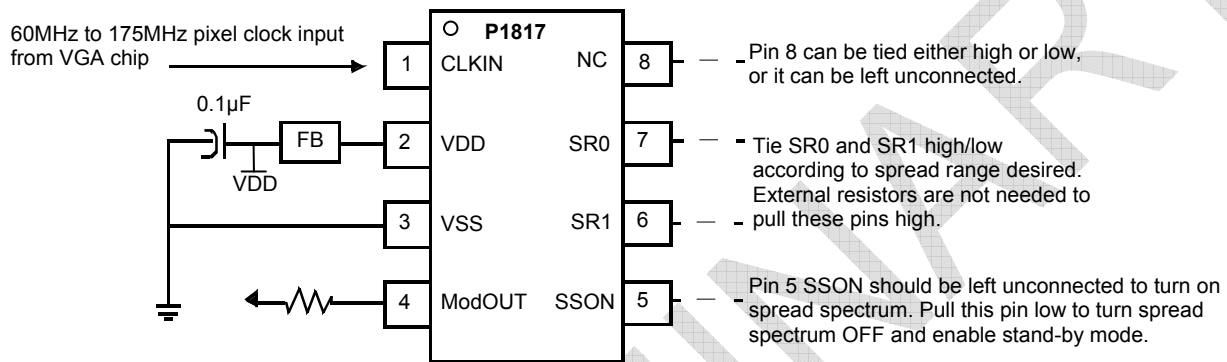
Standby Mode Selection

CLKIN	SSON/SBM	Spread Spectrum	ModOUT	PLL	Mode
Disabled	0	N/A	Disabled	Disabled	Standby
Disabled	1	N/A	Disabled	Free Running	Free Running
Enabled	0	Off	Reference	Disabled	Buffer out
Enabled	1	On	Normal	Normal	Normal

Spread Range Selection, VDD = 5V

SR1	SR0	Spreading Range	Modulation Rate
0	0	± 1.50%	$(F_{IN}/80) * 34.72$ KHz
0	1	± 2.50%	$(F_{IN}/80) * 34.72$ KHz
1	0	± 0.50%	$(F_{IN}/80) * 34.72$ KHz
1	1	± 1.00%	$(F_{IN}/80) * 34.72$ KHz

Schematic for Notebook VGA Application



Note: To set the P1817 to standby mode, disable the input clock (pin 1 CLKIN) and pull SSON (pin 5) low. Refer Standby Mode Selection Table.

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, VIN	Voltage on any pin with respect to GND	-0.5 to +4.6	V
T _{STG}	Storage temperature	-65 to +125	°C
T _A	Operating temperature	0 to 70	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V _{IL}	Input low voltage	GND – 0.3	-	0.8	V
V _{IH}	Input high voltage	2.0	-	VDD + 0.3	V
I _{IL}	Input low current (pull-up resistors on inputs SR0, SR1 and SSON/SBM)	-	-	-35	µA
I _{IH}	Input high current	-	-	35	µA
I _{XOL}	X _{OUT} output low current @ 0.4V, VDD = 3.3V	-	3	-	mA
I _{XOH}	X _{OUT} output high current @ 2.5V, VDD = 3.3V	-	3	-	mA
V _{OL}	Output low voltage VDD = 3.3V, I _{OL} = 20mA	-	-	0.4	V
V _{OH}	Output high voltage VDD = 3.3V, I _{OH} = 20mA	2.5	-	-	V
I _{CC}	Dynamic supply current normal mode 3.3V and 10pF loading	8.46	12	17.78	mA
I _{DD}	Static supply current standby mode	-	0.6	-	mA
VDD	Operating voltage	2.7	3.3	3.7	V
t _{ON}	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
Z _{OUT}	Clock output impedance	-	50	-	Ω

AC Electrical Characteristics

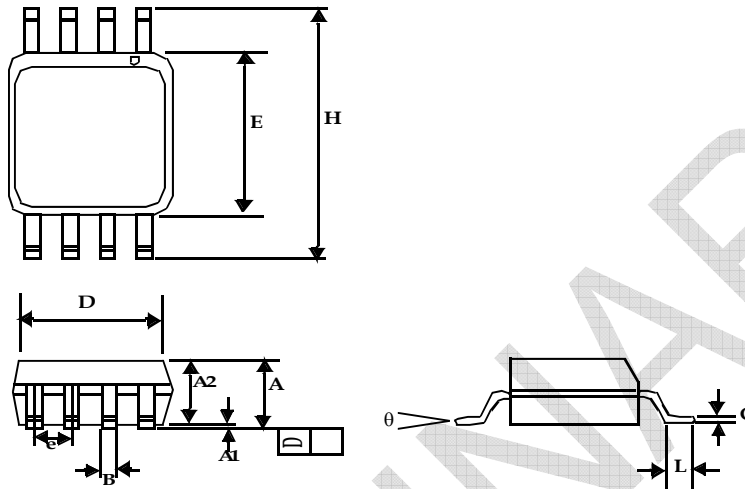
Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	60	-	175	MHz
f_{OUT}	Output frequency	60	-	175	MHz
t_{LH}^*	Output rise time Measured at 0.8V to 2.0V	0.7	0.9	1.1	nS
t_{HL}^*	Output fall time Measured at 0.8V to 2.0V	0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle to cycle)	-	-	360	pS
t_D	Output duty cycle	45	50	55	%

* t_{LH} and t_{HL} are measured into a capacitive load of 15pF

PRELIMINARY

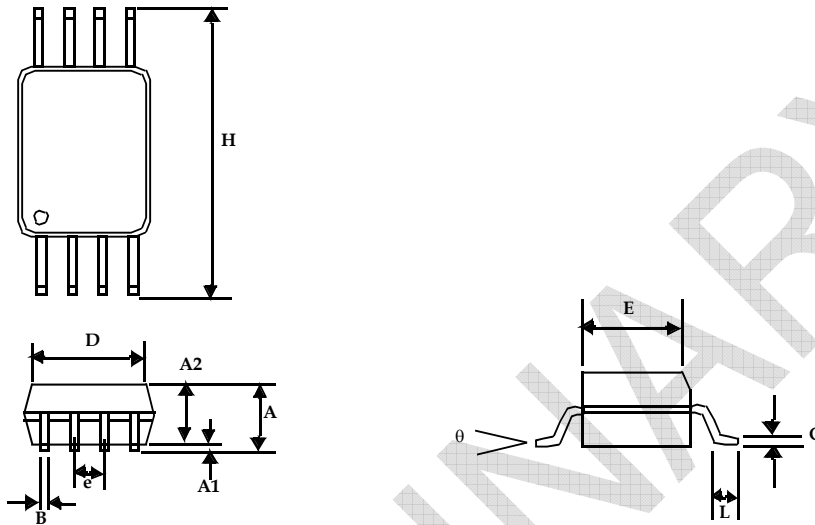
Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

8-lead Thin Shrunk Small Outline Package (4.40-MM Body)



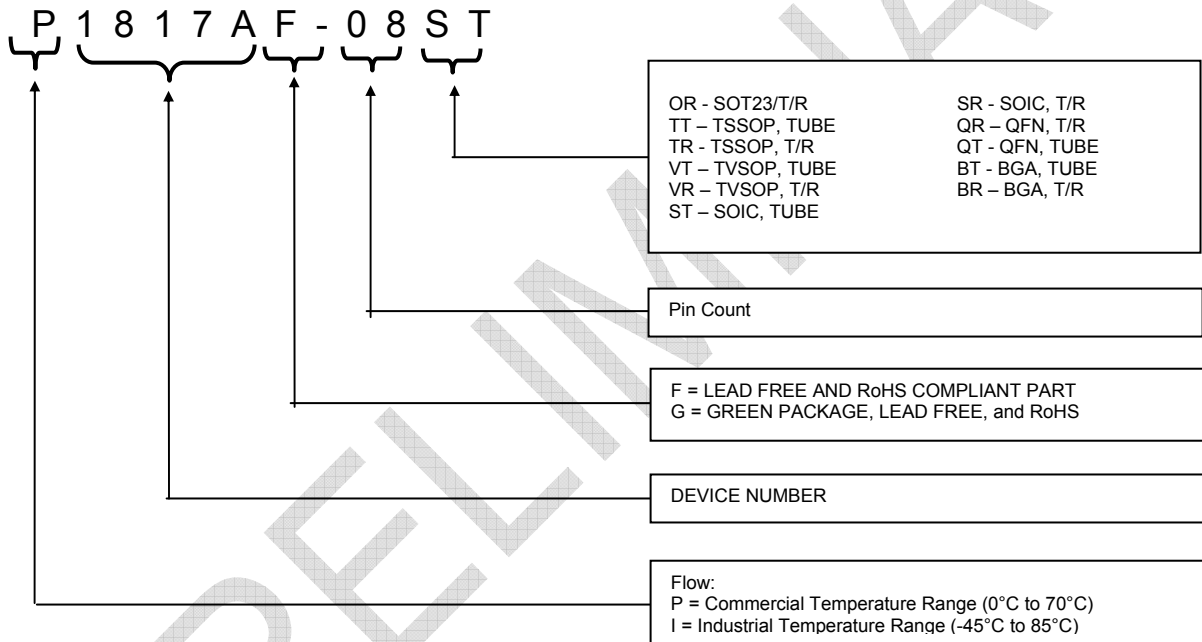
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

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Ordering Codes

Part Number	Marking	Package Type	Pb Free	Temperature
P1817A-08ST	P1817A	8-pin SOIC, tube	No	Commercial
P1817AF-08SR	P1817AF	8-pin SOIC, tape & reel	Yes	Commercial
I1817A-08TT	P1817A	8-pin TSSOP, tube	No	Industrial
I1817AF-08TR	P1817BF	8-pin TSSOP, tape and reel	Yes	Industrial

Device Ordering Information





PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

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Preliminary Information
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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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