ICD2025

Motherboard Clock Generator

Features

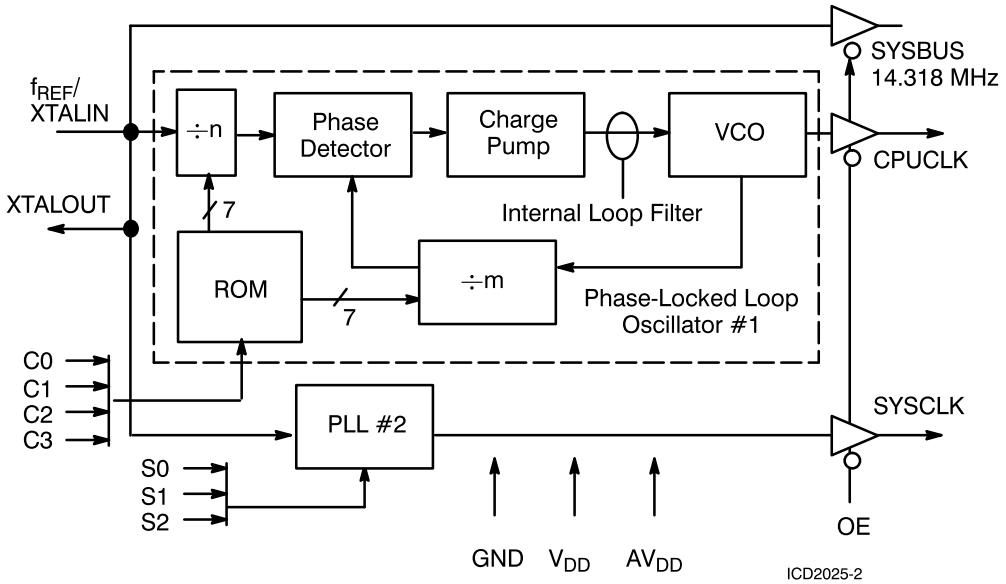
- **Three independent clock outputs: separate CPUCLK, SYSCLK and Buffered Reference Clock**
- **Ideally suited for 386/486 motherboard applications**
- **Phase-locked loop output range of 1.843 MHz – 100 MHz**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package**

Functional Description

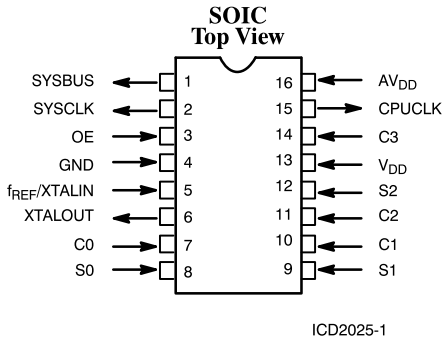
A modern personal computer motherboard often requires many different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit borad space required.

The ICD2025 is a low-cost approach to the generation of the 3 necessary clocks required by any PC motherboard.

Logic Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
SYSBUS	1	Buffered 14.31818 MHz crystal output (z)
SYSCLK	2	System clock output (see *Table 2*)
OE	3	Output Enable three-states output when signal is LO. (pin has internal pull-up)
GND	4	Ground
f_{REF}/ XTALIN[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	6	Oscillator output to a reference crystal.
C0	7	CPUCLK Select signal—Bit 0 (internal pull-up)
S0	8	SYSCLK Clock Select signal—Bit 0 (internal pull-up)
S1	9	SYSCLK Select signal—Bit 1 (internal pull-up)
C1	10	CPUCLK Select signal—Bit 1 (internal pull-up)
C2	11	CPUCLK Select signal—Bit 2 (internal pull-up)
S2	12	SYSCLK Select signal—Bit 2 (internal pull-up)
VDD	13	+5V to I/O Ring
C3	14	CPUCLK Select signal—Bit 3 (internal pull-down)
CPUCLK	15	CPU Clock Output (See CPUCLK Selection Table)
AVDD	16	+5V to Analog Core

Available Frequencies (MHz)

SYSCLK	CPUCLK
1.843	16.000
3.686	20.000
8.000	25.000
12.000	32.000
18.432	33.333
20.000	40.000
24.000	50.000
32.000	66.667
	80.000
	100.000

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

General Considerations

CPU and System Clock Oscillator Selection

The frequency value of the CPU clock output (CPUCLK) is selected by the four CPU clock select inputs: C0, C1, C2, and C3. This feature allows the ICD2025 to support different CPU speeds. The frequency value of the system clock output (SYSCLK) is selected by the three system clock selection inputs: S0, S1, and S2. The selection tables are shown in *Tables 1* and *2* .

At any time during operation, the select lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the 14.31818 MHz reference signal until the PLL settles to the new frequency. The timing for this transition is shown in AC Characteristics.

Table 1. CPUCLK Selection

C3	C2	C1	C0	Word	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	0	40.000	39.812	4734
0	0	0	1	1	80.000	79.623	4734
0	0	1	0	2	33.333	33.322	320
0	0	1	1	3	66.667	66.645	335
0	1	0	0	4	25.000	25.000	0
0	1	0	1	5	50.000	50.000	0
0	1	1	0	6	16.000	15.923	4848
0	1	1	1	7	32.000	31.846	4848
1	0	0	0	8	20.000	19.906	4734
1	0	0	1	9	100.000	99.840	1600
1	0	1	0	10	40.000	39.812	4734
1	0	1	1	11	80.000	79.623	4734
1	1	0	0	12	33.333	33.322	320
1	1	0	1	13	66.667	66.645	335
1	1	1	0	14	25.000	25.000	0
1	1	1	1	15	50.000	50.000	0

Table 2. SYSCLK Selection

S2	S1	S0	Word	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	18.432	18.431	62
0	0	1	1	20.000	20.003	167
0	1	0	2	24.000	23.998	80
0	1	1	3	1.843	1.843	144
1	0	0	4	12.000	11.999	80
1	0	1	5	8.000	8.001	167
1	1	0	6	3.686	3.687	144
1	1	1	7	32.000	32.005	167

Output Frequency Accuracy

The accuracy of the ICD2025 output frequencies depends on the target output frequencies. The tables within this document contain target frequencies that differ from the actual frequencies produced by the clock synthesizer.

The output frequencies of the ICD2025 are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times {}^{P}/_{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2025 always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard system logic requirements. (Actual values are given in the tables.)

Three-State Output Operation

The OE signal, when pulled LOW, will three-state the SYSCLK, CPUCLK, and SYSBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The OE signal contains an internal pull-up but should be tied to V_{DD} if not used.

Short-term stability (also called bit-jitter) is a manifestation of the frequency synthesis process. The Cypress/IC Designs frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the dance of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC Designs families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough for system logic applications.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	ICD2025		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Wxcept crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND		60	mA
I_{ADD}	Analog Power Supply Current			6	mA

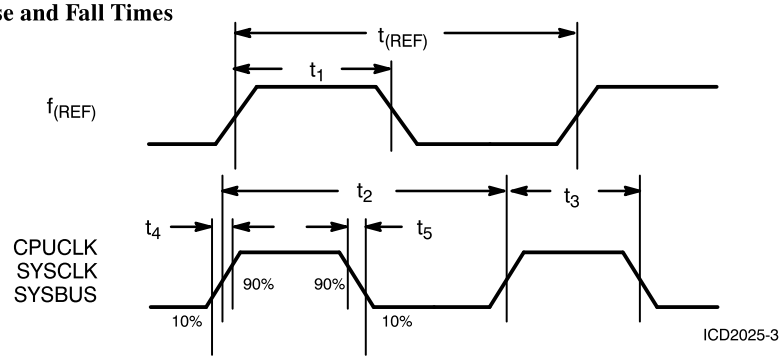
Switching Characteristics Over the Operating Range[2]

Parameter	Name	Drscription	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value	4	14.318	26	MHz
$t_{(REF)}$	Ref Clock Period	$1 \div f_{(REF)}$	38.5	69.8	2500	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	Output Period	CPUCLK output value	10 100 MHz		544 1.84 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_3 \div t_2$ (measured at 2.5V)	40%		60%	
t_4	Rise Time	Rise time for the outputs into a 25 pF load			4	ns
t_5	Fall Time	Fall time for the outputs into a 25 pF load			4	ns
t_6	Three-State	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_7	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_{MUXREF}	Clk Stable	Time required for the outputs to become valid after C0−C3 or S0−S2 select signals change value	3.4	5	6.9	msec
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_8	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	ns
t_9	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	ns

Note:
2. Input capacitance is typically 10 pF, except for the crystal pads.

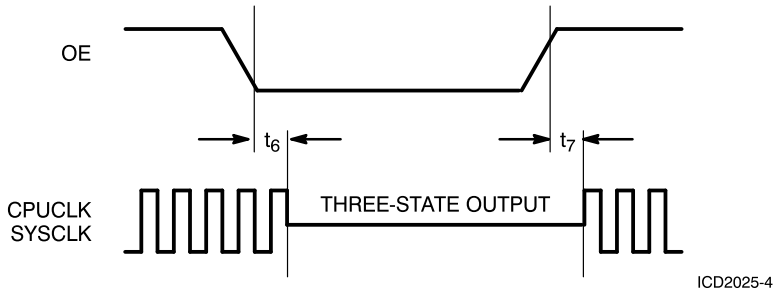
Switching Waveforms

Rise and Fall Times

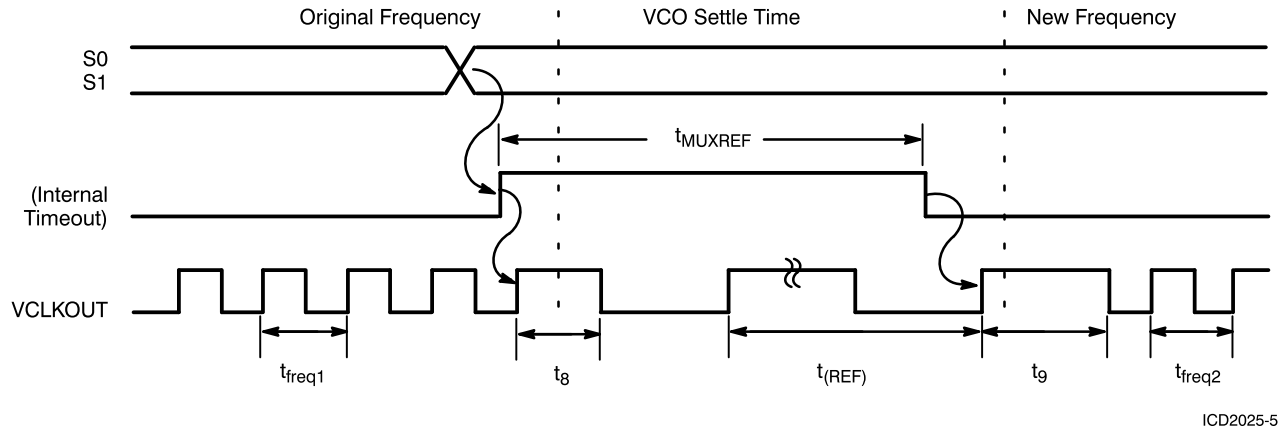


Switching Waveforms (continued)

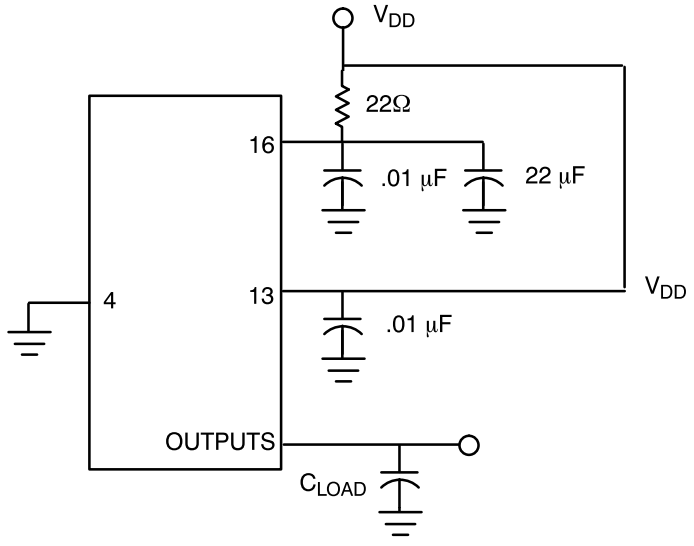
Three-State Timing



Selection Timing



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information[3]

Ordering Code	Package Name	Package Type	Operating Range
ICD2025−	S1	16-Pin SOIC	Commercial[4]

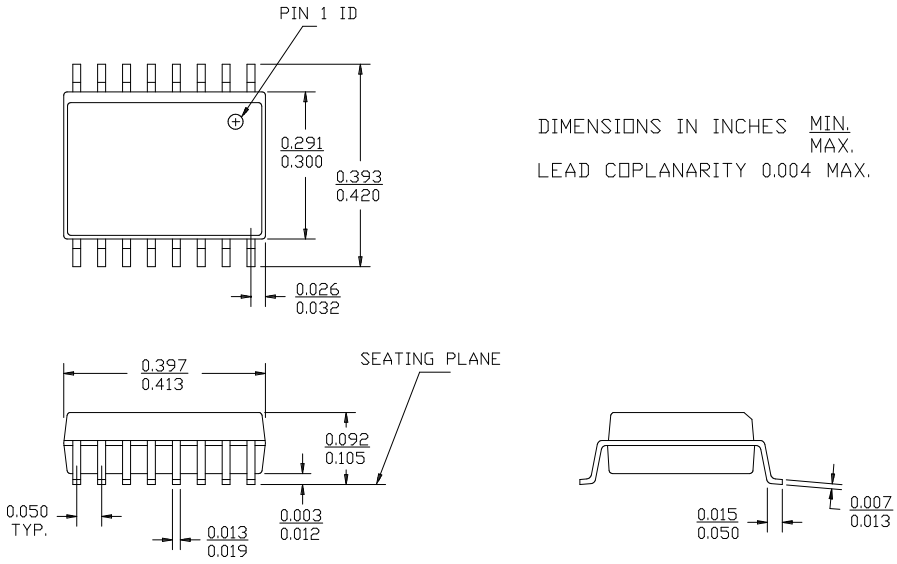
Note:
3. Contact your local Cypress representative.
4. 0°C to +70°C

Example: order ICD2025SC for the ICD2025, 16-pin plastic SOIC, commercial temperature range device.

Document #: 38−00398

Package Diagram

16-Lead Molded SOIC S1



ICD2025-7