ICL7106/7107

3½-Digit Single Chip A/D Converter

FEATURES

- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA typical input current.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV p-p.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

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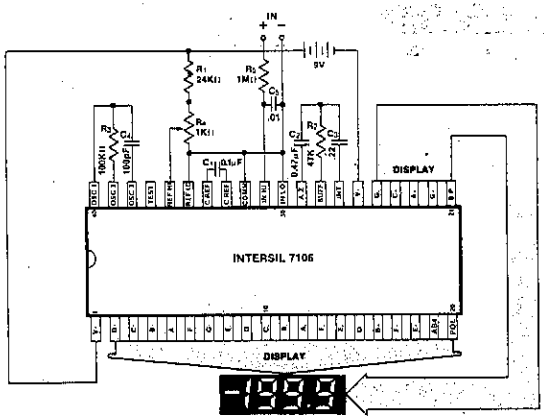
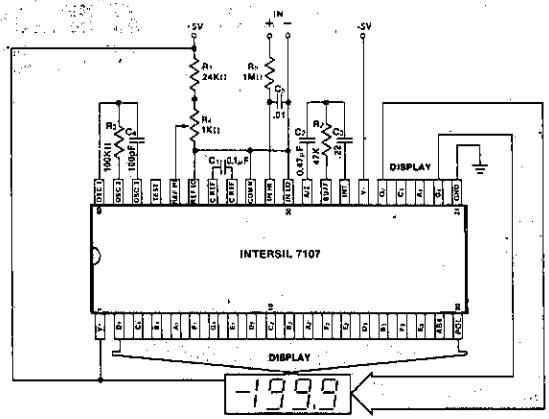
GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.



ICL7106 with Liquid Crystal Display

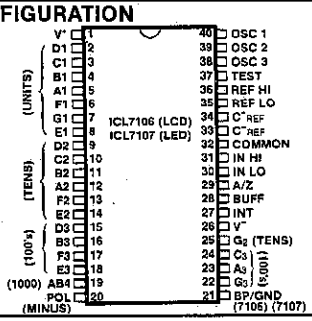


ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current | Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25° C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TEST CIRCUITS

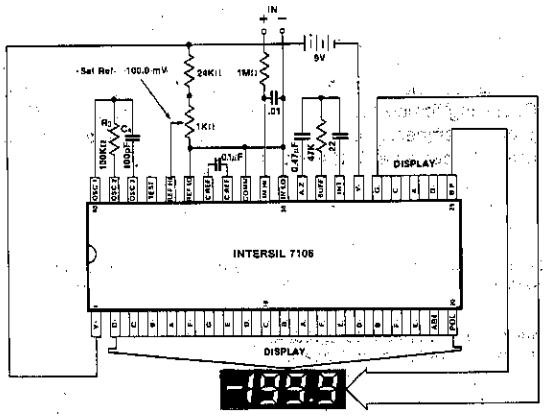


Figure 1: 7106

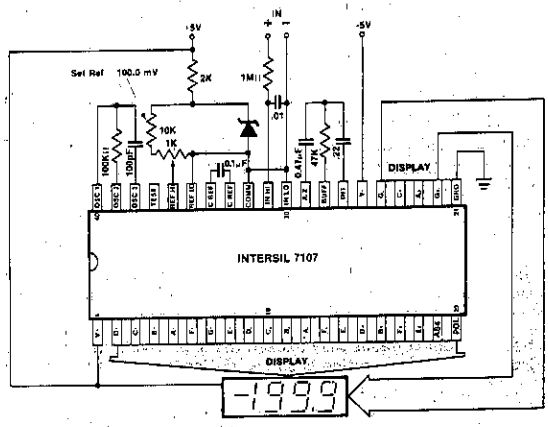


Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

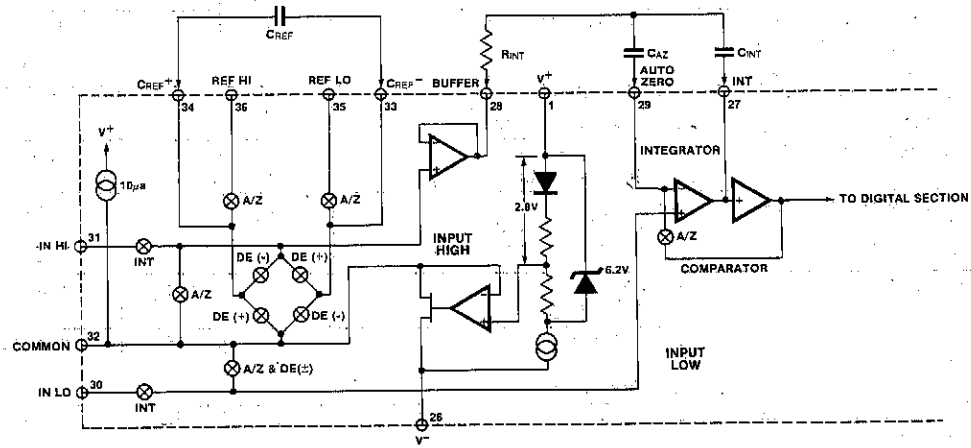


Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{IN}}{V_{REF}})$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

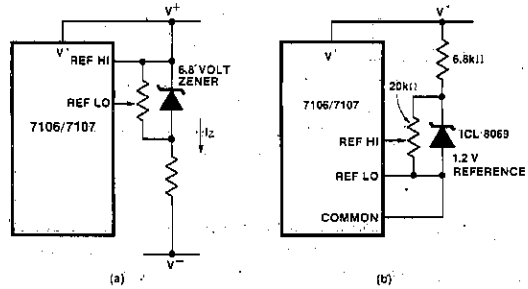


Figure 4: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

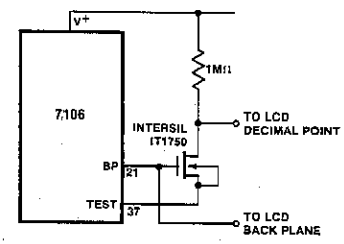


Figure 5: Simple Inverter for Fixed Decimal Point

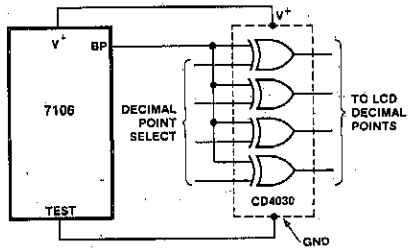


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

4

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

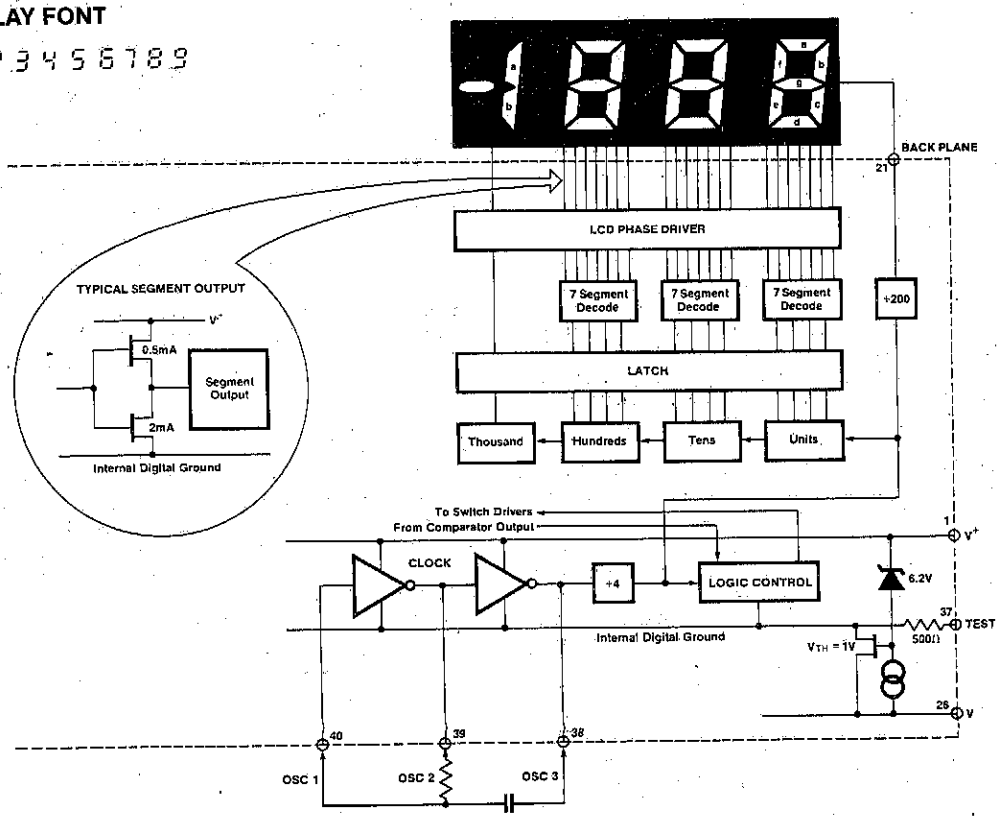


Figure 7: Digital Section 7106

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

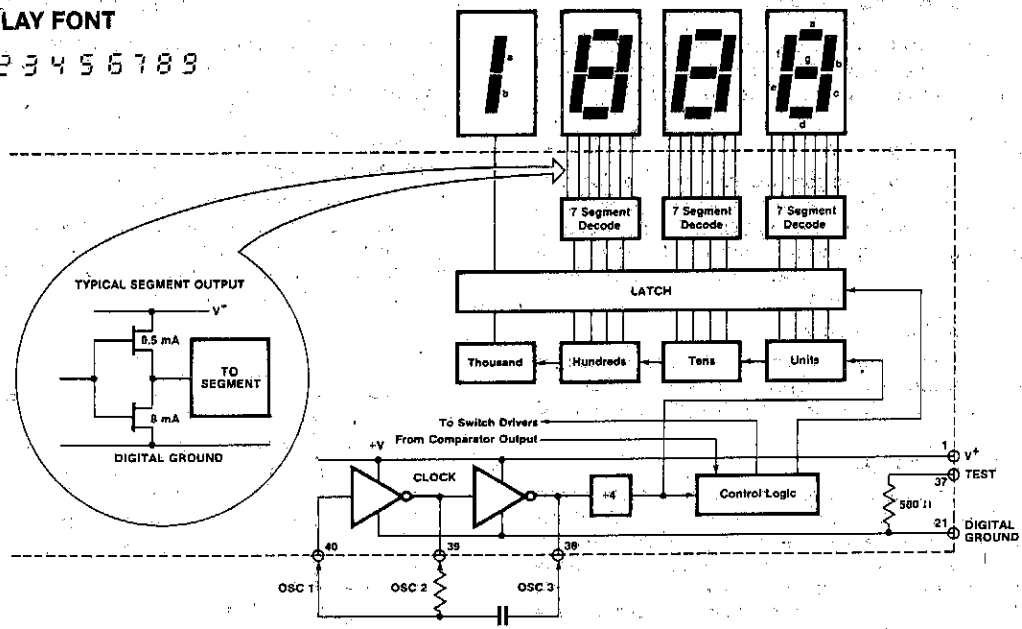


Figure 8: Digital Section 7107

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System Timing

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

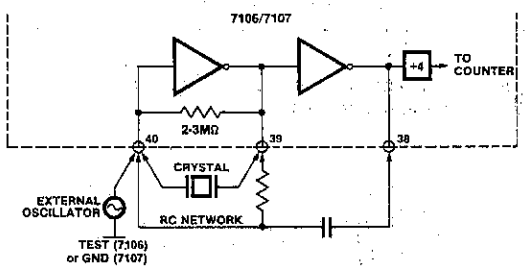

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470KΩ is near optimum and similarly a 47KΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 100KΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = .341V$. Suitable values for integrating resistor and capacitor would be 120KΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this sytem occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

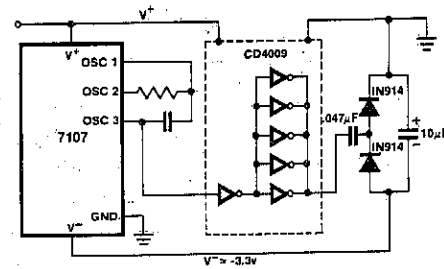

Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

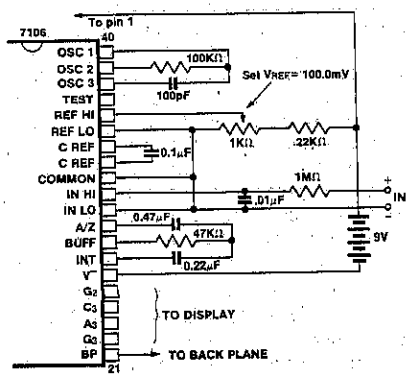

Figure 11: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

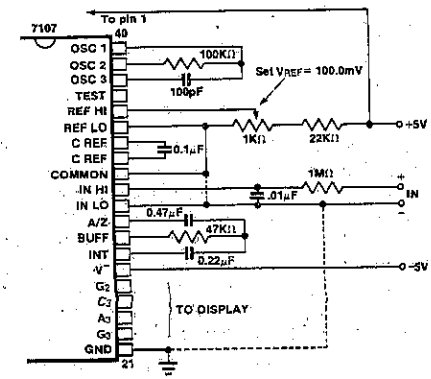

Figure 12: 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

TYPICAL APPLICATIONS (Contd.)

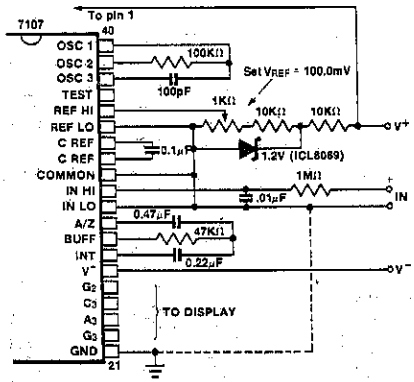

Figure 13: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

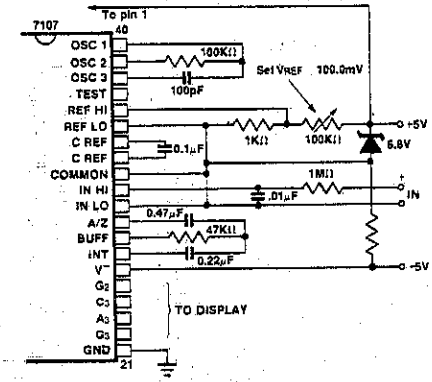

Figure 14: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

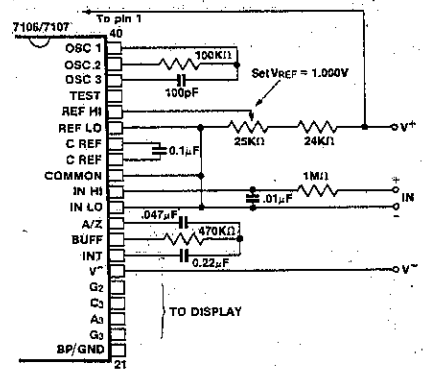

Figure 15: 7106/7107: Recommended component values for 2.000V full scale.

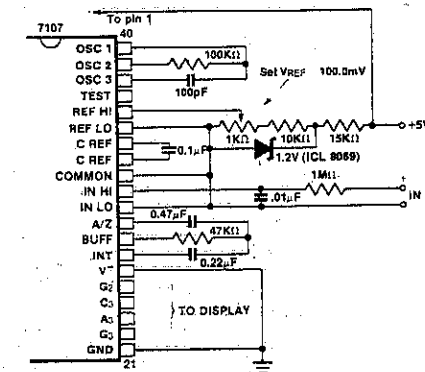

Figure 16: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

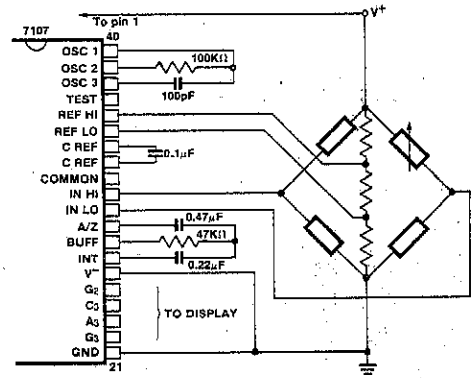

Figure 17: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

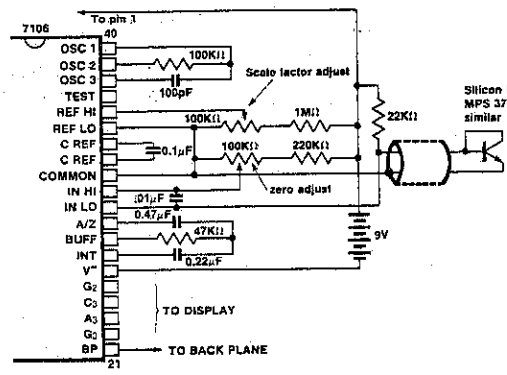

Figure 18: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

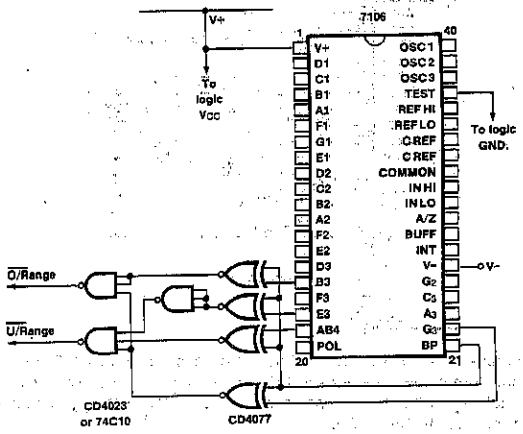

Figure 19: Circuit for developing Underrange and Overrange signals from 7106 outputs.

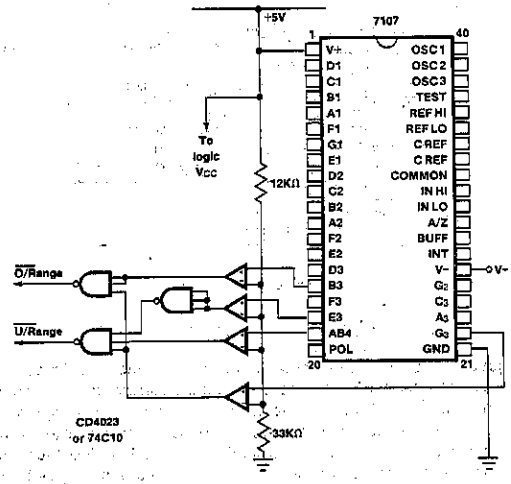

Figure 20: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

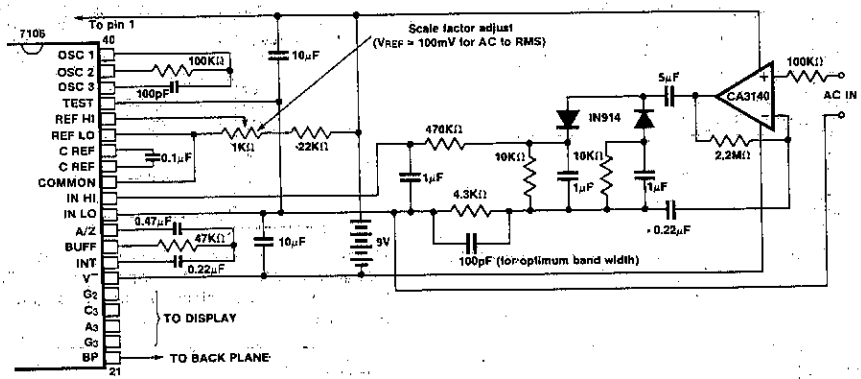

Figure 21: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

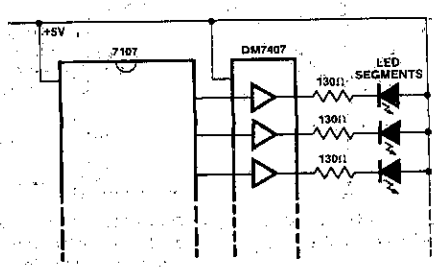

Figure 22: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.