ICM7231, ICM7232

Numeric/Alphanumeric Triplexed LCD Display Drivers

August 1997

Features

- **ICM7231 Drives 8 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**

- **ICM7232 Drives 10 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Serial Format**

- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display are Provided**

- **Display Voltage Independent of Power Supply**

- **On-Chip Oscillator Provides All Display Timing**

- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**

- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**

- **Direct Interface to High-Speed Microprocessors**

Description

The ICM7231 and ICM7232 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high-performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	NUMBER OF DIGITS	INPUT FORMAT	PKG. NO.
ICM7231BFIJL	-25 to 85	40 Ld CERDIP	8 Digit	Parallel	F40.6
ICM7231BFIPL	-25 to 85	40 Ld PDIP	8 Digit	Parallel	E40.6
ICM7232BFIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6
ICM7232CRIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6

NOTE:

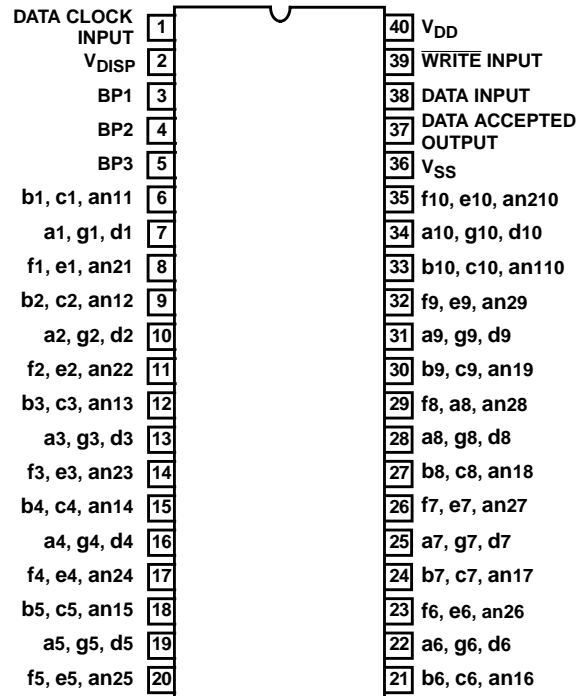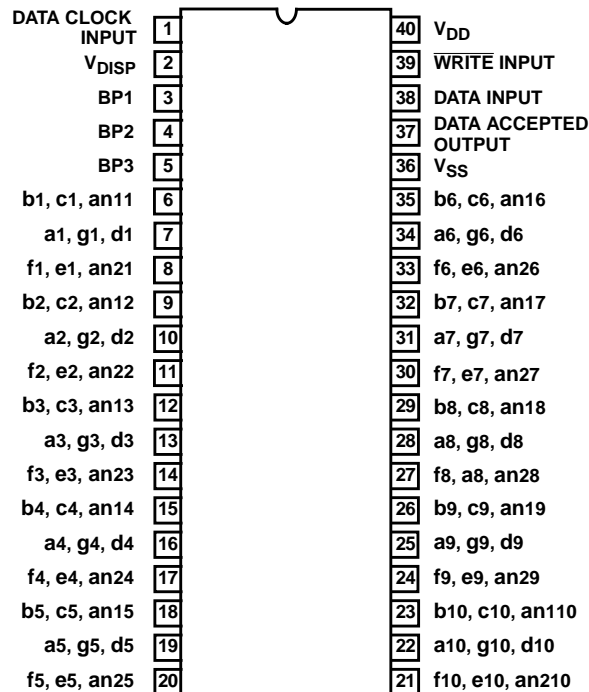All versions intended for triplexed LCD displays.

File Number **3161.1**

Pinouts

ICM7231BF
(PDIP, CERDIP)
TOP VIEW

$\overline{CS}$	1		40	V_{DD}
V_{DISP}	2		39	A2
BP1	3		38	A1
BP2	4		37	A0
BP3	5		36	V_{SS}
b1, c1, an11	6		35	BD3
a1, g1, d1	7		34	BD2
f1, e1, an21	8		33	BD1
b2, c2, an12	9		32	BD0
a2, g2, d2	10		31	AN2
f2, e2, an22	11		30	AN1
b3, c3, an13	12		29	f8, a8, an28
a3, g3, d3	13		28	a8, g8, d8
f3, e3, an23	14		27	b8, c8, an18
b4, c4, an14	15		26	f7, e7, an27
a4, g4, d4	16		25	a7, g7, d7
f4, e4, an24	17		24	b7, c7, an17
b5, c5, an15	18		23	f6, e6, an26
a5, g5, d5	19		22	a6, g6, d6
f5, e5, an25	20		21	b6, c6, an16
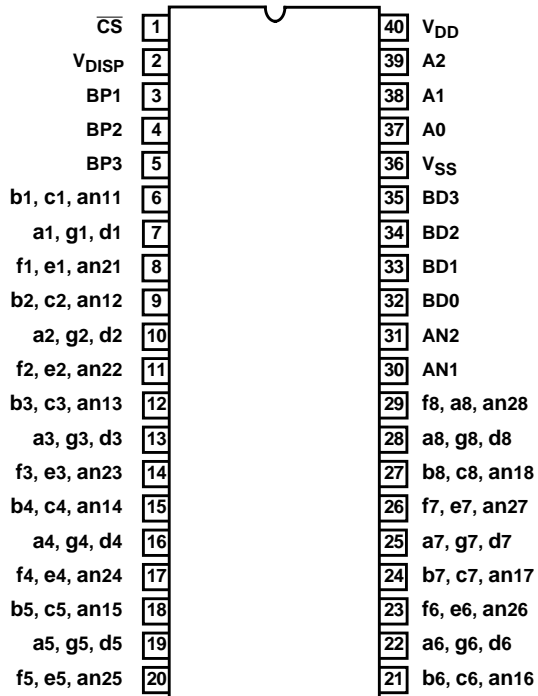
ICM7232AF, BF
(PDIP, CERDIP)
TOP VIEW

DATA CLOCK INPUT	1		40	V_{DD}
V_{DISP}	2		39	$\overline{WRITE}$ INPUT
BP1	3		38	DATA INPUT
BP2	4		37	DATA ACCEPTED OUTPUT
BP3	5		36	V_{SS}
b1, c1, an11	6		35	f10, e10, an210
a1, g1, d1	7		34	a10, g10, d10
f1, e1, an21	8		33	b10, c10, an110
b2, c2, an12	9		32	f9, e9, an29
a2, g2, d2	10		31	a9, g9, d9
f2, e2, an22	11		30	b9, c9, an19
b3, c3, an13	12		29	f8, a8, an28
a3, g3, d3	13		28	a8, g8, d8
f3, e3, an23	14		27	b8, c8, an18
b4, c4, an14	15		26	f7, e7, an27
a4, g4, d4	16		25	a7, g7, d7
f4, e4, an24	17		24	b7, c7, an17
b5, c5, an15	18		23	f6, e6, an26
a5, g5, d5	19		22	a6, g6, d6
f5, e5, an25	20		21	b6, c6, an16

ICM7232CR
(PDIP)
TOP VIEW

DATA CLOCK INPUT	1		40	V_{DD}
V_{DISP}	2		39	$\overline{WRITE}$ INPUT
BP1	3		38	DATA INPUT
BP2	4		37	DATA ACCEPTED OUTPUT
BP3	5		36	V_{SS}
b1, c1, an11	6		35	b6, c6, an16
a1, g1, d1	7		34	a6, g6, d6
f1, e1, an21	8		33	f6, e6, an26
b2, c2, an12	9		32	b7, c7, an17
a2, g2, d2	10		31	a7, g7, d7
f2, e2, an22	11		30	f7, e7, an27
b3, c3, an13	12		29	b8, c8, an18
a3, g3, d3	13		28	a8, g8, d8
f3, e3, an23	14		27	f8, a8, an28
b4, c4, an14	15		26	b9, c9, an19
a4, g4, d4	16		25	a9, g9, d9
f4, e4, an24	17		24	f9, e9, an29
b5, c5, an15	18		23	b10, c10, an110
a5, g5, d5	19		22	a10, g10, d10
f5, e5, an25	20		21	f10, e10, an210

Functional Block Diagrams

ICM7231

D8   D7   D6   D5   D4   D3   D2   D1

f2, e2, an22
a2, g2, d2
b2, c2, an12

f1, e1, an21
a1, g1, d1
b1, c1, an11

SEGMENT LINE DRIVERS 3 WIDE

OUTPUT LATCHES 9 WIDE

V_{DD}

V_H

V_L

V_{DISP}

ON CHIP DISPLAY VOLTAGE LEVEL GENERATOR

PIN 2 (INPUT)

9   9   9   9   9   9   9

9

DIGIT ADDRESS DECODER   EN

DATA DECODER

DATA INPUT LATCHES   EN

ADDRESS INPUT LATCHES   EN

ONE SHOT

$\overline{CS}$

COMMON LINE DRIVERS

BP1

BP2

BP3

DISPLAY TIMING GENERATOR

AN2   BD1   BD3

AN1   BD0   BD2

DATA INPUTS

A0   A1   A2

ADDRESS INPUTS

NOTE: See Figure 13 for display segment connections.

Functional Block Diagrams (Continued)

ICM7232

NOTE: See Figures 13 and 14 for display segment connections.

Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Note 1). . . . . .V_{SS} - 0.3 $\leq$ V_{IN} $\leq$ 6.5
Display Voltage (Note 1). . . . .$0.3 \leq V_{DISP} \leq +0.3$

Operating Conditions

Temperature Range . . . .-25°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	60	N/A
CERDIP Package	50	12

Maximum Junction Temperature
  Ceramic Package . . . . .175°C
  Plastic Package . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . .300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3V below ground, but maybe connected to voltages above V_{DD} but not more than 6.5V above V_{SS}.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications   V+ = 5V +10%, V_{SS} = 0V, T_A = -25°C to 85°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage, V_{DD}		4.5	>4	5.5	V
Data Retention Supply Voltage, V_{DD}	Guaranteed Retention at 2V	2	1.6	-	V
Logic Supply Current, I_{DD}	Current from V_{DD} to Ground Excluding Display. V_{DISP} = 2V	-	30	100	μA
Shutdown Total Current, I_S	V_{DISP} Pin 2 Open	-	1	10	μA
Display Voltage Range, V_{DISP}	$V_{SS} \leq V_{DISP} \leq V_{DD}$	0	-	V_{DD}	V
Display Voltage Setup Current, I_{DISP}	V_{DISP} = 2V, Current from V_{DD} to V_{DISP} On-Chip	-	15	30	μA
Display Voltage Setup Resistor Value, R_{DISP}	One of Three Identical Resistors in String	40	75	-	kΩ
DC Component of Display Signals	(Sample Test Only)	-	$^1/_4$	1	%(V_{DD}-V_{DISP})
Display Frame Rate, f_{DISP}	See Figure 5	60	90	120	Hz
Input Low Level, V_{IL}	ICM7231, Pins 30 - 35, 37 - 39, 1	-	-	0.8	V
Input High Level, V_{IH}	ICM7232, Pins 1, 38, 39 (Note 2)	2.0	-	-	V
Input Leakage, I_{ILK}		-	0.1	1	μA
Input Capacitance, C_{IN}		-	5	-	pF
Output Low Level, V_{OL}	Pin 37, ICM7232, I_{OL} = 1mA	-	-	0.4	V
Output High Level, V_{OH}	V_{DD} = 4.5V, I_{OH} = -500μA	4.1	-	-	V
Operating Temperature Range, T_{OP}	Industrial Range	-25	-	+85	^{o}C

AC Specifications V_{DD} = 5V +10% V_{SS} = 0V, -25°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL INPUT (ICM7231) See Figure 1					
Chip Select Pulse Width, t_{CS}	(Note 1)	500	350	-	ns
Address/Data Setup Time, t_{DS}	(Note 1)	200	-	-	ns
Address/Data Hold Time, t_{DH}	(Note 1)	0	-20	-	ns
Inter-Chip Select Time, t_{ICS}	(Note 1)	3	-	-	μs
SERIAL INPUT (ICM7232) See Figures 2, 3					
Data Clock Low Time, $t_{\overline{CL}}$	(Note 1)	350	-	-	ns
Data Clock High Time, t_{CL}	(Note 1)	350	-	-	ns
Data Setup Time, t_{DS}	(Note 1)	200	-	-	ns
Data Hold Time, t_{DH}	(Note 1)	0	-20	-	ns
Write Pulse Width, t_{WP}	(Note 1)	500	350	-	ns
Write Pulse to Clock at Initialization, t_{WLL}	(Note 1)	1.5	-	-	μs
Data Accepted Low Output Delay, t_{ODL}	(Note 1)	-	200	400	ns
Data Accepted High Output Delay, t_{ODH}	(Note 1)	-	1.5	3	μs
Write Delay After Last Clock, t_{CWS}	(Note 1)	350	-	-	ns

Table of Features

TYPE NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231BF	Code B	Both Annunciators on BP3	Parallel Entry, 4-bit Data, 2-bit Annunciators, 3-bit Address	8 Digits plus 16 Annunciators
ICM7232AF	Hexadecimal	Both Annunciators on BP3	Serial Entry, 4-bit Data, 2-bit Annunciators, 4-bit Address	10 Digits plus 20 Annunciators
ICM7232BF	Code B			
ICM7232CR	Code B	1 Annunciator BP1 1 Annunciator BP3		

Terminal Definitions

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
ICM7231 PARALLEL INPUT NUMERIC DISPLAY				
AN1	30	Annunciator 1 Control Bit	High = ON	
AN2	31	Annunciator 2 Control Bit	Low = OFF	See Table 3
BD0	32	Least Significant	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
BD1	33	4-bit Binary Data Inputs		
BD2	34			
BD3	35	Most Significant		
A0	37	Least Significant	Input Address (See Table 2)	
A1	38	3-bit Digit Address Inputs		
A2	39	Most Significant		
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 2)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	
ICM7232 SERIAL DATA AND ADDRESS INPUT				
Data Input	38	Data+ Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (O)	
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of $\overline{WRITE}$ causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.	
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic.	
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register.	
ALL DEVICES				
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD}) chip is shutdown; oscillator stops, all display pins to V_{DD}.	
Common Line Driver Outputs	3, 4, 5		Drive display commons, or rows	
Segment Line Driver Outputs	6 - 29 6 - 35	(On ICM7231) (On ICM7232)	Drive display segments, or columns.	
V_{DD}	40	Chip Positive Supply		
V_{SS}	36	Chip Negative Supply		

NOTES:

1. For Design reference only, not 100% tested.

2. $\overline{CS}$ has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several ms. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

Timing Diagrams
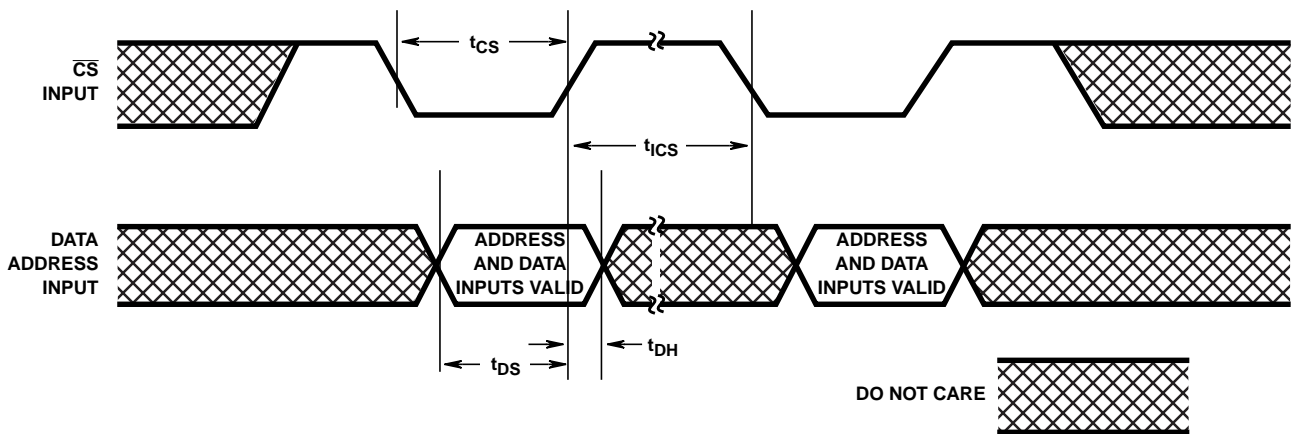
FIGURE 1. ICM7231 INPUT TIMING DIAGRAM
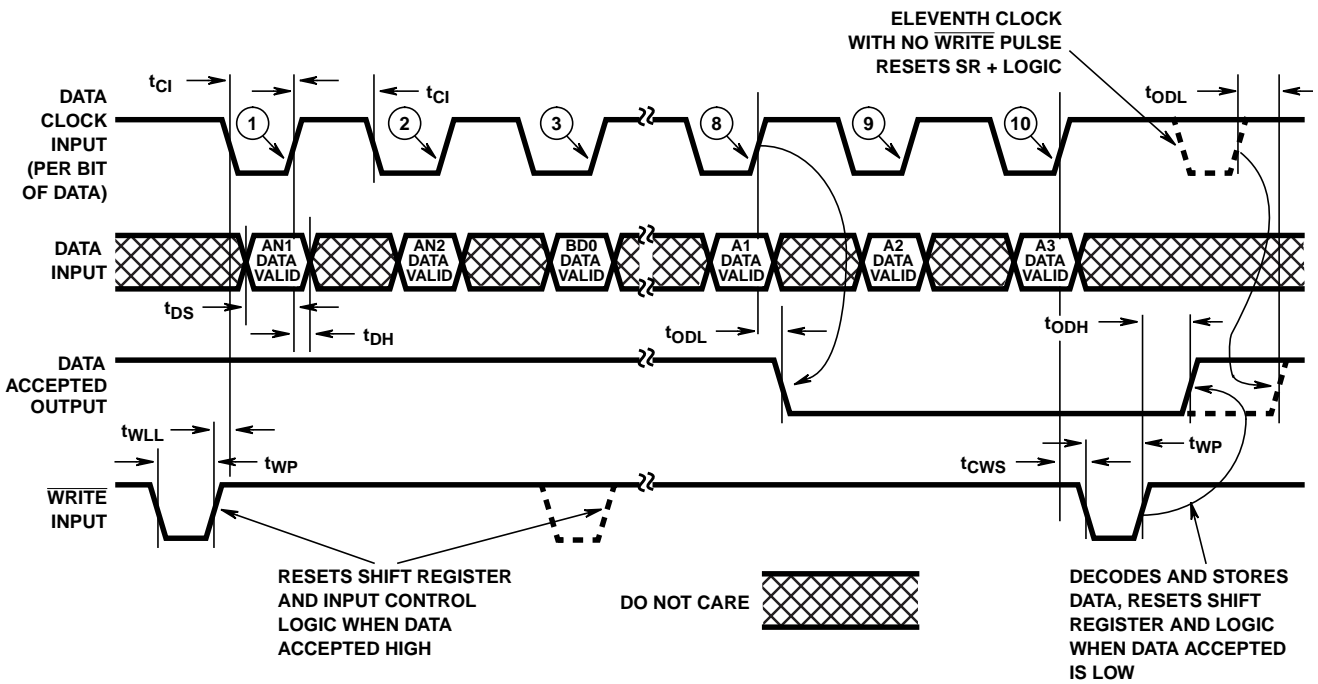
FIGURE 2. ICM7232 ONE DIGIT INPUT TIMING DIAGRAM, WRITING BOTH ANNUNCIATORS

Timing Diagrams

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A0	A1	A2	A3 ENTER LAST

ICM7232 WRITE ORDER

DO NOT CARE

RESETS SHIFT REGISTER AND INPUT CONTROL LOGIC WHEN DATA ACCEPTED HIGH

DECODES AND STORES DATA, RESETS SHIFT REGISTER AND LOGIC WHEN DATA ACCEPTED IS LOW
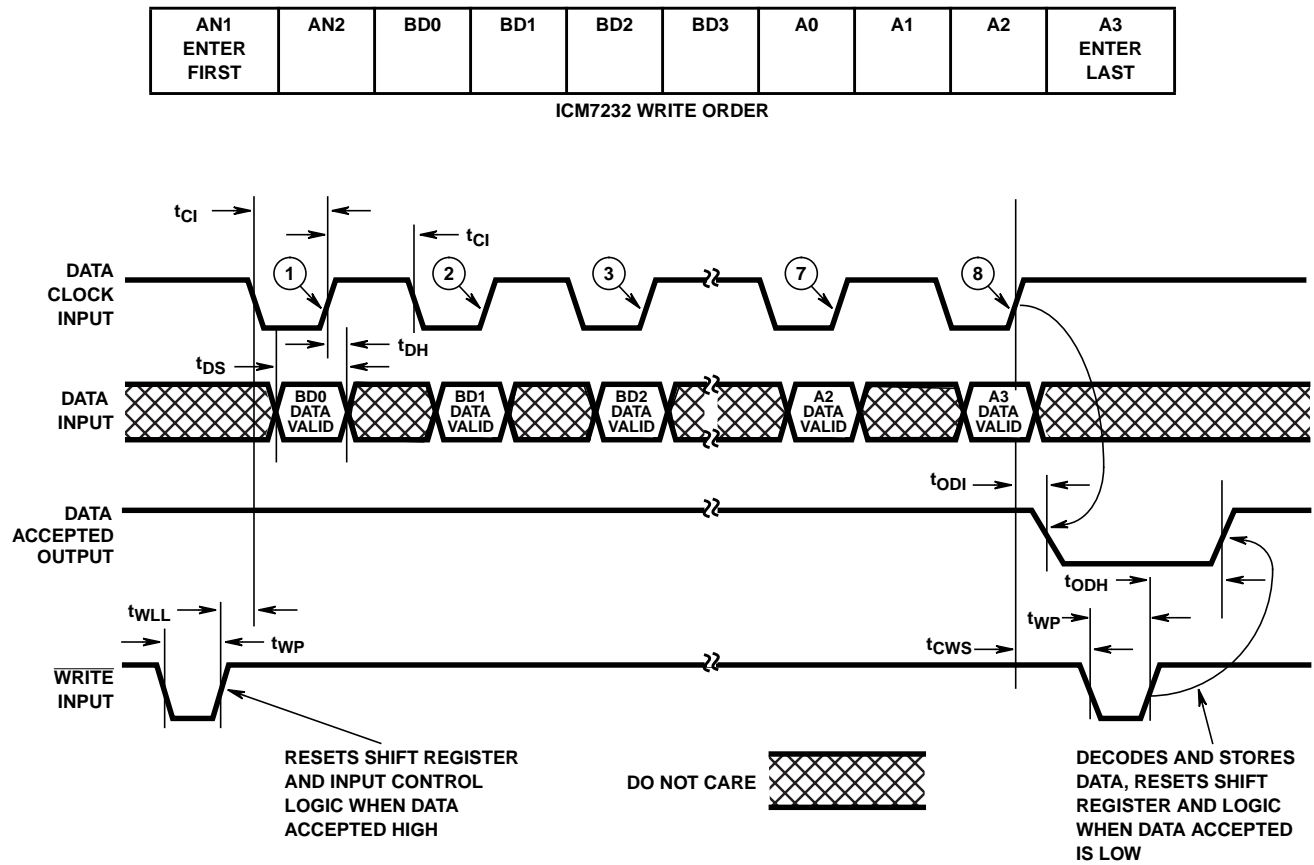
FIGURE 3. ICM7232 INPUT TIMING DIAGRAM, LEAVING BOTH ANNUNCIATORS OFF

ICM7231 Family Description

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil' MAXCMOS® process and all inputs are protected against static discharge.

Triplexed ($^1/_3$ Multiplexed) Liquid Crystal Displays

Figure 4 shows the connection diagram for a typical 7-segment display with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 5 shows the voltage waveforms of the common lines

and one segment line, chosen for this example to be the "a, g, d" segment line. This line intersects with BP1 to form the "a" segment, BP2 to form the "g" segment and BP3 to form the "d" segment. Figure 5 also shows the waveform of the "a, g, d" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 6. Figure 7 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments used in Figure 5.

SEGMENT LINES

SEGMENT LINE CONNECTIONS

BACKPLANE CONNECTIONS
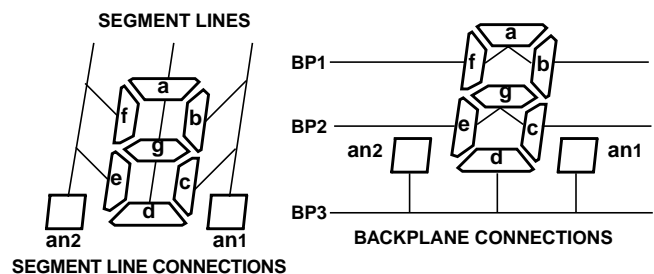
FIGURE 4. CONNECTION DIAGRAMS FOR TYPICAL 7-SEGMENT DISPLAYS
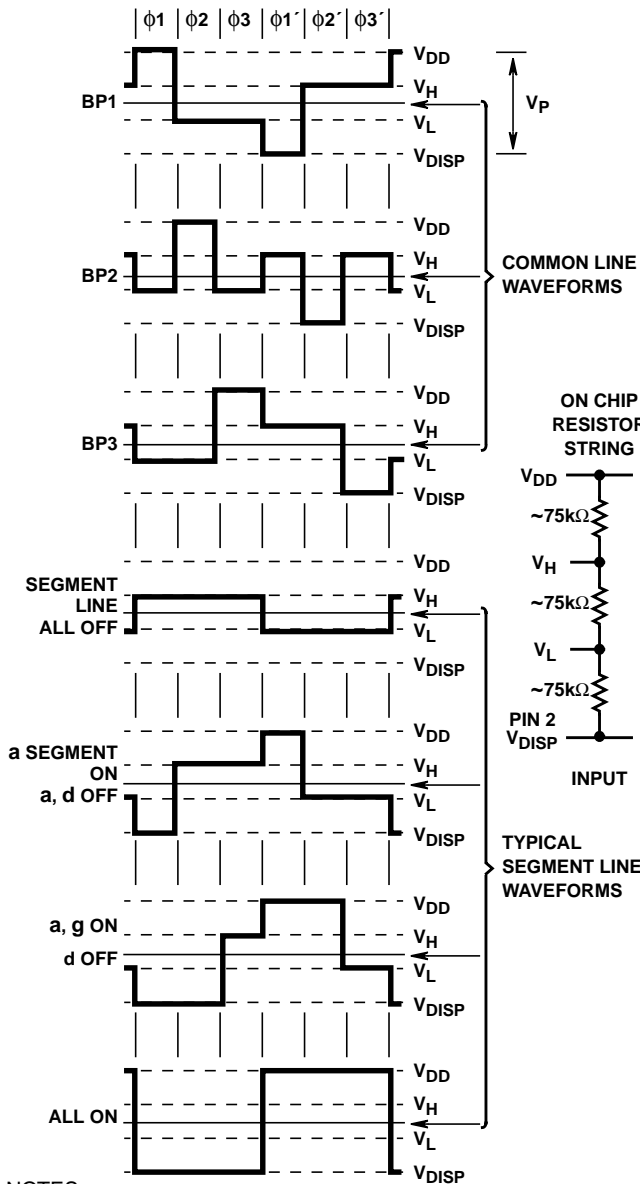
MAXCMOS® is a registered trademark of Intersil Corporation.

FIGURE 5. DISPLAY VOLTAGE WAVEFORMS

NOTES:

1. φ1, φ2, φ3, - BP High with Respect to Segment.

2. φ1´, φ2´, φ3´, - BP Low with Respect to Segment.

3. BP1 Active during φ1, and φ1´.

4. BP2 Active during φ2, and φ2´.

5. BP3 Active during φ3, and φ3´.

FIGURE 6. DISPLAY SCHEMATIC

$$VP = (V+) - VDISP$$

$$V_{RMS} = \frac{VP}{3} = V_{RMS}OFF$$

$$V_{RMS} = \frac{\sqrt{11}}{\sqrt{3}} \times \frac{VP}{3} = V_{RMS}ON$$
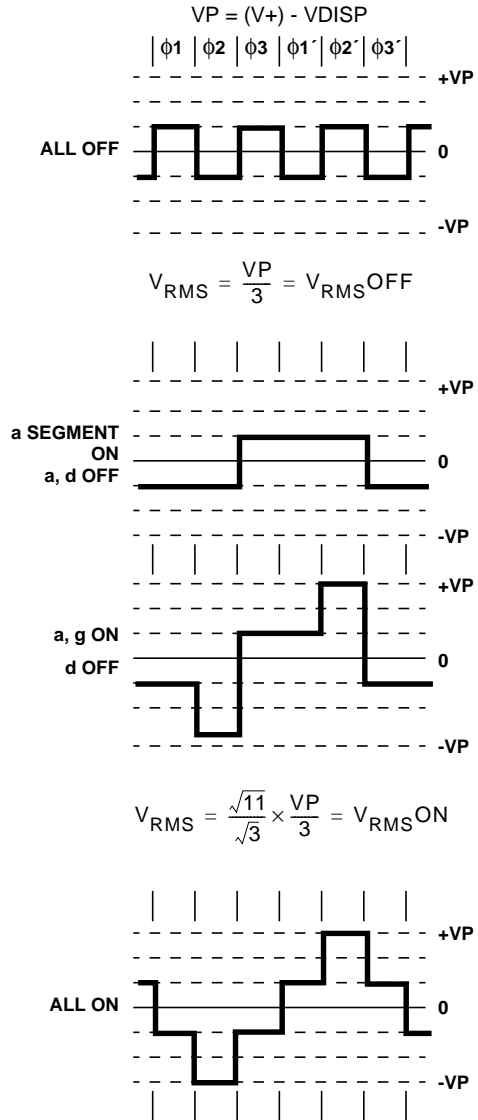
$$\text{Voltage Contrast Ratio} = \frac{V_{RMS}ON}{V_{RMS}OFF} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 7 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always $1.92V_{PEAK}/3$.

For a $^1/_3$ multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

NOTES:

1. φ1, φ2, φ3, - BP High with Respect to Segment.

2. φ1´, φ2´, φ3´, - BP Low with Respect to Segment.

3. BP1 Active during φ1, and φ1´.

4. BP2 Active during φ2, and φ2´.

5. BP3 Active during φ3, and φ3´.

FIGURE 7. VOLTAGE WAVEFORMS ON SEGMENT g(V_G)

Figure 8 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for V_{PEAK} = 3.1V, a typical value for $^1/_3$ multiplexed displays in calculators. Note that the RMS OFF voltage $V_{PEAK}/3 \approx$ 1V is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.
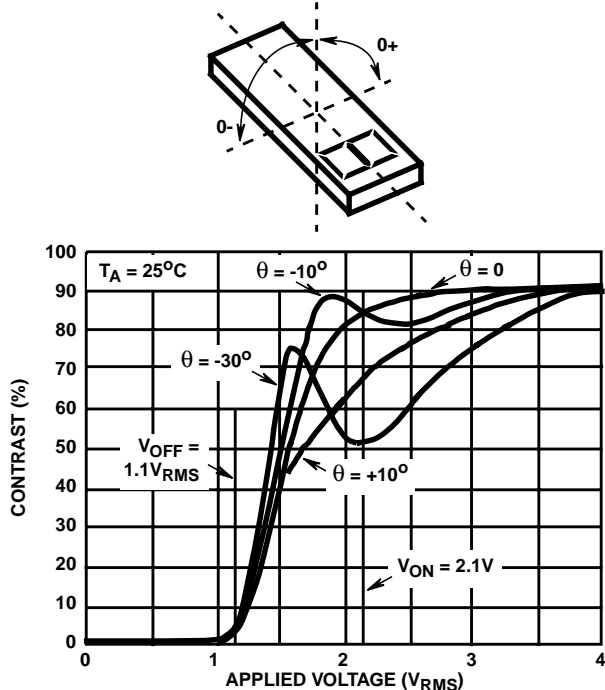
FIGURE 8. CONTRAST vs APPLIED RMS VOLTAGE

All members of the ICM7231 and ICM7232 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_{PEAK} = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS}. This can cause device latchup and destruction of the chip.

Temperature Effects and Temperature Compensation

The performance of the LCD material is affected by temperature in two ways. The response time of the display to changes of applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. At high temperature, the effect to consider deals with plastic materials used to make the polarizer.

Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P when the threshold voltage drops below $V_{PEAK}/3$ OFF segments begin to be visible. Figure 9 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 8.
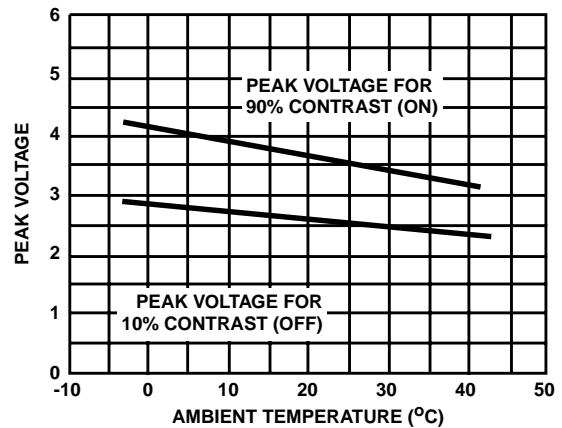
FIGURE 9. TEMPERATURE DEPENDENCE OF LC THRESHOLD

For applications where the display temperature does not vary widely, V_{PEAK} may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_{PEAK}/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_{PEAK}) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

Display Voltage and Temperature Compensation

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 10. A potentiometer with a maximum value of 200kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.
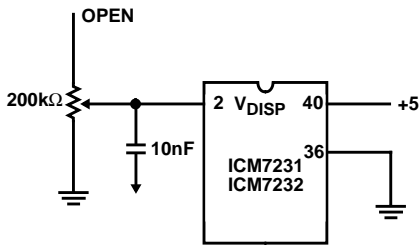
FIGURE 10. SIMPLE DISPLAY VOLTAGE ADJUSTMENT

Figure 11A shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 4 and 5. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2mV/^{o}C; five in series gives -10mV/^{o}C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 11B allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2mV/^{o}C) is also multipled. The transistor should have a beta of at least 100 with a collector current of 10μA. The inexpensive 2N2222 shown in the figure is a suitable device.
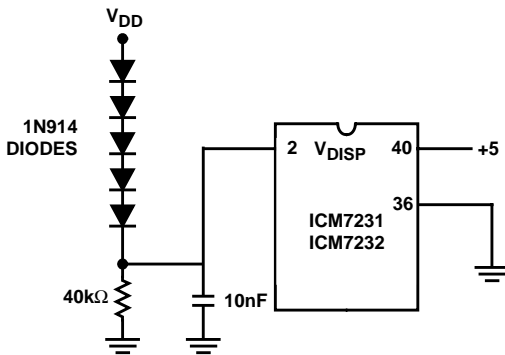
FIGURE 11A. STRING OF DIODES
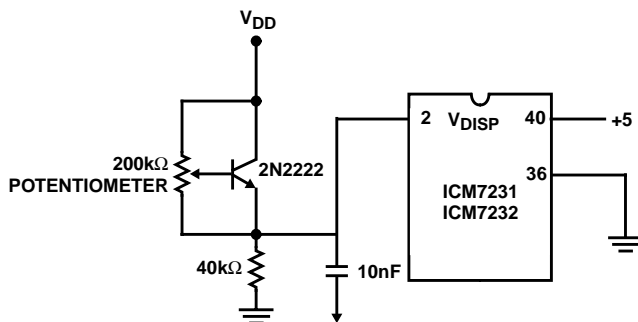
FIGURE 11B. TRANSISTOR-MULTIPLIER

FIGURE 11. DIODE-BASED TEMPERATURE COMPENSATION

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3 - 4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS}. The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663S, as shown in Figure 12. This circuit allows independent adjustment of both voltage and temperature compensation.
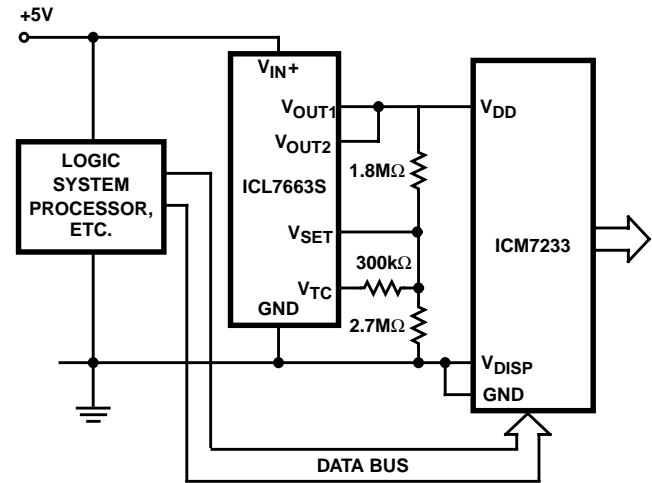

FIGURE 12. FLEXIBLE TEMPERATURE COMPENSATION

Description Of Operation

Parallel Input Of Data And Address (ICM7231)

The parallel input structure of the ICM7231 device is organized to allow simple, direct interfacing to all microprocessors, (see the Functional Block Diagram). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input.

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input device are shown in Figure 1, with the values for setup, hold, and pulse width times shown in the AC Specifications section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

Serial Input Of Data And Address (ICM7232)

The ICM3232 trades six pins used as data inputs on the ICM7231 for six more segment lines, allowing two more 9-segment digits. This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to Functional Block Diagram and timing diagrams, Figures 2 and 3. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{WRITE}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the

DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the WRITE input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 2. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 3.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial Input devices, it is possible to address digits/characters which don't exist. As shown in Table 2 when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

Display Fonts and Output Codes

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on BP3. The display connections for one digit of this display are shown in Figure 13. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on BP1 and the right hand annunciator (usually a decimal point) on BP3. (See Figure 14). The "C" devices provide only a "Code B" output for the 7 segments.

TABLE 1. BINARY DATA DECODING ICM7231 AND ICM7232

CODE INPUT				DISPLAY OUTPUT	
BD3	BD2	BD1	BD0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	–
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

TABLE 2. ADDRESS DECODING (ICM7231 AND ICM7232)

CODE INPUT				DISPLAY OUTPUT
ICM7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CODE INPUT		DISPLAY OUTPUT	
AN2	AN1	ICM7231A AND ICM7231B ICM7232A AND ICM7232B BOTH ANNUNCIATORS ON BP3	ICM7231C ICM7232C an2 ANNUNCIATOR BP1 an1 ANNUNCIATOR BP3
0	0		
0	1		
1	0		
1	1		

SEGMENT LINES

SEGMENT LINE CONNECTIONS

BACKPLANE CONNECTIONS
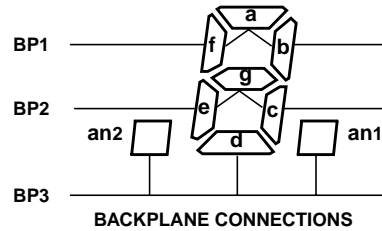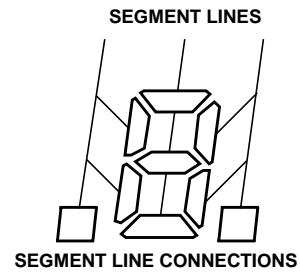
FIGURE 13. ICM7231 AND ICM7232 DISPLAY FONTS ("A" AND "B" SUFFIX VERSIONS)

SEGMENT LINES

(NOTE 1)

SEGMENT LINE CONNECTIONS

SEGMENT LINES

BACKPLANE CONNECTIONS
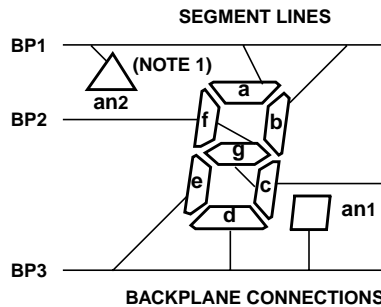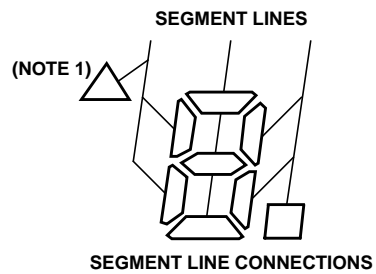
NOTE:

1. Annunciators can be: STOP , GO , △ , ↑ -arrows that point to information printed around the display opening etc., whatever the designer display opening etc., whatever the designer chooses to incorporate in the liquid crystal display.

FIGURE 14. ICM7231 DISPLAY FONTS ("C" SUFFIX VERSIONS)
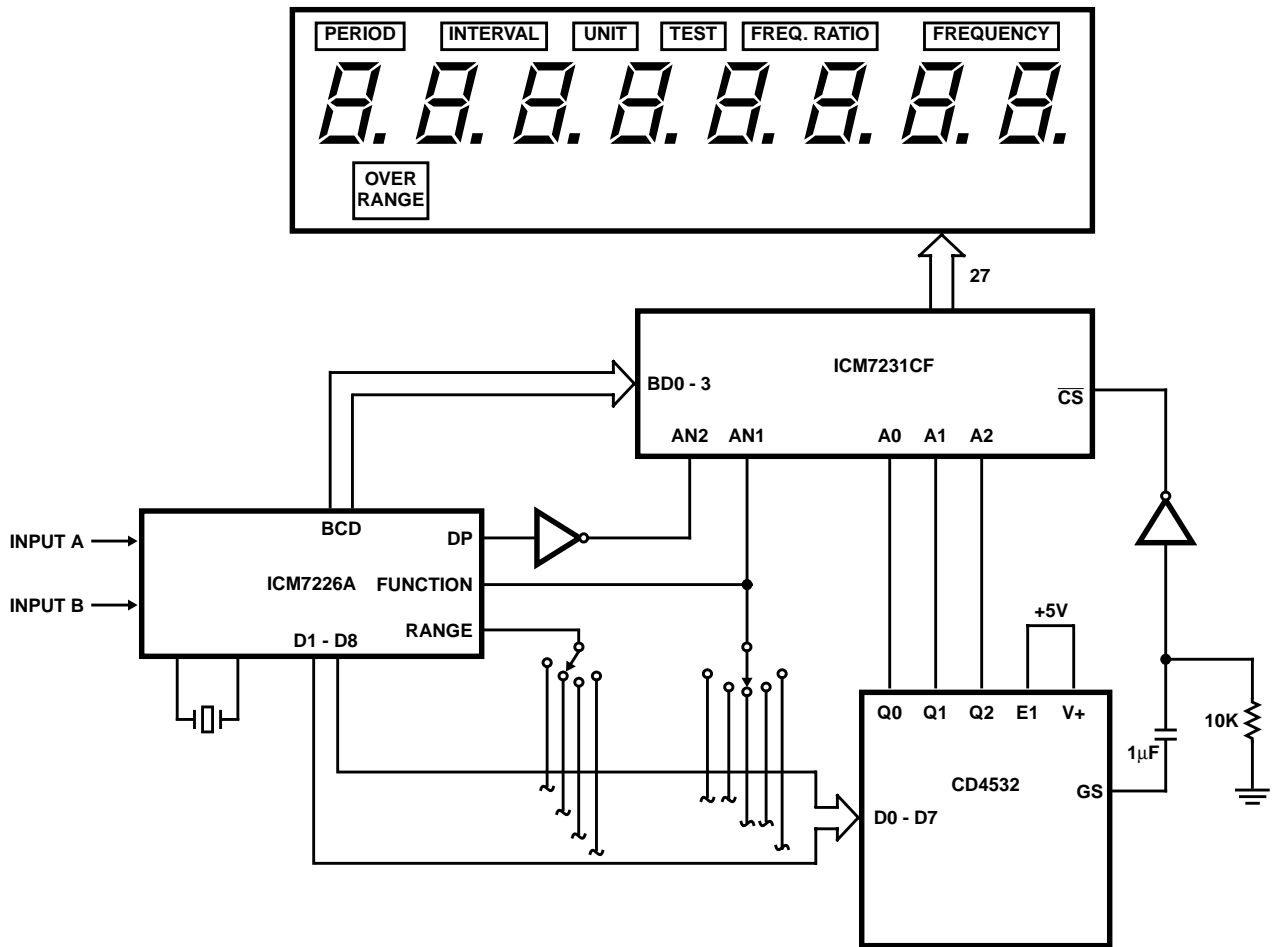
Compatible Displays

Compatible displays are manufactured by: G.E. Displays Inc., Beechwood, Ohio (216) 831-8100 (#356E3R99HJ)

Epson America Inc., Torrance CA (Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA (Custom Displays)

Crystaloid, Hudson, OH

Typical Applications

NOTE: The annunciators show function and the decimal points indicate the range of the current operation. the system can be efficiently battery operated.

FIGURE 15. 10MHz FREQUENCY/PERIOD POINTER WITH LCD DISPLAY
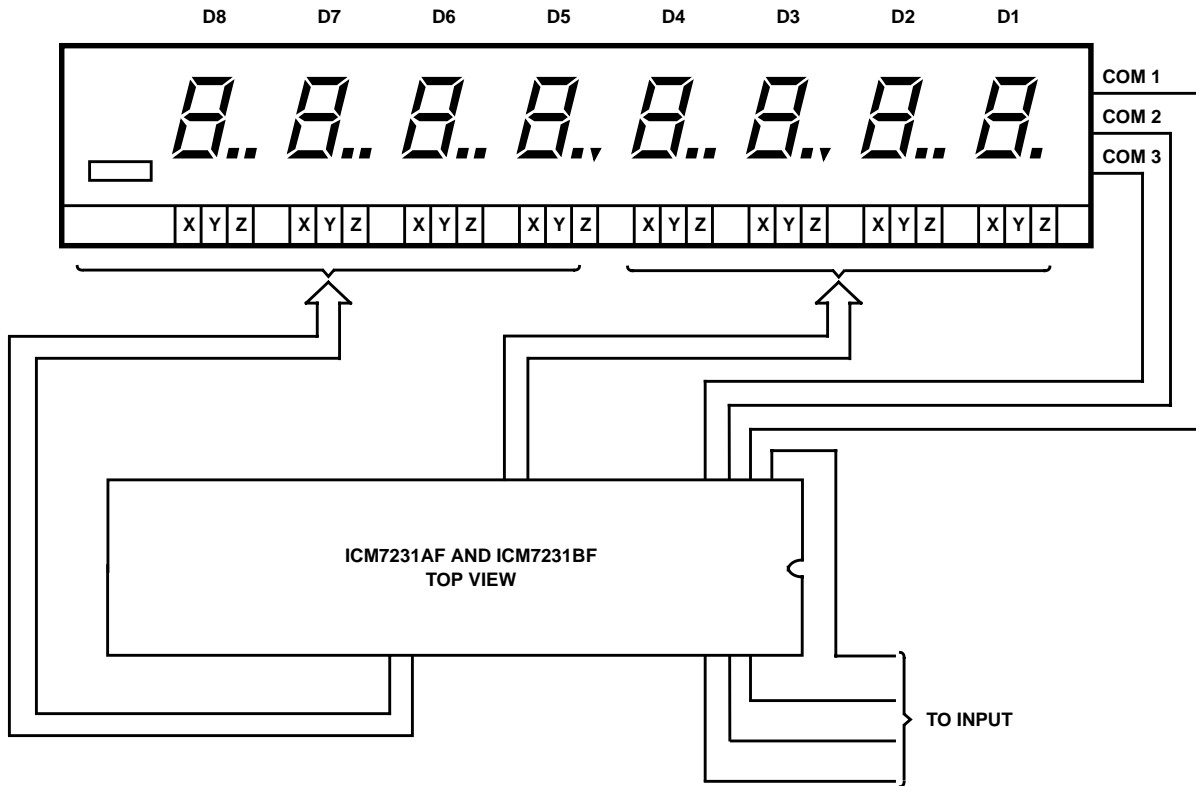
Typical Applications (Continued)

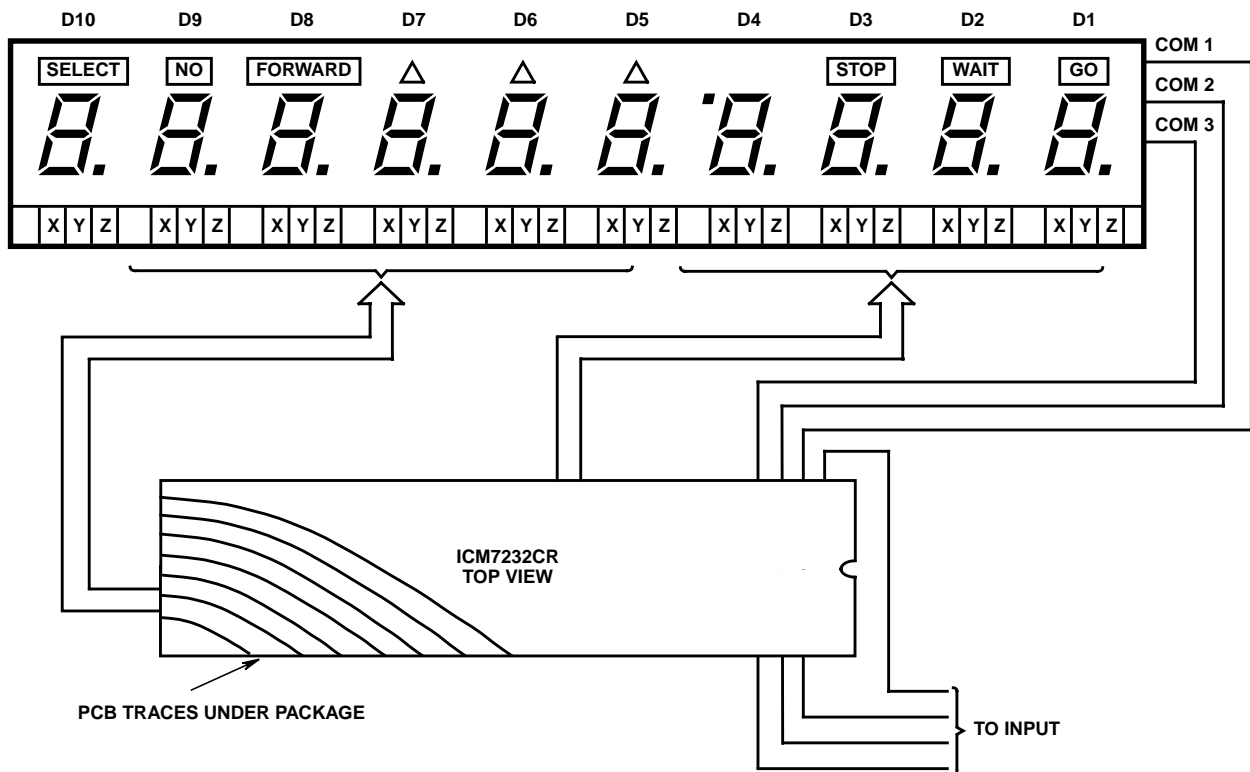**FIGURE 16. "FORWARD" PIN ORIENTATION AND DISPLAY CONNECTIONS**

FIGURE 17. "REVERSE" PIN ORIENTATION AND DISPLAY CONNECTIONS

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