Integrated Circuit Systems, Inc.

ICS9112-27

Preliminary Product Preview

Low Skew PCI / PCI-X Buffer

General Description

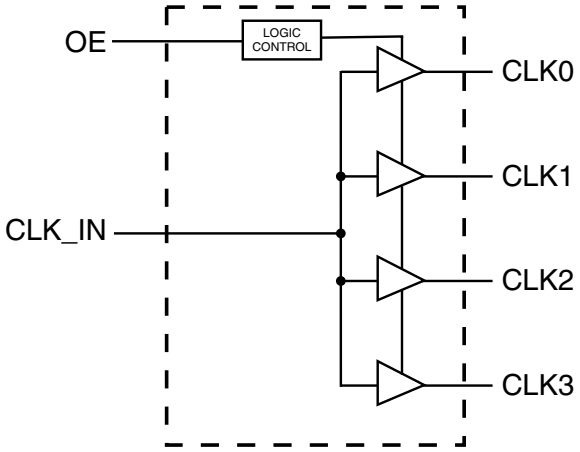
The **ICS9112-27** is a high performance, low skew, low jitter PCI / PCI-X clock driver. It is designed to distribute high speed signals in PCI / PCI-X applications operating at speeds from 0 to 140 MHz.

The **ICS9112-27** is characterized for operation from -40°C to 85°C for automotive and industrial applications.

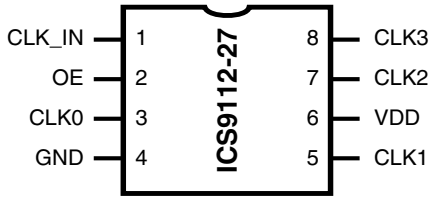
Features

- Frequency range 0 - 140 MHz (3.3V)
- Less than 200 ps Jitter between outputs
- Skew controlled outputs < 100 ps
- Distribute one clock input to one bank of four outputs
- 3.3V ±10% operation
- Available in 8 pin TSSOP, and SOIC packages.

Block Diagram



Pin Configuration



8 pin TSSOP & SOIC

Functionality Table

INPUTS		OUTPUTS
CLK_IN	OE	CLK(3:0)
0	0	0
0	1	0
1	0	0
1	1	1

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CLK_IN	IN	Input reference frequency.
2	OE	IN	Output enable (has internal pull_up.) when OE is low, it tristates the clock outputs
3	CLK0	OUT	Buffered clock output
4	GND	PWR	Ground
5	CLK1	OUT	Buffered clock output
6	VDD	PWR	Power supply for 3.3V
7	CLK2	OUT	Buffered clock output
8	CLK3	OUT	Buffered clock output

Absolute Maximum Ratings

Supply voltage range V_{DD} ..... -0.5V to 4.3 V
Input voltage rangeV_I (see notes 1 & 2) ..... -0.5V to V_{DD} + 0.5V
Output voltage range V_O (see notes 1 & 2) ..... -0.5V to V_{DD} + 0.5V
Input clamp current I_{IK} (V_I< 0 or V_I >V_{DD}) ..... ±50 mA
Output clamp current I_{OK} (V_O< 0 or V_O) ..... ±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD}) ..... ±50 mA
Package thermal impedance $Ø_{JA}$ (see note 3): PW package ... 230.5°C/W
Storage temperature rante, T_{stg} ..... -65°C to 150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Notes:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Terminal Functions

Terminal	No	I/O	Description
CLK (3-0)	8, 7, 5, 3	O	Buffered output clocks
CLKIN	1	I	Input reference frequency
GND	4	PWR	Ground
OE	2	I	Outputs enable control
V_{DD} 3.3V	6	PWR	3.3V supply

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{DD}	3	3.3	3.6	V
High-level input voltage, V_{IH}	$0.7_X V_{DD}$			V
Low-level input voltage, V_{IL}			$0.3_X V_{DD}$	V
Input voltage, V_I	0		V_{DD}	V
High-level output current, I_{OH}			-24	mA
Low-level output current, I_{OL}			24	mA
Operating free-air temperature, T_A	-40		85	°C

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

	Min	Nom	Max	Unit
Clock frequency f_{CLK}	0		140	MHz

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions	Min	Nom	Max	Unit
Input voltage V_{IK}	V_{DD} = 3.3V, I_I = 18 mA			-1.2	V
High-level output voltage V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DD} -0.2			V
	V_{DD} = 3 V I_{OH} = 24 mA	2			V
	V_{DD} = 3 V I_{OH} = 12 mA	2.4			V
Low-level output voltage V_{OL}	V_{DD} = min to max, I_{OL} = -1 mA			0.2	V
	V_{DD} = 3 V I_{OL} = 24 mA			0.8	V
	V_{DD} = 3 V I_{OL}= 12 mA			0.55	V
High-level output current I_{OH}	V_{DD} = 3 V V_O = 1 V	-50			mA
	V_{DD} = 3.3 V V_O = 1.65 V		-55		mA
Low-level output current I_{OL}	V_{DD} = 3 V V_O = 2 V	60			mA
	V_{DD} = 3.3 V V_O = 1.65 V		70		mA
Input current I_I	V_I = V_O or V_{DD}			±5	µA
Dynamic Current, see figure 5 I_{DD}	f = 67 MHz			37	mA
Input capacitance C_i	V_{DD} = 3.3V V_I = 0 V or V_{DD}		3		pF
Output capacitance C_o	V_{DD} = 3.3V V_I = 0 V or V_{DD}		3.2		pF

Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL = 25 pF, VDD = 3.3 V (see note 6 and figures 1 and 2)

Parameter	Test Conditions	Min	Nom	Max	Unit
High-to-low propagation delay t_{PLH}	See figures 1 and 2	1.8	2.5	3	ns
Low-to-high propagation delay t_{PHL}		1.8	2.4	3	ns
Output skew (see note 4) $T_{SK\ (O)}$				100	ps
Pulse skew $t_{SK\ (P)}$	V_{IH} = V_{DD}, V_{IL} = 0 V			150	ps
Process skew $T_{SK\ (PR)}$					ns
CLK high time, see figure 4 T_{high}	66 MHz	6			ns
	140 MHz	3			
CLK low time, see figure 4 T_{low}	66 MHz	6			ns
	140 MHz	3			
Output rise slew rate‡ T_r	0.2V_{DD} to 0.6V_{DD}	1.5	2.7	4	V/ns
Output fall slew rate‡ T_f	0.6V_{DD} to 0.2V_{DD}	1.5	2.7	4	V/ns

Parameter Measurement Information

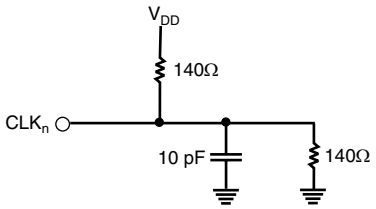


Figure 1. Test Load Circuit

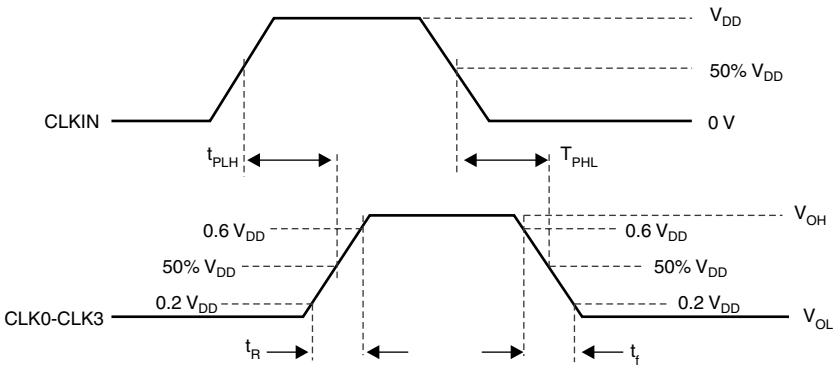


Figure 2. Voltage Thresholds for Propagation Delay (t_{pd}) Measurements

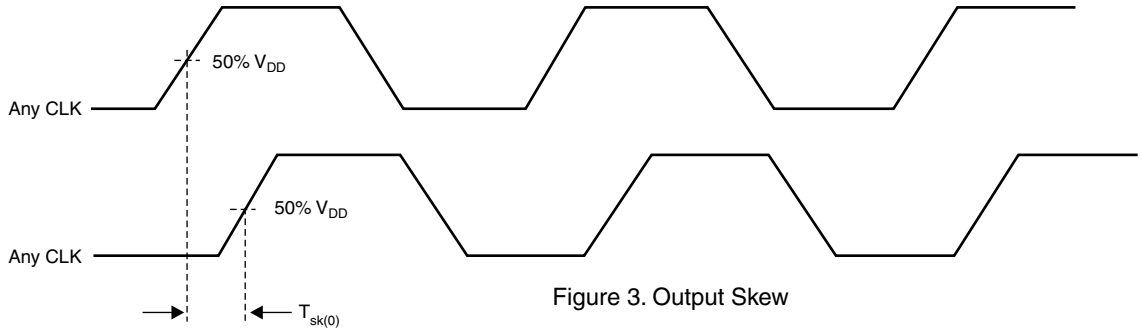


Figure 3. Output Skew

Paramameter	Value	Unit
$V_{IH(Min)}$	0.5 V_{DD}	V
$V_{IL(Max)}$	0.35 V_{DD}	V
V_{test}	0.4 V_{DD}	V

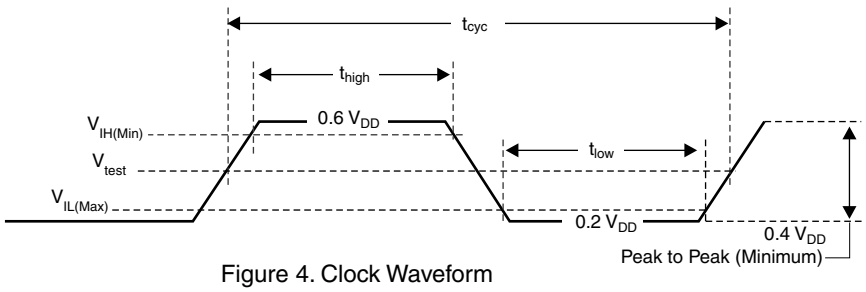


Figure 4. Clock Waveform

Note: All parameters in Figure 4 are according to PCI-X 1.0 specifications.

Parameter Measurement Information

Supply Current
vs
Frequency

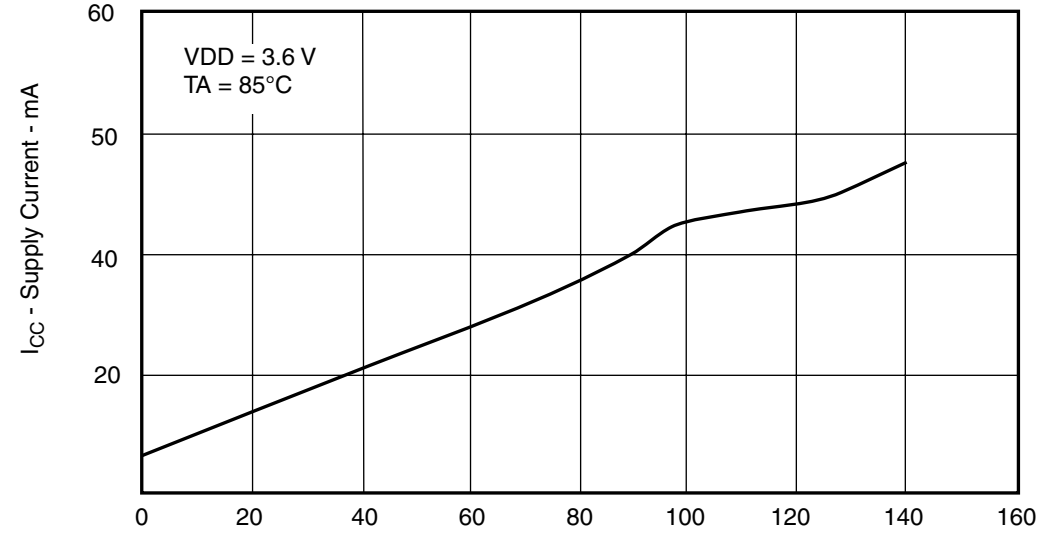


Figure 5

High Level Output Voltage
vs
High-Level Output Current

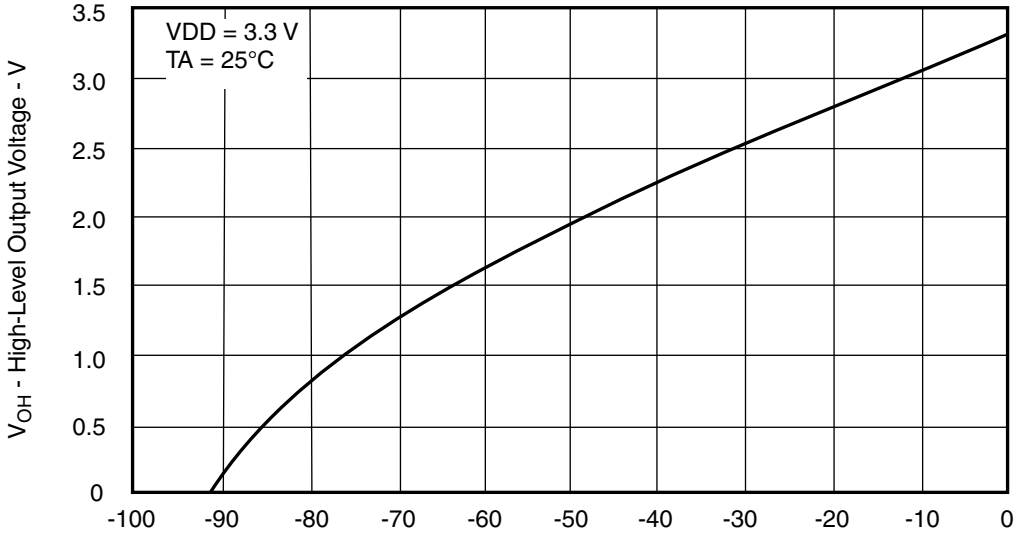


Figure 6

Parameter Measurement Information

Low Level Output Voltage
vs
Low-Level Output Current

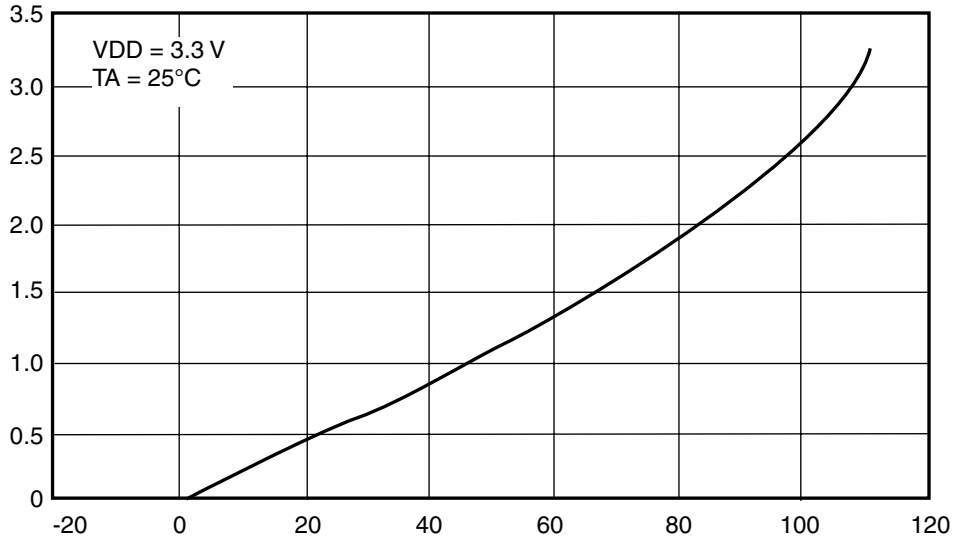
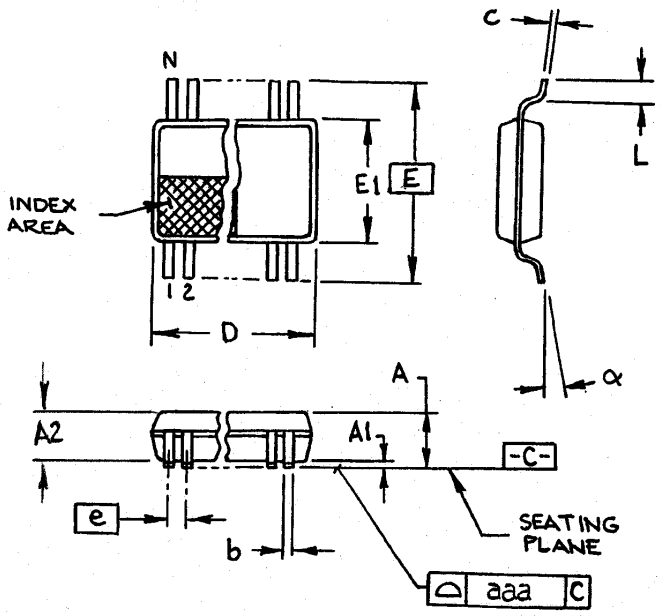


Figure 7



4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	2.90	3.10	.114	.122

MO-153 JEDEC 7/6/00 Rev B
Doc.# 10-0038

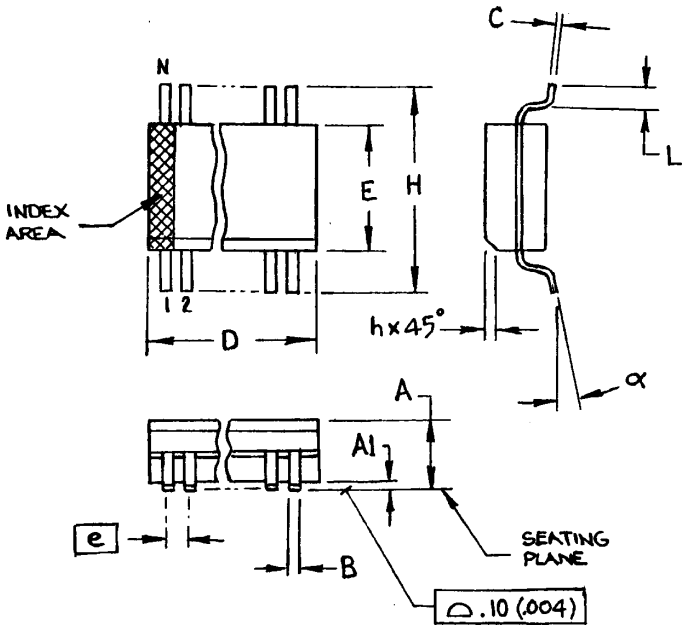
Ordering Information

ICS9112yG-27-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



150 mil (Narrow Body) SOIC

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

10-0030 Rev A - MS-012

Ordering Information

ICS9112yM-27-T

Example:

ICS XXXX y M - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device