Integrated Circuit Systems, Inc.

ICS9148-13

Frequency Generator & Integrated Buffers for PENTIUM™

General Description

The **ICS9148-13** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel Pentium and PentiumPro. An output enable is provided for testability.

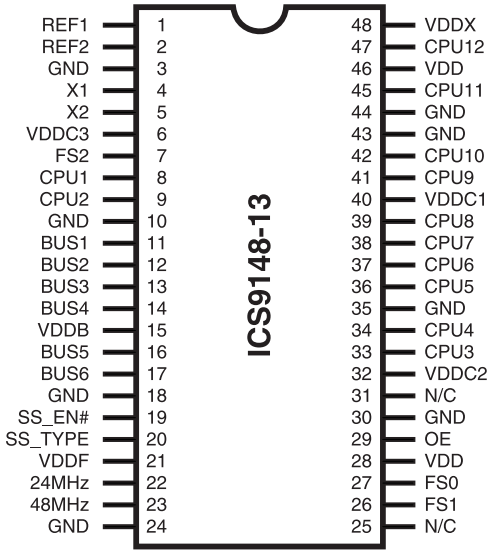
Spread Spectrum is available to modulate the CPU and BUS PLL (leaving the REF, 24, 48 MHz operating normally). The SS_EN# pin enables the spreading when low. The SS_TYPE pin choses ±0.5% (nominally) center spread or +0, -2% (nominally) downspread modulation.

High drive BUS outputs typically provide greater than 1V/ns slew rate into 30 pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50 ± 5% duty cycle. The REF clock outputs typically provide better than 0.8/ns slew rates.

Features

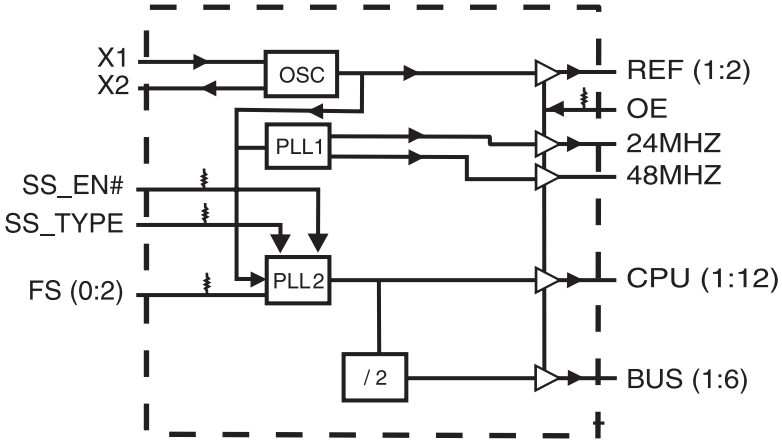
- Generates twelve processor, six bus, two 14.31818 MHz, 24MHz and one 48 MHz clock for USB support.
- Synchronous clocks skew matched to 250 ps window on CPUs and 500 ps window on BUSs
- CPU to BUS skew, 3.0 to 5.0ns (CPU Early)
- 3.0V - 3.7V supply range
- 48-pin SSOP package

Pin Configuration



48-Pin SSOP

Block Diagram



Output Enable

OE	REF	24 (MHz)	48 (MHz)	CPU	BUS	VCO	OSC
1	Runs	Runs	Runs	Runs	Runs	Runs	Runs
0	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Runs	Runs

30K pullup resistor to VDD on OE, FS(0:2), SS_EN#, SS_TYPE

Functionality

FS2	FS1	FS0	CPU (1:12) in MHz	BUS (1:6) in MHz
0	0	0	75	37.5
0	0	1	100	33.3
0	1	0	75	30.0
0	1	1	83.3	41.65
1	0	0	50	25
1	0	1	60	30
1	1	0	66.67	33.33
1	1	1	55	27.5

Pentium is a trademark of Intel Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2	REF1, REF2	OUT	14.318 MHz reference clock outputs.
3, 10, 18, 24, 30, 35, 43, 44	GND	PWR	Device Ground
4	X1	IN	Crystal or external clock input.
5	X2	OUT	Crystal output. (for external reference clock leave unconnected)
6	VDD	PWR	3.3V volt I/O power supply.
7, 26, 27	FS (0:2)	IN	Frequency select inputs. See function list table. Has pull up resistors
11,12,13,14,16, 17	BUS (1:6)	OUT	BUS clock outputs.
19	SS_EN#	IN	Spread Spectrum Enable. Low=enable.
20	SS_TYPE	IN	High=Spread Spectrum down spread. Low=Spread Spectrum center spread.
15, 21, 28, 31, 32, 40, 46, 48	VDD	PWR	Core power supply. 3.3V
22	24MHz	OUT	24MHz clock output
23	48MHz	OUT	48MHz clock output.
25	N/C		No connect
29	OE	IN	Output Enable when this signal is Low all Bus Clocks, Fixed Clocks, CPU Clocks outputs placed in tristate mode (internally pulled up)
33, 34, 36, 37, 38, 39, 41, 42, 45, 47, 8, 9	CPU (1:12)	OUT	CPU clocks outputs see functionality table for frequency specifications

Spread Spectrum Functionality

Input Pin 19 SS_EN#	Input Pin 20 SS_TYPE	CPU, SDRAM and PCICLOCKS	REF, IOAPIC	24MHz	48MHz
0	0	Frequency modulated in spread spectrum mode +0.5%, -0.5% (nominally)	14.318MHz	24MHz	48MHz
	1	Frequency modulated in spread spectrum mode +0%, -2.0% (nominally)	14.318MHz	24MHz	48MHz
1	X	Normal, Steady frequency mode	14.318MHz	24MHz	48MHz

VDD Pins: 48, REFs, XTAL OSC
VDD Pins: 6, CPU 1- 2
VDD Pins: 15, BUS 1-6
VDD Pins: 24, 48, Fix PLL
VDD Pins: 28, CPU PLL CORE
VDD Pins: 32, CPU 3-6
VDD Pins: 40, CPU 7-10
VDD Pins: 46, CPU 11-12

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH1}	V_{IN} = $V_{DD;}$ SS_Type only		68.0	200	µA
	I_{IH2}	V_{IN} = $V_{DD;}$ All outputs Except SS_Type	-5	0.2	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V;with pull-down resistors SS_Type only	-5	0.2	5	µA
	I_{IL2}	V_{IN} = 0 V;with pull-up resistors except SS_Type	-200	-100		µA
Supply Current	I_{DD}	C_L = 0 pF; Select @ 66M		67	180	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		1.5	3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-BUS}$	V_T = 1.5 V;	3.0	4.0	5.0	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4	2.5		V
Output Low Voltage	V_{OL2A}	I_{OL} = 27 mA		0.35	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-52	-48	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	49.3	59		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.5	2.5	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		1.3	2	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk2A}[1]	V_T = 1.5 V		120	250	ps
Jitter	t_{j1s2A}[1]	V_T = 1.5 V		60	150	ps
	t_{jabs2A}[1]	V_T = 1.5 V; For 66.66 MHz and lower	-250	100	+250	ps
	t_{jabs2A}[1]	V_T = 1.5 V; For 75 MHz and Higher	-300	150	-300	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF(1:2)

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -8 mA	2.6	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		2.0	2.5	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		1.8	2.3	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	40	53	60	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V		200	300	ps
	t_{jabs5}[1]	V_T = 1.5 V	-700	500	700	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - BUS

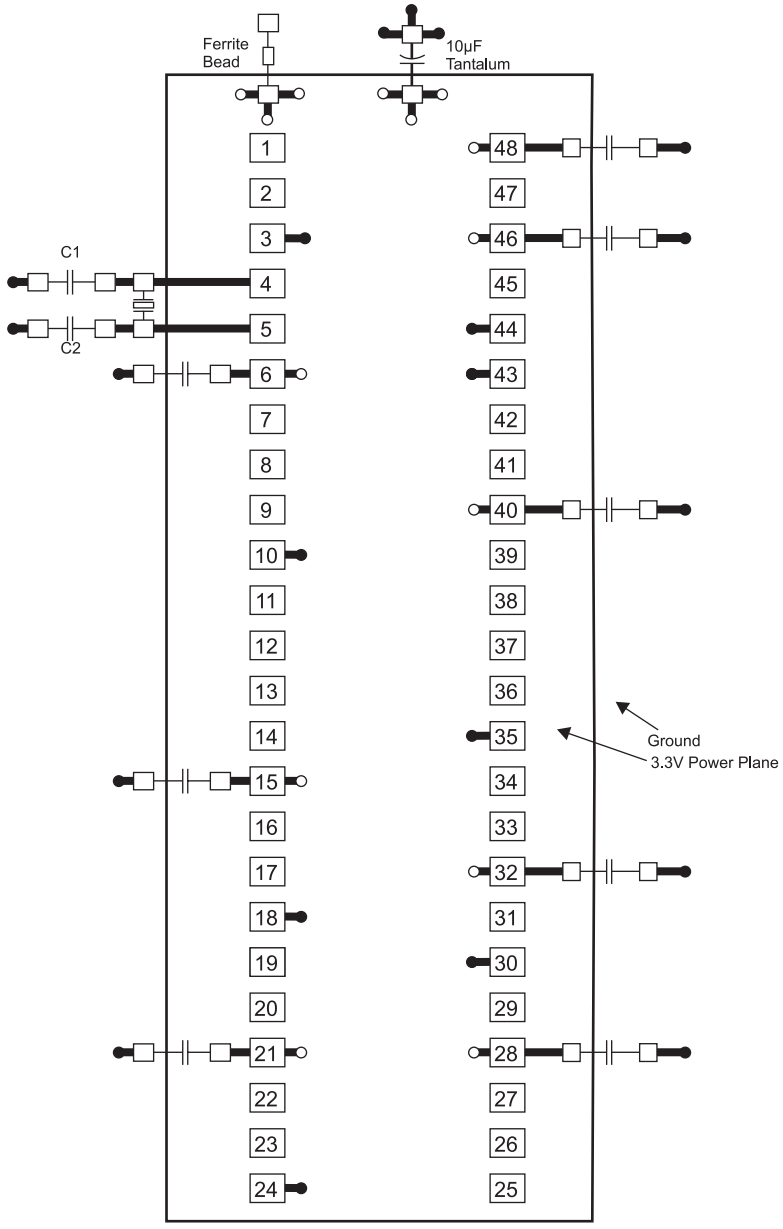
T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	46		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		1.7	2	ns
Fall Time	t_{fl}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		1.5	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		200	500	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V		30	150	ps
	t_{jabs1}[1]	V_T = 1.5 V	-250	110	250	ps

[1]Guarenteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

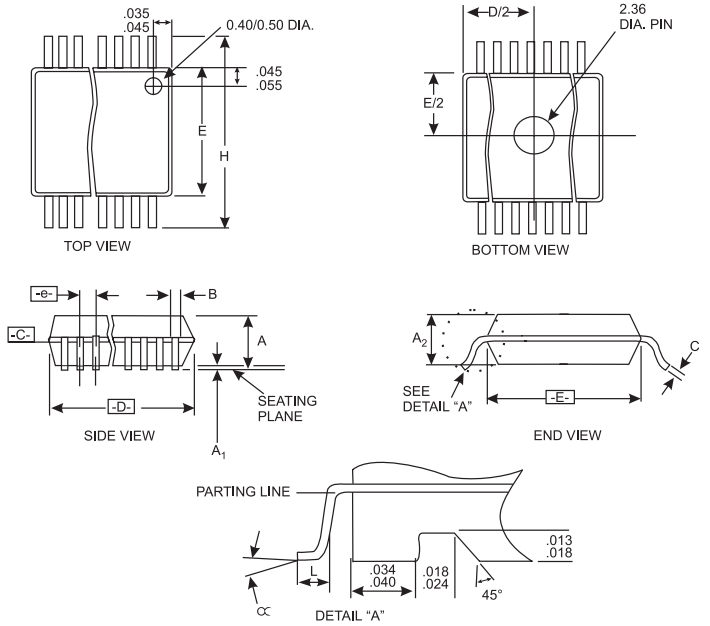


Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3. Optional crystal load capacitors are recommended

Capacitor Values:

C1, C2: Crystal load values determined by user.
All unmarked capacitors are 0.01µF ceramic



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9148F-13

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device