Integrated
Circuit
Systems, Inc.

ICS9159-07

Frequency Generator for NexGen™ Nx586 Systems

General Description

The **ICS9159-07** is a low-cost frequency generator designed specifically for NexGen Nx586 systems. The integrated buffer minimizes skew and provides the CPU clocks required by the NexGen Nx586 microprocessor. A 14.318 MHz XTAL oscil-lator provides the reference clock to generate standard Nx586 frequencies. The CPU clock makes gradual frequency transi-tions without violating the PLL timing of internal microproc-essor clock multipliers.

Either synchronous (2XCPU/3) or asynchronous (32 MHz) PCI bus operation can be selected. Green PC systems are supported through doze mode.

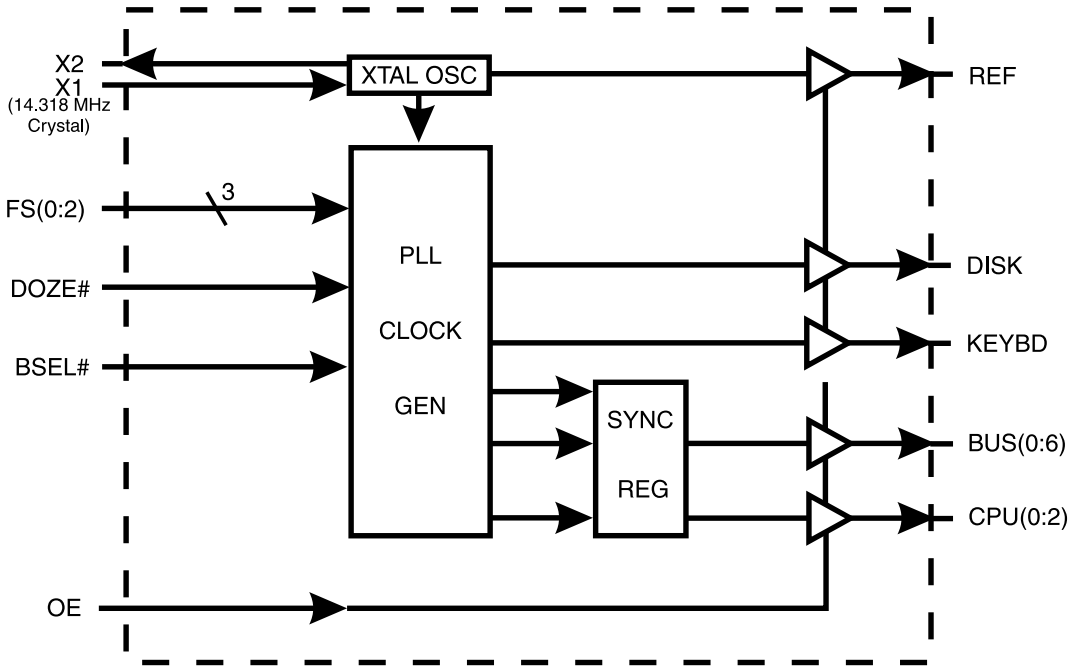
Features

- Three CPU clocks operate up to 65 MHz at 3.3V, plus smooth transitions
- Selection of nine frequencies, tristate
- Seven BUS clocks support sync or async bus operation
- Integrated buffer outputs drive up to 10pF loads
- 3.13 to 5.25V (3.3±5%, 5.0±5%) supply range
- 28-pin SOIC package
- Clock duty cycles 45/55

Applications

- Ideal for NexGen Nx586 PCI-based motherboard designs

Block Diagram



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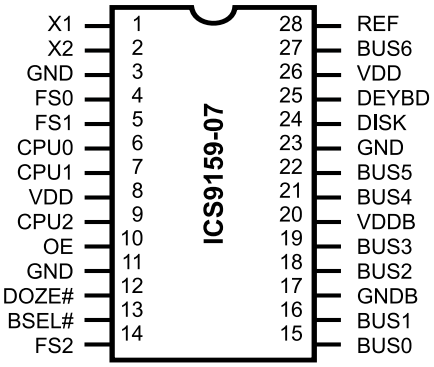
Pin Configuration



28-Pin SOIC

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz XTAL. Normally, 14.318 MHz.
2	X2	OUT	XTAL output which includes XTAL load capacitance.
6,7, 9	CPU(0:2)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table below.
3, 11, 23	GND	PWR	Device Ground.
4, 5, 14	FS(0:2)	IN	Frequency multiplier select pins. See table below. These inputs have internal pull-up devices.*
8, 26	VDD	PWR	Positive power supply.
10	OE	IN	Output Enable. All outputs tristate when low.**
12	DOZE#	IN	Reduces CPU clock frequency to 10 MHz when at a logic low level.*
13	BSEL#	IN	Synchronous and non-synchronous bus clock selector.* ASYNC=0, SYNC=1
15, 16, 18 19, 21, 22, 27	BCLK(0:6)	OUT	Bus clock outputs are fixed at 2 ¤3 the PCLK frequency.
20	VDDB	PWR	Power for BUS output buffers.
17	GNDB	PWR	This ground return path is brought on separately to permit separating the noise impulses from high output buffers from affecting sensitive internal circuitry.***
24	DISK	OUT	Fixed 24 MHz clock (with 14.318 MHz input).
25	KEYBD	OUT	Fixed 12 MHz clock (with 14.318 MHz input).
28	REF	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

* Internally pulled-up.
** External pull-up resistor of 5 to 20 kW recommended due to dynamic coupling of adjacent CPU pins.
*** Ground for bus clock buffers.

Functionality

14.318 MHz Input, all frequencies in MHz.

OE	FS2	FS1	FS0	DZE	CPU (0:2)	BUS 0:6	
						BSEL=1	BSEL=0
1	0	0	0	1	65	43.3	32
1	0	0	1	1	60	40	32
1	0	1	0	1	55.5	37	32
1	0	1	1	1	51	34	32
1	1	0	0	1	46.5	31	32
1	1	0	1	1	42	28	32
1	1	1	0	1	37.5	25	32
1	1	1	1	1	35	23.3	32
1	X	X	X	0	10	6.6	32
0	X	X	X	X	Tristate	Tristate	Tristate

Actual CPU Frequencies

CPU Frequency (MHz)	Actual Frequency (MHz)
65	64.98
60	60.03
55.5	55.50
51	51.00
46.5	46.53
42	42.00
37.5	37.48
35	35.00
10	10.00
Tristate	Tristate

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	25.0	-5.0	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current [1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage [1]	V_{OL}	I_{OL}=15mA; for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage [1]	V_{OH}	I_{OH}=-30mA; for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage [1]	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage [1]	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{CC}	CPU @65.0 MHz; BUS @ 43.3 MHz; all outputs unloaded	-	80.0	130.0	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.1 – 3.7 V, T_A = 0 – 70° C

AC Characteristics							
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]		T_{r1}	20pF load; 0.8 to 2.0V	-	0.9	1.5	ns
Fall Time[1]		T_{f1}	20pF load; 2.0 to 0.8V	-	0.8	1.4	ns
Rise Time[1]		T_{r2}	20pF load; 20% to 80%	-	1.5	2.5	ns
Fall Time[1]		T_{f2}	20pF load; 80% to 20%	-	1.4	2.4	ns
Duty Cycle[1]		D_t	20pF load; VOUT=1.4V	45	50	55	%
CPU(0:2)	Jitter[1] Cycle-to-Cycle	T_{jcc1}	Load=10pF	-150	50	+150	ps
	Slew[1]	SR_1	Load=10pF; 0.8 to 2.0V	1.0	1.6	A	V/ns
BUS(0:6)	Jitter 1Cycle-to-Cycle	T_{jcc2}	Load=10pF	-250	-	250	ps
	Slew[1]	SR_2	Load=30pF; 0.8 to 2.0V	0.6	1.0	A	V/ns
Jitter, One Sigma[1]		T_{jis}	Fixed CLK; Load=20pF; Comp. to the period	-	1	3	%
Jitter, Absolute[1]		T_{jab}	Fixed CLK; Load=20pF; Comp. to the period	-	2	5	%
Input Frequency[1]		F_i	A	12.0	14.318	16.0	MHz
Logic Input Capacitance[1]		C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]		C_{INX}	X1, X2 pins	-	18	-	pF
Frequency Transition Time[1]		T_{a1}	Acquisition from 35 MHz to 65 MHz (first crossing) (and 65 to 35).	-	0.46	1.4	ms
Frequency Transition Time (to DOZE)[1]		T_{a2}	Acquisition from 10 MHz to 65 MHz (first crossing) (and 65 to 10)	-	0.76	2.3	ms
Frequency Settling Time[1]		t_s	From 1 st crossing of acquisition to <1% settling.	-	400	-	ms
Skew[1]	CPU to CPU	T_{SK1}	CL=10pF VO=1.5V	-250	-	+250	ps
	CPU to BUS(0:5)	T_{SK2}		-600	200	1000	
	CPU to BUS(6)	T_{SK3S}		-900	-400	110	
	BUS(0:5) to BUS(0:5)	T_{SK4}		-500	-	+500	
	BUS(0:5) to BUS(6)	T_{SK5}		-1050	-550	250	

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.5V

V_{DD} = 4.5 – 5.5 V, T_A = 0 – 70° C

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-45.0	-15.0	A	mA
Input High Current	I_{IH}	V_{IN}=V_{DD}, other logic inputs	-5.0	-	5.0	mA
Input High Current Output Enable Pin[2]	$I_{IH(OE)}$	V_{IN}=V_{DD}, OE pin	-5.0	A	400.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for PCLKS & BCLKS	-	-152.0	-90.0	mA
Output Low Current [1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	30.0	50.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-110.0	-65.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=20mA; for PCLKS & BCLKS	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-70mA; for PCLKS & BCLKS	2.4	4.0	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for fixed CLKs	-	0.2	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-50mA; for fixed CLKs	2.4	4.7	-	V
Supply Current	I_{CC}	CPU @65.0 MHz; BUS @ 43.3 MHz; all outputs unloaded	-	130.0	220.0	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

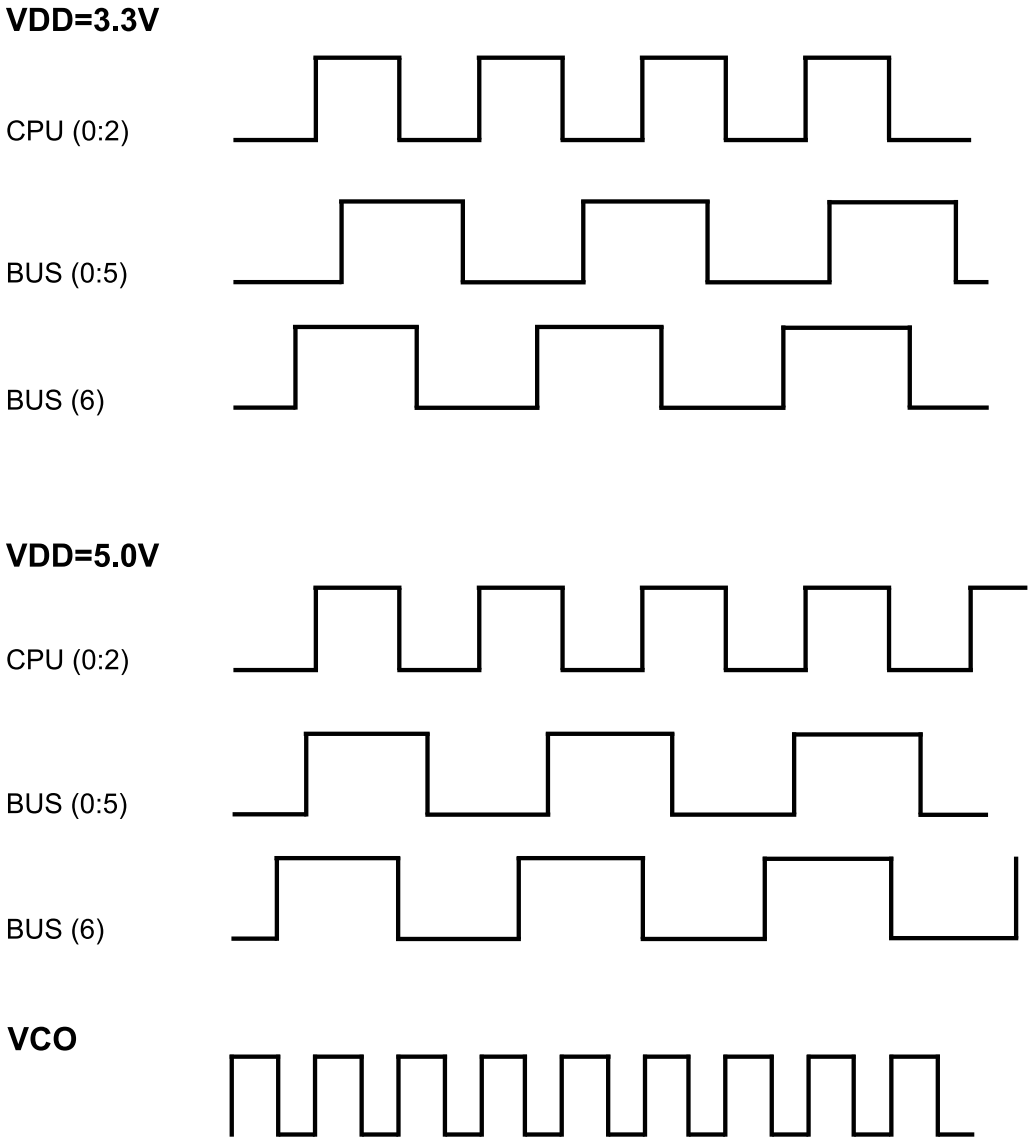
Electrical Characteristics at 5.5V

V_{DD} = 4.5 – 5.5 V, T_A = 0 – 70° C

AC Characteristics							
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]		T_{r1}	20pF load; 0.8 to 2.0V	-	0.55	0.95	ns
Fall Time[1]		T_{f1}	20pF load; 2.0 to 0.8V	-	0.52	0.90	ns
Rise Time[1]		T_{r2}	20pF load; 20% to 80%	-	1.2	2.1	ns
Fall Time[1]		T_{f2}	20pF load; 80% to 20%	-	1.1	2.0	ns
Duty Cycle[1]		D_t	20pF load; VOUT=1.4V	45	50	55	%
CPU(0:2)	Jitter[1] Cycle-to-Cycle	T_{jcc1}	Load=10pF	-150	50	+150	ps
	Slew[1]	SR_1	Load=10pF; 0.8 to 2.0V	1.6	2.6	-	V/ns
BUS(0:6)	Jitter[1]Cycle-to-Cycle	T_{jcc2}	Load=10pF	-250	-	250	ps
	Slew[1]	SR_2	Load=30pF; 0.8 to 2.0V	1.0	1.6	-	V/ns
Jitter, One Sigma[1]		T_{jis}	Fixed CLK; Load=20pF; Comp. to the period	-	1	3	%
Jitter, Absolute[1]		T_{jab}	Fixed CLK; Load=20pF; Comp. to the period	-	2	5	%
Input Frequency[1]		F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]		C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]		C_{INX}	X1, X2 pins	-	18	-	pF
Frequency Transition Time[1]		T_{a1}	Acquisition from 35 MHz to 65 MHz (first crossing) (and 65 to 35).	-	0.50	1.5	ms
Frequency Transition Time (to DOZE)[1]		T_{a2}	Acquisition from 10 MHz to 65 MHz (first crossing) (and 65 to 10)	-	0.78	2.4	ms
Frequency Settling Time[1]		t_s	From 1 st crossing of acquisition to <1% settling.	-	400	-	ms
Skew[1]	CPU to CPU	T_{SK1}	CL=10pF VO=1.5V	-250	-	+250	ps
	CPU to BUS(0:5)	T_{SK2}		-1600	-800	0	
	CPU to BUS(6)	T_{SK3S}		-1750	-1250	-750	
	BUS(0:5) to BUS(0:5)	T_{SK4}		-500	-	+500	
	BUS(0:5) to BUS(6)	T_{SK5}		-900	-400	-100	

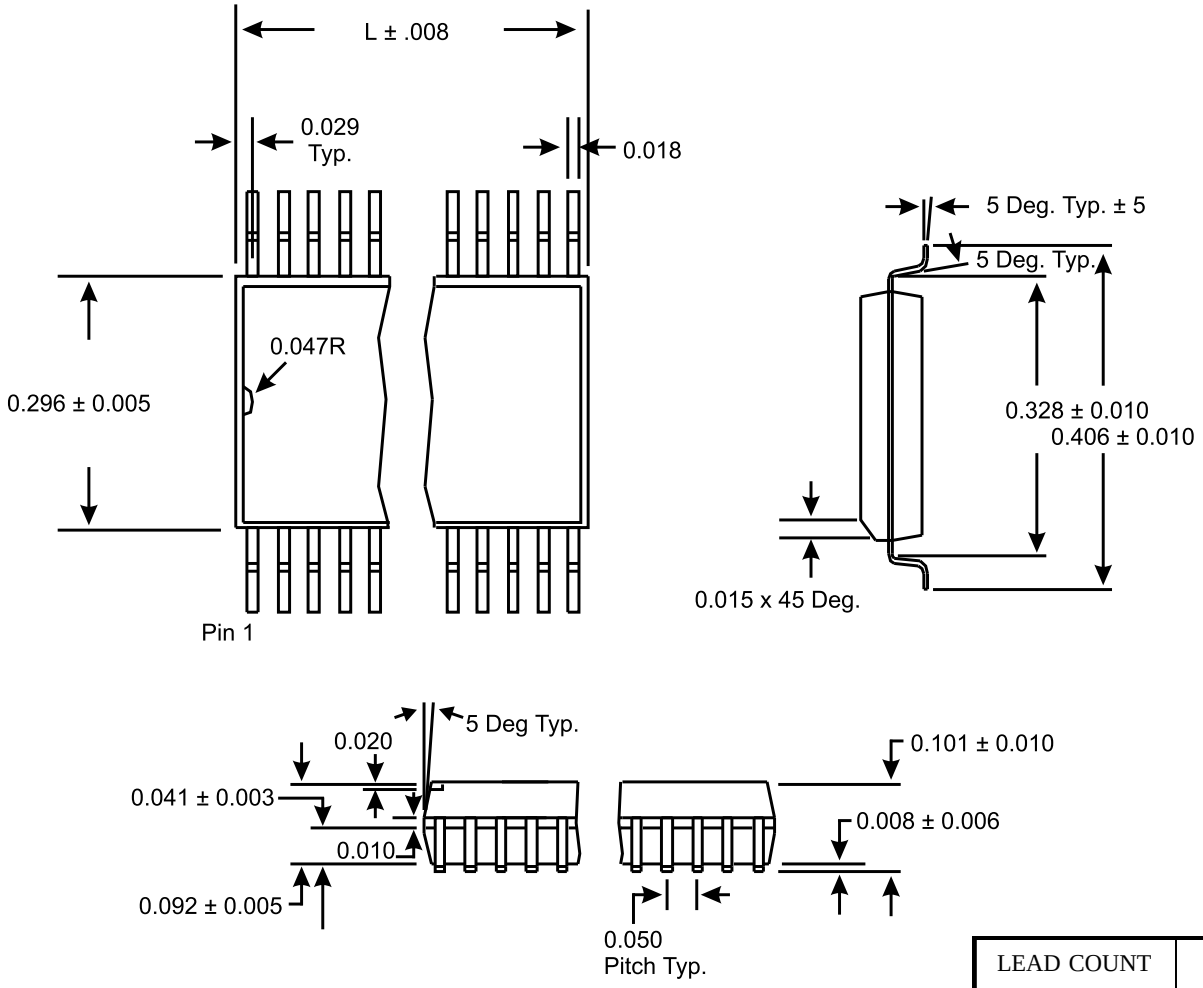
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Typical Timing Diagram of Outputs Showing Skew Relationship



Clock Singles

Note that the skew is rising edge to rising edge. The CPU is runniing at VCO/2 and the BUS clock is runing at VCO/3 resulting in the output rising edges being coincident every 3rd pulse.



LEAD COUNT	28L
DIMENSIONL	0.704

SOIC Package

Ordering Information

ICS9159M-07

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, SOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device