Integrated Circuit Systems, Inc.

ICS9248-103

Frequency Generator & Integrated Buffers for PENTIUM/Pro™

General Description

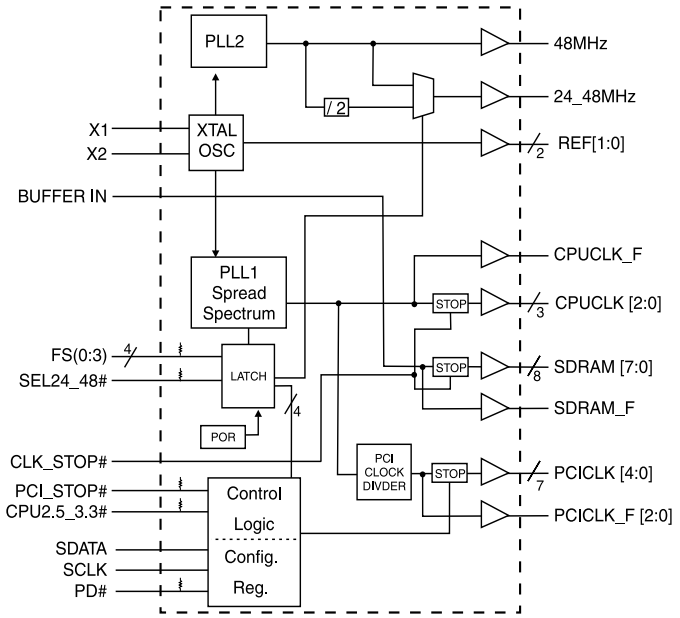
The **ICS9248-103** is the single chip clock solution for Notebook designs using the 440BX or the VIA Apollo Pro 133 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-103** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

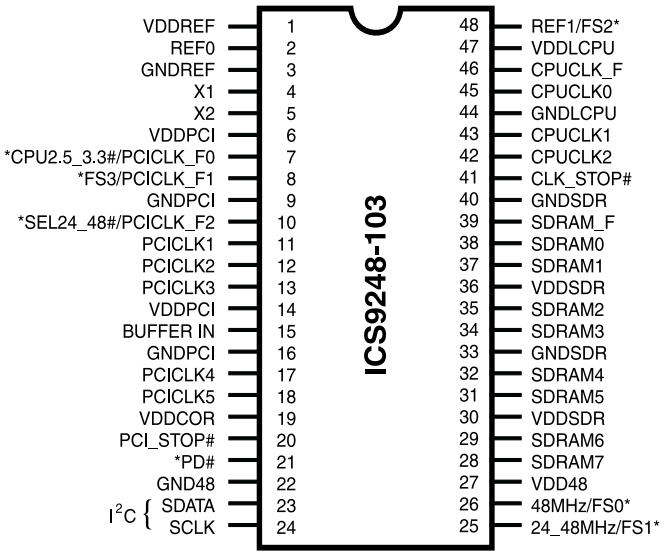
Features

- Up to 137MHz frequency support
- Spread Spectrum for EMI control
- Serial I^2C interface for Power Management, Frequency Select, Spread Spectrum
- Provides the following system clocks
  - 4-CPUs @ 2.5/3.3V, up to 137MHz (including CPUCLK_F)
  - 9-SDRAMs @3.3V, up to 137MHz (including SDRAM_F)
  - 8-PCI @3.3V, CPU/2 or CPU/3 (including 3 free running PCICLK_Fs)
  - 1-24/48MHz @3.3V
  - 1-48MHz @3.3V fixed
  - 2-REF @3.3V, 14.318MHz.
- Efficient Power management scheme through PCI and STOP CLOCKS
- Spread Spectrum ± .25%, & 0 to -0.5% down spread

Block Diagram



Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of 120K to VDD

Power Groups

VDDLCPU, GNDLCPU = CPUCLK [2:0], CPUCLK_F
VDDSDR, GNDSDR = SDRAMCLKS [7:0], SDRAM_F
VDDPCI, GNDPCI = PCICLKS [6:0], PCICLK_F
VDD48, GND48 = 48MHz, 24MHz
VDDREF, GNDREF = REF, X1, X2
VDDCOR = PLL CORE

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I^2C is a trademark of Philips Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.This REF output is the STRONGER buffer for ISA BUS loads
20	PCI_STOP#	IN	Halts PCICLK [4:0]clocks at logic 0 level, when input low (In mobile mode, MODE=0)
3, 9, 16, 33, 40, 44	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz.
6,14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK [6:0], nominal 3.3V
7	CPU2.5_3.3#[1,2]	IN	Indicates whether VDDLCPU is 2.5 or 3.3V. High=2.5V CPU, LOW=3.3V CPU. Latched Input.
	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
8	FS3[1,2]	IN	Frequency select pin. Latched Input.
	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
10	SEL24_48#MHz[1,2]	IN	Selects either 24 or 48MHz when Low = 48MHz
	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
11	PCICLK1	OUT	PCI clock output Synchronous to CPU clocks with 1-4ns skew (CPU early)
18, 17, 13, 12	PCICLK [5:2]	OUT	PCI clock outputs. Synchronous to CPU clocks with 1-4ns skew (CPU early)
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
19	VDDCOR	PWR	Power pin for the PLL core. 3.3V
21	PD#[1]	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 4ms.
22	GND48	PWR	Ground pin for 24 & 48MHz output buffers & fixed PLL core.
28, 29, 31, 32, 34, 35, 37, 38	SDRAM [7:0]	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
30, 36	VDDSDR	PWR	Supply for SDRAM [7:0] and CPU PLL Core, nominal 3.3V.
23	SDATA	IN	Data input for I^2C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
25	24_48MHz	OUT	24MHz or 48MHz output clock selectable by pin 10
	FS1[1, 2]	IN	Frequency select pin. Latched Input.
26	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched Input
27	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
39	SDRAM_F	OUT	Free running SDRAM clock output. Not affected by CPU_STOP#
41	CLK_STOP#	IN	This asynchronous input halts CPUCLK & SDRAM (0:7) at logic "0" level when driven low.
42, 43, 45	CPUCLK [2:0]	OUT	CPU clock outputs, powered by VDDLCPU
46	CPUCLK_F	OUT	Free running CPU clock. Not affected by the CPU_STOP#
47	VDDLCPU	PWR	Supply for CPU clocks 2.5V
48	REF1	OUT	14.318 MHz reference clock.
	FS2[1, 2]	IN	Frequency select pin. Latched Input

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Functionality

V_{DD} = 3.3V±5%, V_{DDL} = 2.5V±5% or 3.3±5%, TA=0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS3	FS2	FS1	FS0	CPU (MHz)	PCI (MHz)
0	0	0	0	124.00	41.33
0	0	0	1	120.00	40.00
0	0	1	0	114.99	38.33
0	0	1	1	109.99	36.66
0	1	0	0	105.00	35.00
0	1	0	1	83.31	41.65
0	1	1	0	137.00	34.25
0	1	1	1	75.00	37.50
1	0	0	0	100.00	33.33
1	0	0	1	95.00	31.67
1	0	1	0	83.31	27.77
1	0	1	1	133.33	33.33
1	1	0	0	90.00	30.00
1	1	0	1	96.22	32.07
1	1	1	0	66.82	33.41
1	1	1	1	91.5	30.5

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description			PWD
Bit 7	0 - ±0.25% Spread Spectrum Modulation, Center Spread 1 - 0 to -0.5% Down Spread			1
Bit [2, 6:4]	Bit [2, 6:4]	CPUCLK (MHz)	PCICLK (MHz)	Note1
	0000	124.00	41.33	
	0001	120.00	40.00	
	0010	114.99	38.33	
	0011	109.99	36.66	
	0100	105.00	35.00	
	0101	83.31	41.65	
	0110	137.00	34.25	
	0111	75.00	37.50	
	1000	100.00	33.33	
	1001	95.00	31.67	
	1010	83.31	27.77	
	1011	133.33	33.33	
	1100	90.00	30.00	
	1101	96.22	32.07	
	1110	66.82	33.41	
	1111	91.5	30.5	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit [2, 6:4]			0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled			1
Bit 0	0 - Running 1- Tristate all outputs			0

Note 1, Default at Power-up will be for latched logic inputs to define frequency. Bit [2, 6:4] are default to 0010.

Note 2, PWD = Power-Up Default

Note 3, When disabling spread spectrum bit7 needs to be set to 0 to maintain nominal frequency.

Byte 1: CPU, Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	46	1	CPUCLK_F (Act/Inact)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	39	1	SDRAM_F (Act/Inact)
Bit 2	42	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	45	1	CPUCLK0 (Act/Inact)

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	7	1	PCICLK_F0 (Act/Inact)
Bit 6	18	1	PCICLK4(Act/Inact)
Bit 5	17	1	PCICLK3 (Act/Inact)
Bit 4	13	1	PCICLK2 (Act/Inact)
Bit 3	12	1	PCICLK1 (Act/Inact)
Bit 2	11	1	PCICLK0 (Act/Inact)
Bit 1	10	1	PCICLK_F1 (Act/Inact)
Bit 0	8	1	PCICLK_F2 (Act/Inact)

Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	28	1	SDRAM7 (Active/Inactive)
Bit 2	29	1	SDRAM6 (Active/Inactive)
Bit 1	31	1	SDRAM5 (Active/Inactive)
Bit 0	32	1	SDRAM4 (Active/Inactive)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 4: Reserved Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(SEL24_48)#
Bit 4	-	1	(Reserved)
Bit 3	-	X	Latched FS1#
Bit 2	-	1	(Reserved)
Bit 1	-	X	Latched FS3#
Bit 0	-	1	(Reserved)

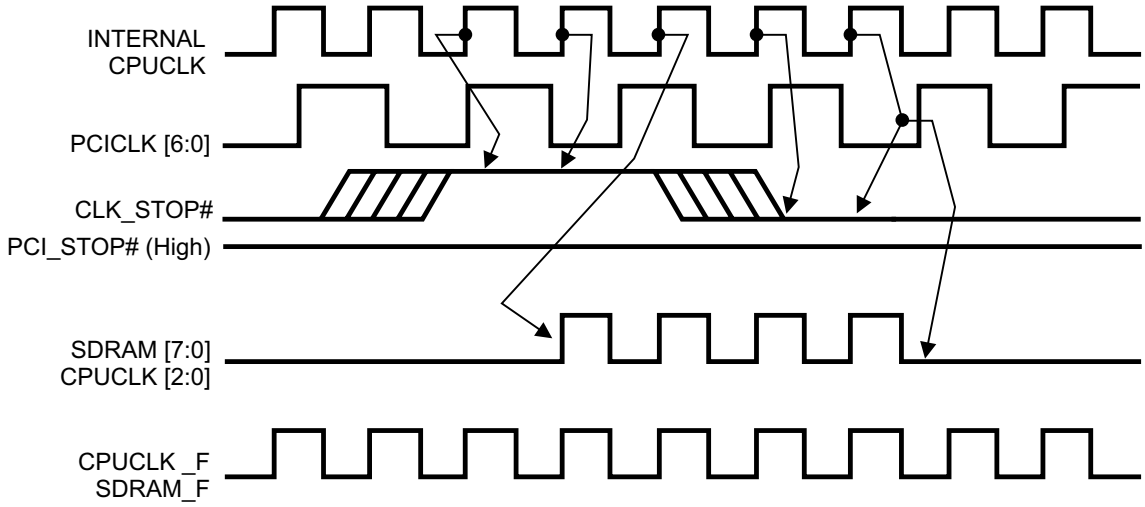
Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	34	1	SDRAM3 (Act/Inact)
Bit 6	35	1	SDRAM2 (Act/Inact)
Bit 5	37	1	SDRAM1 (Act/Inact)
Bit 4	38	1	SDRAM0 (Act/Inact)
Bit 3	26	1	48MHz (Act/Inact)
Bit 2	25	1	24MHz (Act/Inact)
Bit 1	48	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

CLK_STOP# Timing Diagram

CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS9248-103**. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



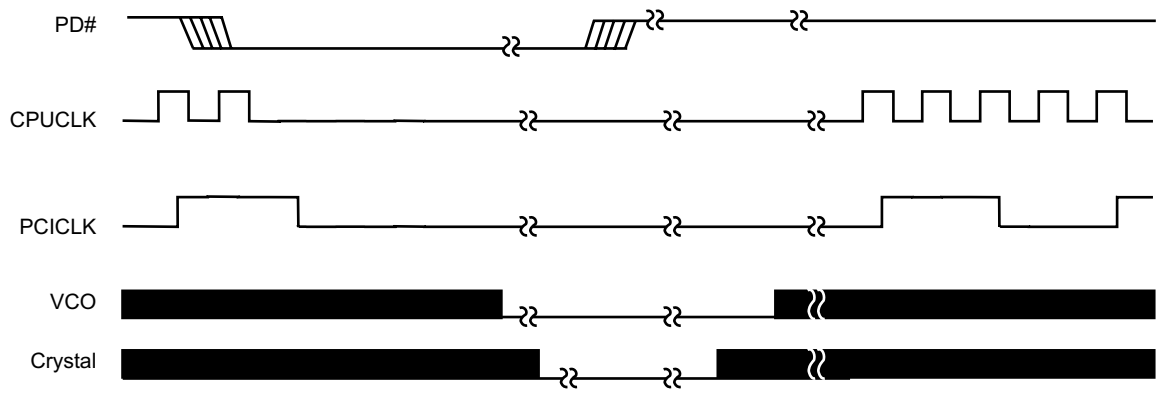
Notes:

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-103.
3. IOAPIC output is Stopped Glitch Free by CPUSTOP# going low.
4. SDRAM-F output is controlled by Buffer in signal, not affected by the ICS9248-103 CLK_STOP# signal. SDRAM [7:0] are controlled as shown.
5. All other clocks continue to run undisturbed.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 4 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CLK_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

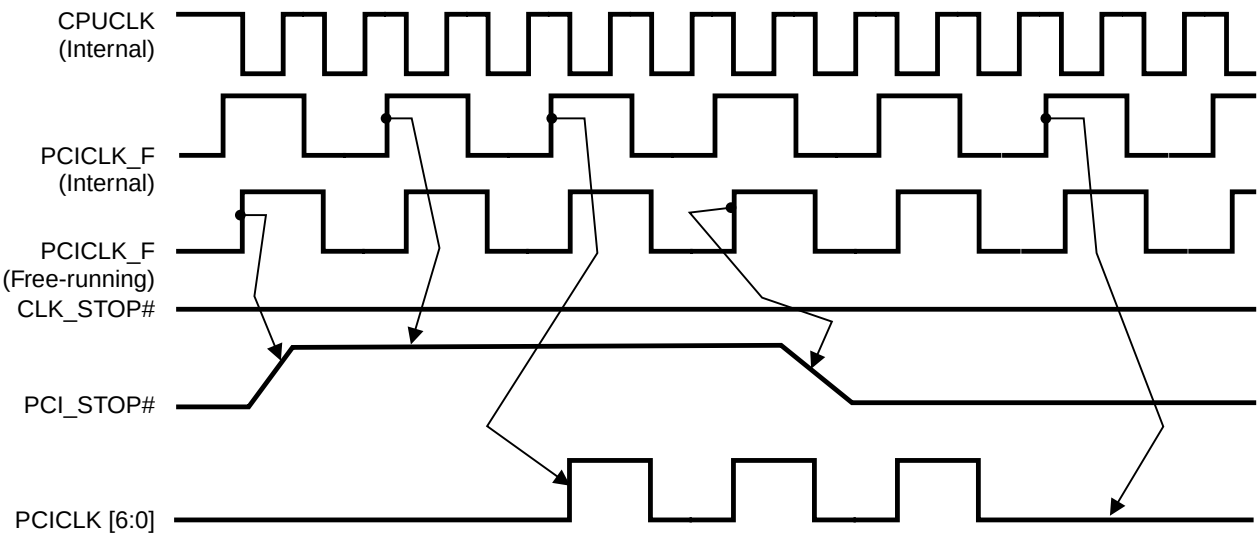


Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-103**. It is used to turn off the PCICLK [4:0] clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-103** internally. The minimum that the PCICLK [4:0] clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK [4:0] clocks. PCICLK [4:0] clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK [4:0] clock on latency cycles are only three rising PCICLK clocks off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CLK_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9248-103** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

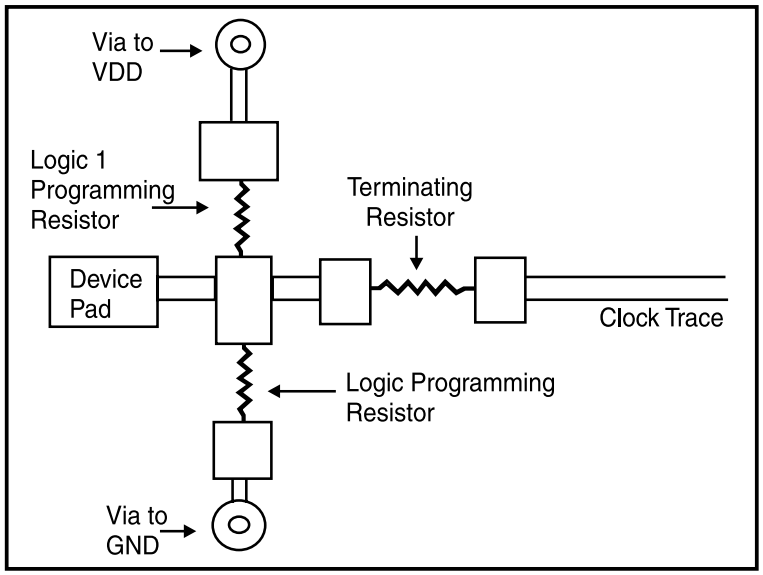


Fig. 1

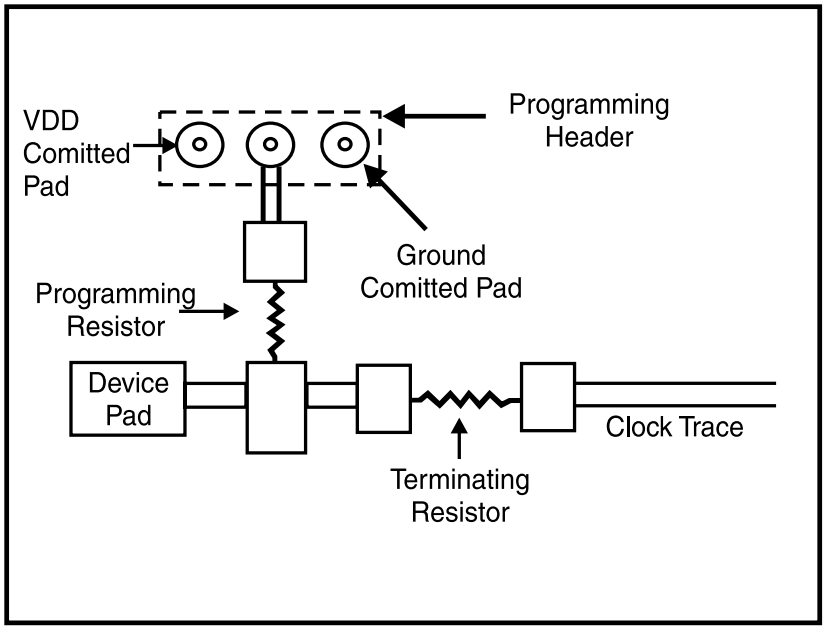

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

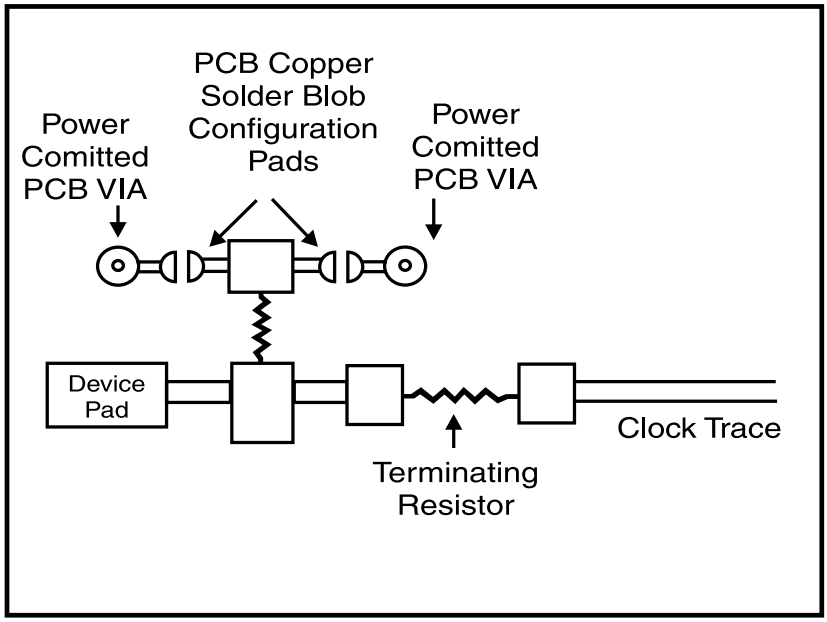

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66MHz		90	150	mA
		C_L = 0 pF; Select @ 100MHz		120	170	
		C_L = 0 pF; Select @ 133MHz		151	180	
Powerdown Current	I_{DDPD}	CL = 0 pF; Input address VDD or GND		250	600	µA
Input Frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			5.5	ms
Skew[1]	$t_{CPU-PCI1}$	V_T = 1.5 V	1	2.8	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating SupplyCurrent	$I_{DDL2.5}$	C_L = 0 pF; Select @ 66.8 MHz		8	15	mA
		C_L = 0 pF; Select @ 100 MHz		11	18	
		C_L = 0 pF; Select @ 133 MHz		17	20	
Powerdown Current	I_{DDLPD}	CL = 0 pF; Input address VDD or GND		<1	10	µA
Skew[1]	$t_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V	1	2.4	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2A}	I_{OH} = -20 mA	2.4	2.85		V
Output Low Voltage	V_{OL2A}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-45	-27	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	22	29		mA
Rise Time[1]	t_{r2A}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f2A}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle[1]	d_{t2A}	V_T = 1.5 V	45		55	%
Skew window[1]	t_{sk2A}	V_T = 1.5 V		80	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2A}$	V_T = 1.5 V		200	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-39	-21	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	22	26		mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.4	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V, < 133 MHz	45	47.5	55	%
		V_T = 1.25 V, >= 133 MHz	42	47	52	
Skew window[1]	t_{sk2B}	V_T = 1.25 V		70	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V		200	300	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-33	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	38	43		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.5	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		180	500	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		15	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-250	75	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL3}	I_{OL} = 19 mA		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-69	-46	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	32	42		mA
Rise Time[1]	T_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1	1.3	ns
Fall Time[1]	T_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.3	2	ns
Duty Cycle[1]	D_{t3}	V_T = 1.5 V	45	50	55	%
Skew window[1]	T_{sk3}	V_T = 1.5 V		185	250	ps
Propagation Time[1] (Buffer In to output)	T_{sk3}	V_T = 1.5 V		4	5	ns

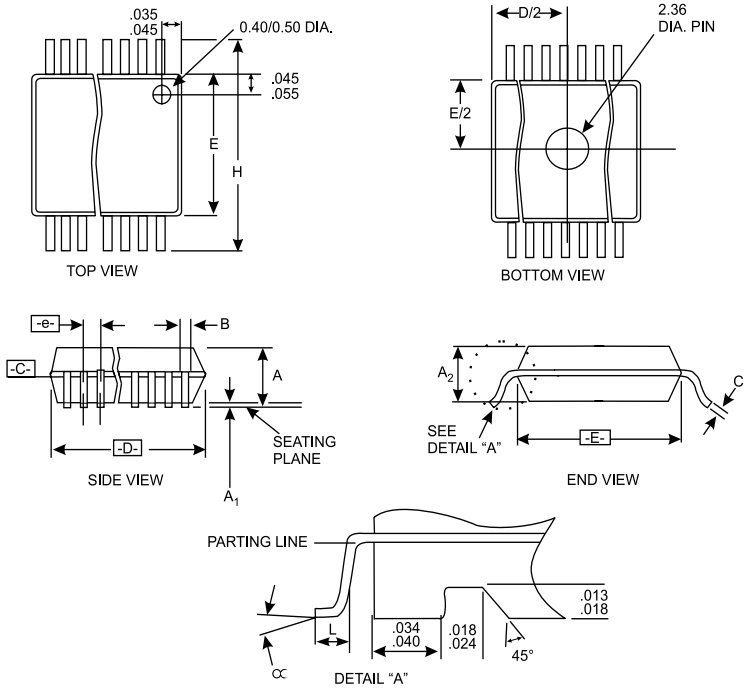
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24,48MHz, REF(0:1)

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 6 mA		0.22	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	1	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		150	250	ps
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-600		600	ps

[1]Guaranteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

SSOP Package

Ordering Information

ICS9248yF-103

Example:

ICS XXXX y F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**