SONY

ICX076AL

Diagonal 3.6mm (Type 1/5) CCD Image Sensor for EIA Black-and-White Video Cameras

For the availability of this product, please contact the sales office.

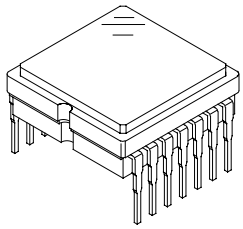
Description

The ICX076AL is an interline CCD solid-state image sensor suitable for EIA black-and-white video cameras. High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration readout system and an electronic shutter with variable charge-storage time.

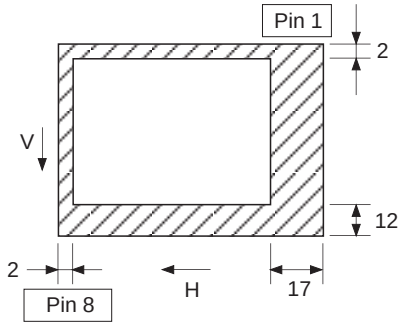
The package is a 10mm-square 14-pin DIP (Plastic).

14 pin DIP (Plastic)



Features

- High sensitivity and low dark current
- 6.75MHz horizontal drive frequency employed
- Electronic iris, backlight compensation function (when CXD2409 is used)
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 5V drive
- Reset gate: 5V drive (no bias adjustment)



Optical black position (Top View)

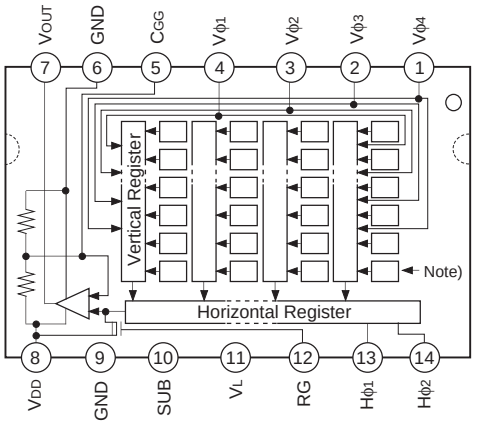
Device Structure

- Image size: Diagonal 3.6mm (Type 1/5)
- Number of effective pixels: 362 (H) × 492 (V) approx. 180K pixels
- Total number of pixels: 381 (H) × 506 (V) approx. 190K pixels
- Interline CCD image sensor
- Chip size: 3.75mm (H) × 3.30mm(V)
- Unit cell size: 8.10µm (H) × 4.45µm(V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 17 pixels
  Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 14
  Vertical 1 (even fields only)
- Substrate material: Silicon

E94608C99

Block Diagram and Pin Configuration

(Top View)



Note) ☐ : Photo sensor

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	8	V_{DD}	Supply voltage
2	Vφ3	Vertical register transfer clock	9	GND	GND
3	Vφ2	Vertical register transfer clock	10	SUB	Substrate (overflow drain)
4	Vφ1	Vertical register transfer clock	11	V_L	Protective transistor bias
5	C_{GG}	Output amplifier gate *1	12	RG	Reset gate clock
6	GND	GND	13	Hφ1	Horizontal register transfer clock
7	V_{OUT}	Signal output	14	Hφ2	Horizontal register transfer clock

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1µF or more.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB – GND		–0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, C_{GG} – GND	–0.3 to +18	V	
	V_{DD}, V_{OUT}, C_{GG} – SUB	–55 to +12	V	
Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4 – GND	–15 to +20	V	
	Vφ1, Vφ2, Vφ3, Vφ4 – SUB	to +12	V	
Voltage difference between vertical clock input pins		to +15	V	*2
Voltage difference between horizontal clock input pins		to +17	V	
Hφ1, Hφ2 – Vφ4		–17 to +17	V	
Hφ1, Hφ2 – GND		–10 to +15	V	
Hφ1, Hφ2 – SUB		–55 to +10	V	
V_L – SUB		–65 to +0.3	V	
Vφ1, Vφ3, V_{DD}, V_{OUT} – V_L		–0.3 to +27.5	V	*3
RG – GND		–0.3 to +22.5	V	
Vφ2, Vφ4, C_{GG}, Hφ1, Hφ2, GND – V_L		–0.3 to +17.5	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*2 +27V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

*3 When C_{GG} or GND (Pin 6) are grounded.
–0.3 to +17.5V when C_{GG} and GND (Pin 6) are to be disconnected.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.25	15.0	15.75	V	
Substrate voltage adjustment range	V_{SUB}	5.0		12.75	V	*1
Substrate voltage adjustment precision		Indicated voltage – 0.1	Indicated voltage	Indicated voltage + 0.1	V	
Protective transistor bias	V_L	*2				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		3	5	mA	
Input current	I_{IN1}			1	µA	*3
Input current	I_{IN2}			10	µA	*4

*1 Indications of substrate voltage (V_{SUB}) setting value

The setting value of the substrate voltage is indicated on the back of image sensor by a special code. Adjust the substrate voltage (V_{SUB}) to the indicated voltage.

V_{SUB} code – one character indication □

↑

V_{SUB} code

Code and optimal setting correspond to each other as follows.

V_{SUB} code	—	=	0	1	2	3	4	6	7	8	9	A	C	d
Optimal setting	5.0	5.25	5.5	5.75	6.0	6.25	6.5	6.75	7.0	7.25	7.5	7.75	8.0	8.25

V_{SUB} code	E	f	G	h	J	K	L	m	N	P	R	S	U	V
Optimal setting	8.5	8.75	9.0	9.25	9.5	9.75	10.0	10.25	10.5	10.75	11.0	11.25	11.5	11.75

V_{SUB} code	W	X	Y	Z
Optimal setting	12.0	12.25	12.5	12.75

<Example> "L" → V_{SUB} = 10.0V

*2 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*3
1) Current to each pin when 16V is applied to V_{DD}, V_{OUT}, RG, C_{GG}, GND (Pin 6), and SUB pins, while pins that are not tested are grounded.
2) Current to each pin when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, and $V\phi_4$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB pin.
3) Current to each pin when 15V is applied sequentially to $H\phi_1$ and $H\phi_2$ pins, while pins that are not tested are grounded. However, 15V is applied to SUB pin.
4) Current to V_L pin when 25V is applied to $V\phi_1$, $V\phi_3$, V_{DD}, and V_{OUT} pins or when, 15V is applied to $V\phi_2$, $V\phi_4$, $H\phi_1$, and $H\phi_2$ pins, while V_L pin is grounded. However, GND and SUB pins are left open.
5) Current to GND pin when 20V is applied to the RG pin and the GND pin is grounded.

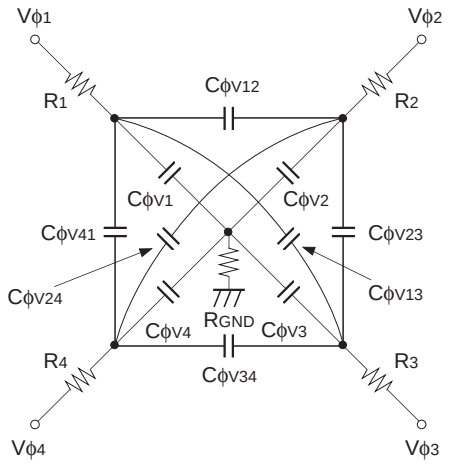
*4 Current to SUB pin when 55V is applied to SUB pin, while all pins that are not tested are grounded.

Clock Voltage Conditions

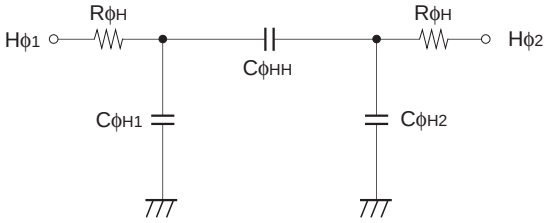
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.25	15.0	15.75	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.5	–8.0	–7.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi V$	7.3	8.0	8.55	V	2	$V\phi V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.3	V	2	High-level coupling
	V_{VHL}			0.3	V	2	High-level coupling
	V_{VLH}			0.3	V	2	Low-level coupling
	V_{VLL}			0.3	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi RG$	4.5	5.0	5.5	V	4	Input through 0.01µF capacitance
	$V_{RGLH} – V_{RGLL}$			0.8	V	4	Low-level coupling
	V_{RGH}	V_{DD} + 0.3	V_{DD} + 0.6	V_{DD} + 0.9	V	4	
Substrate clock voltage	$V\phi SUB$	21.25	22.5	23.75	V	5	

Clock Equivalent Circuit Constant

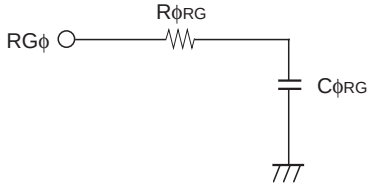
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$, $C\phi V3$		520		pF	
	$C\phi V2$, $C\phi V4$		390		pF	
Capacitance between vertical transfer clocks	$C\phi V12$, $C\phi V34$		220		pF	
	$C\phi V23$, $C\phi V41$		150		pF	
	$C\phi V13$, $C\phi V24$		39		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$, $C\phi H2$		24		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		18		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		3		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		170		pF	
Vertical transfer clock series resistor	$R1$, $R2$, $R3$, $R4$		100		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock series resistor	$R\phi H$		30		Ω	
Reset gate clock series resistor	$R\phi RG$		39		Ω	



Vertical transfer clock equivalent circuit



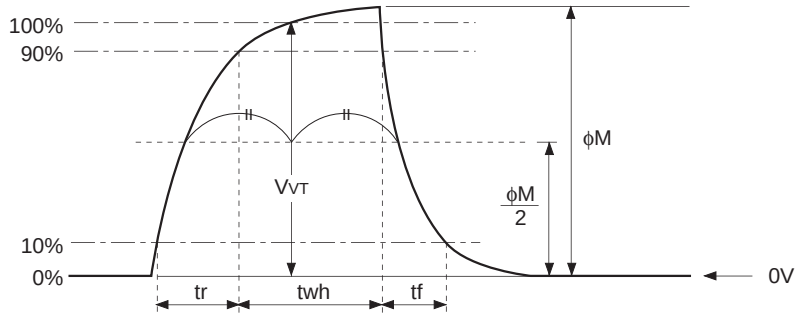
Horizontal transfer clock equivalent circuit



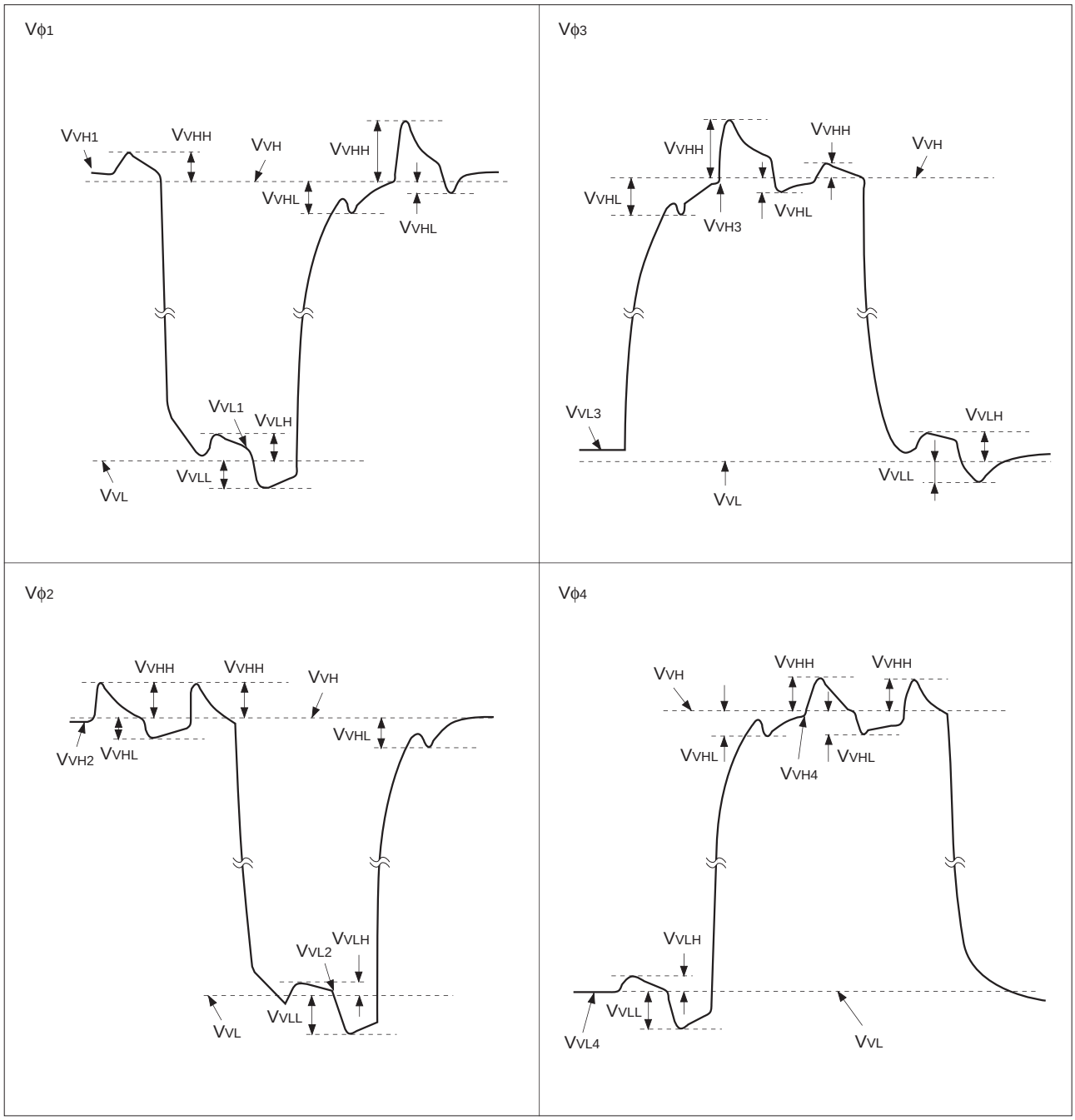
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform

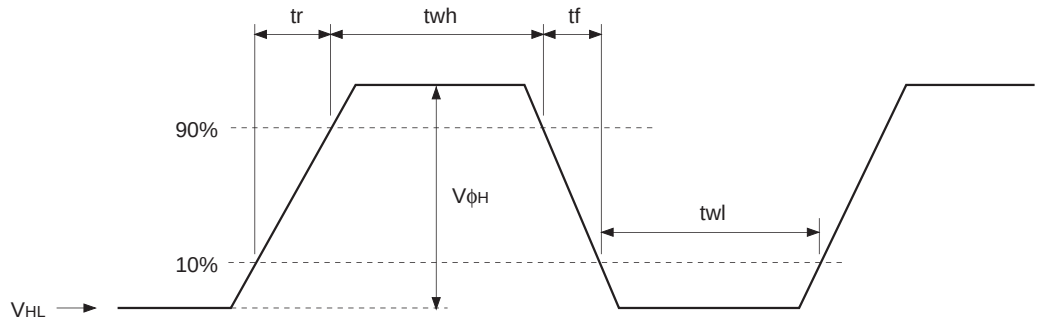


(2) Vertical transfer clock waveform

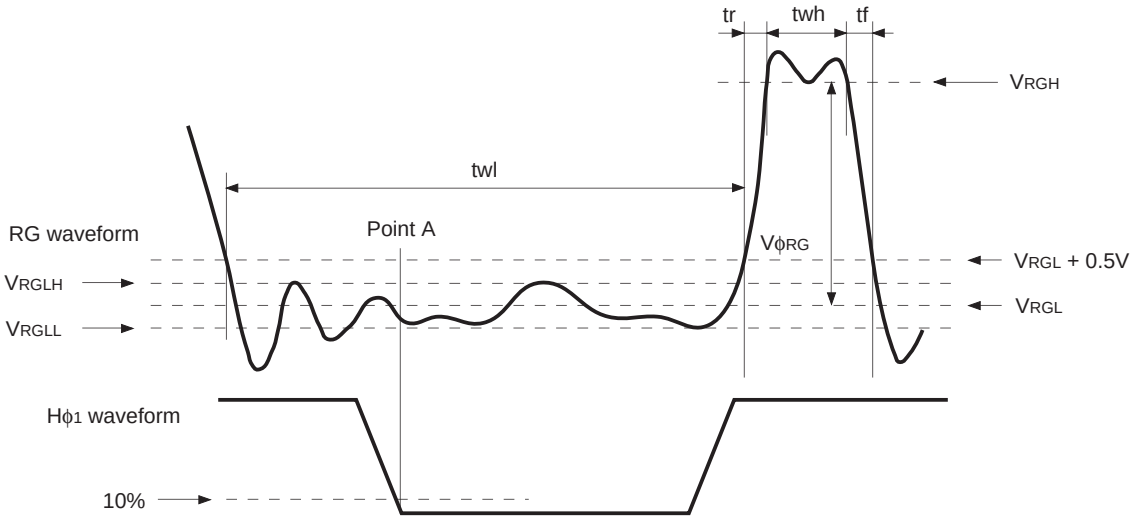


$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



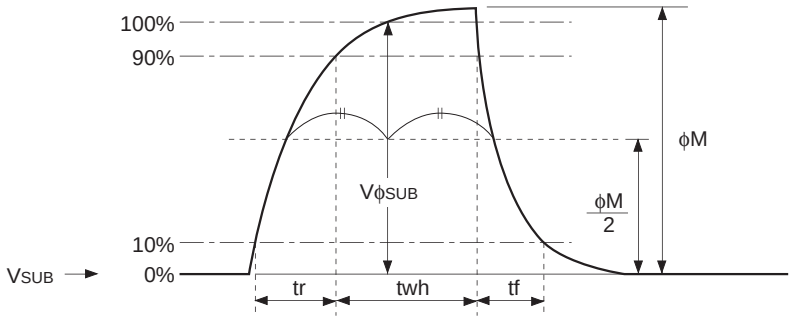
V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	*1
Horizontal transfer clock	$H\phi$	55	67		55	67			9	18		7	18	ns	During imaging
	$H\phi_1$		5.6						0.007			0.007		µs	During parallel-serial conversion
	$H\phi_2$					5.6			0.007			0.007		µs	
Reset gate clock	ϕ_{RG}	25	34			107			8			5		ns	
Substrate clock	ϕ_{SUB}	1.5	1.65							0.5			0.5	µs	During drain charge

*1 When vertical transfer clock driver CXD1267 is used. tr and tf are defined by the rise and fall times for 10% to 90% of the interval between V_{VL} and V_{VH}.

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	285	360		mV	1	
Saturation signal	Vsat	700			mV	2	Ta = 60°C
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SH			25	%	4	Zone II'
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Lag	Lag			0.5	%	7	

Zone Definition of Video Signal Shading

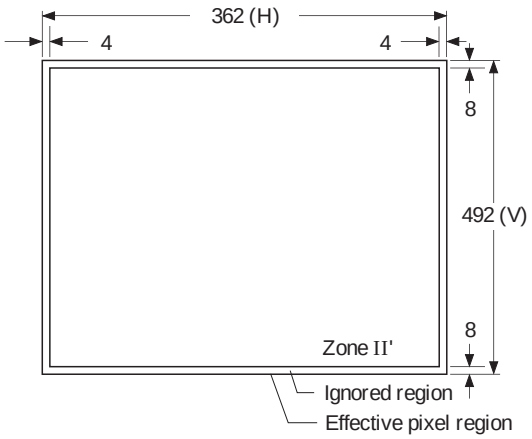


Image Sensor Characteristics Measurement Method

◎ Measurement conditions

1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*A] in the drive circuit example is used.

◎ Definition of standard imaging conditions

1) Standard imaging condition I:
Use a pattern box (luminance 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal (Vs) at the center of the screen and substitute the value into the following formula.

$$S = Vs \times \frac{250}{60} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of signal output, 200mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

$$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%]} \text{ (1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/200 \times 100 \text{ [\%]}$$

5. Dark signal
Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

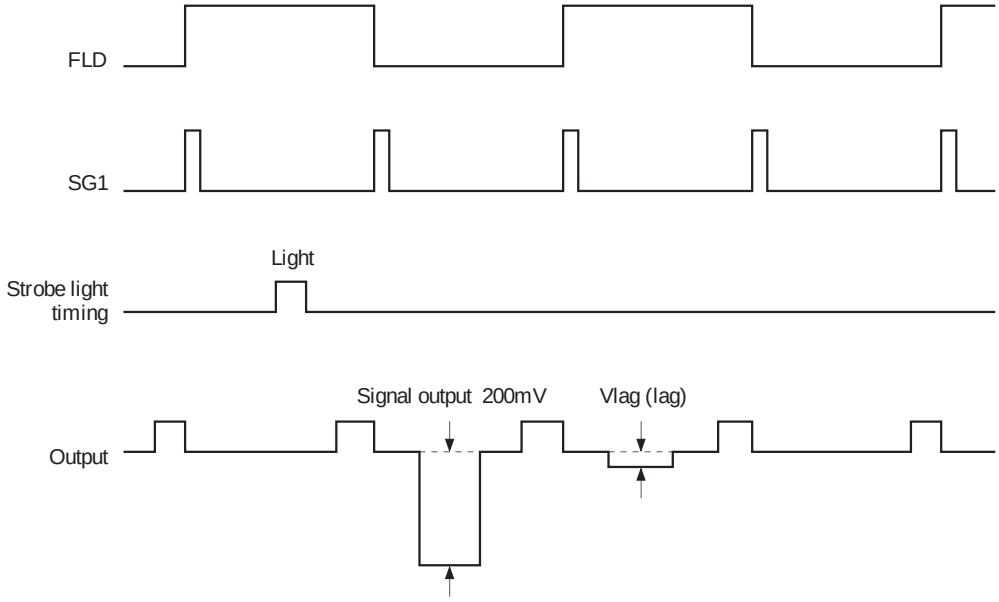
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

   $\Delta Vdt = Vdmax - Vdmin$ [mV]

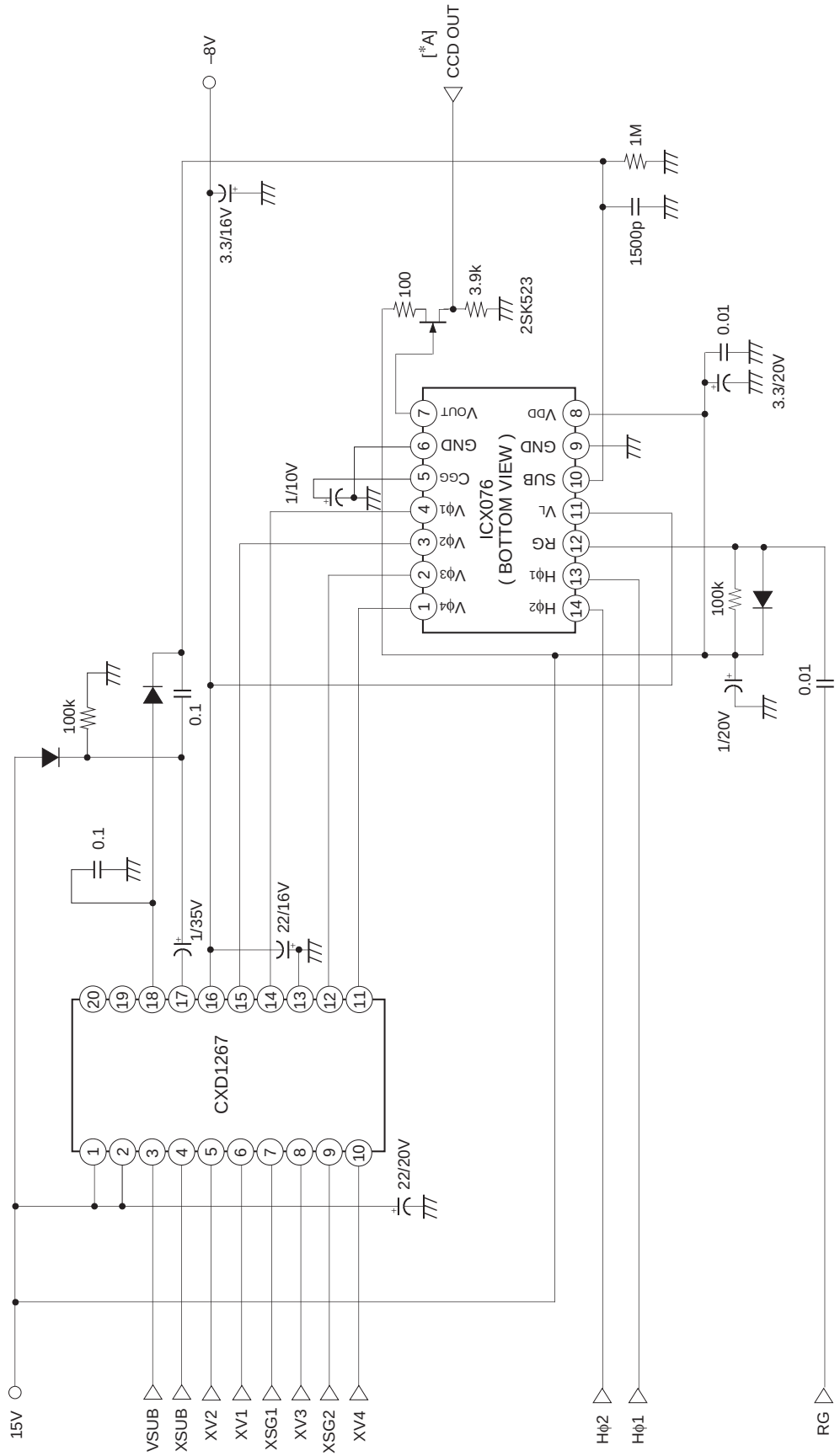
7. Lag

   Adjust the signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/200) \times 100$ [%]

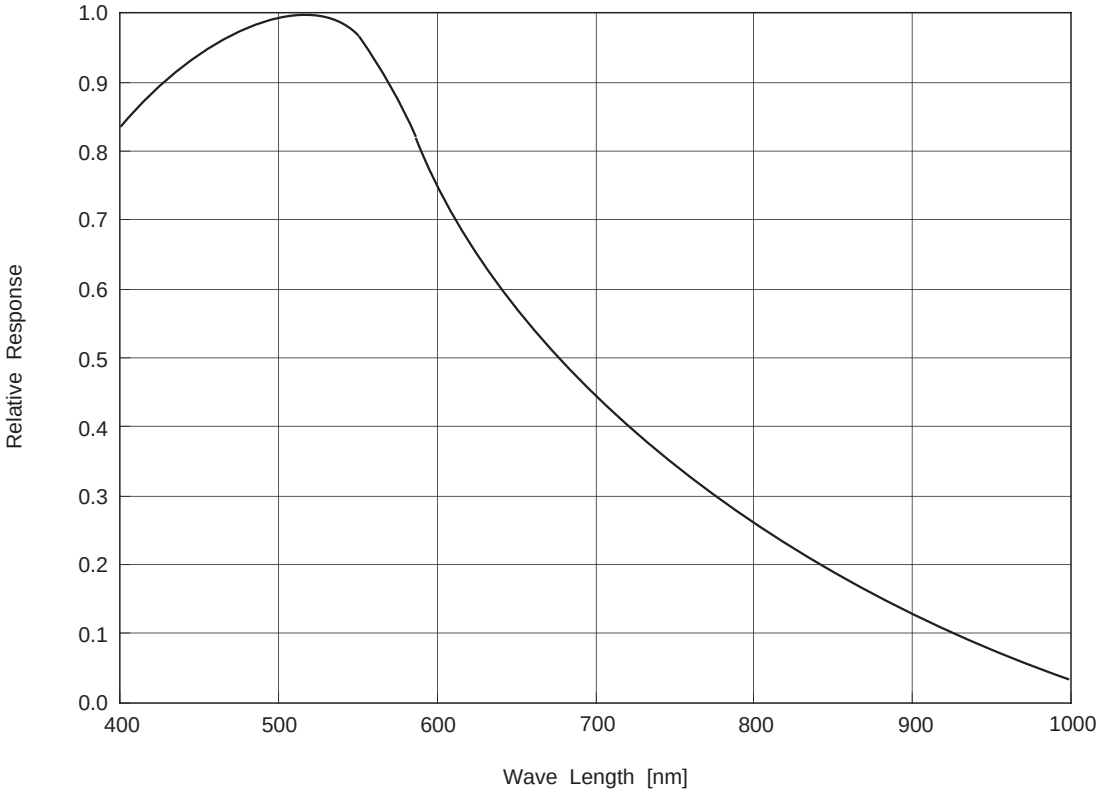


Drive Circuit

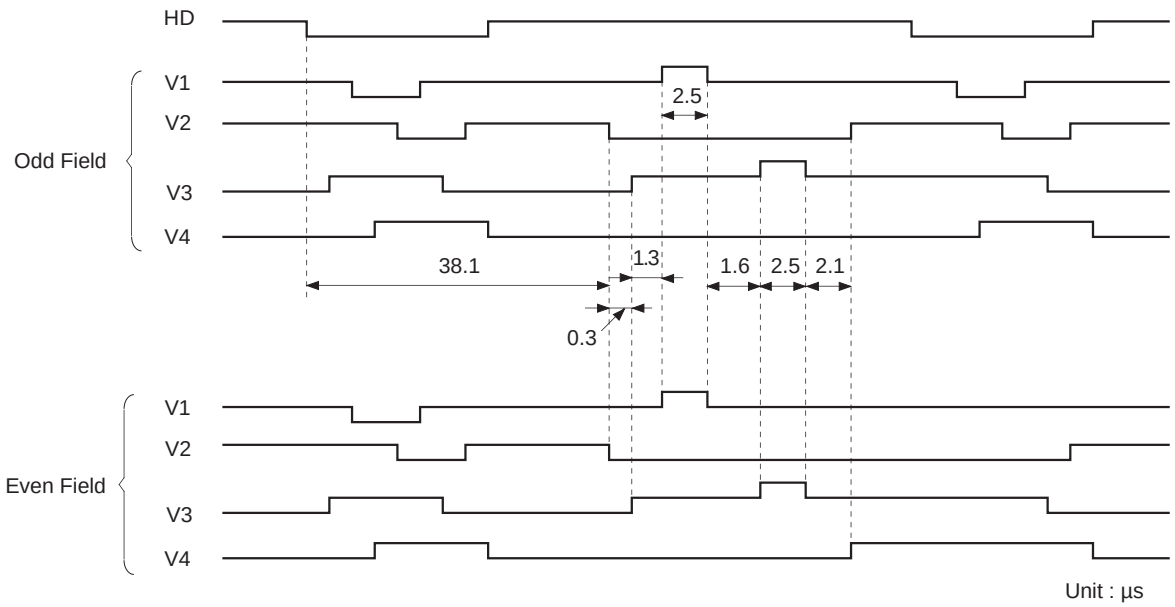


Spectral Sensitivity Characteristics

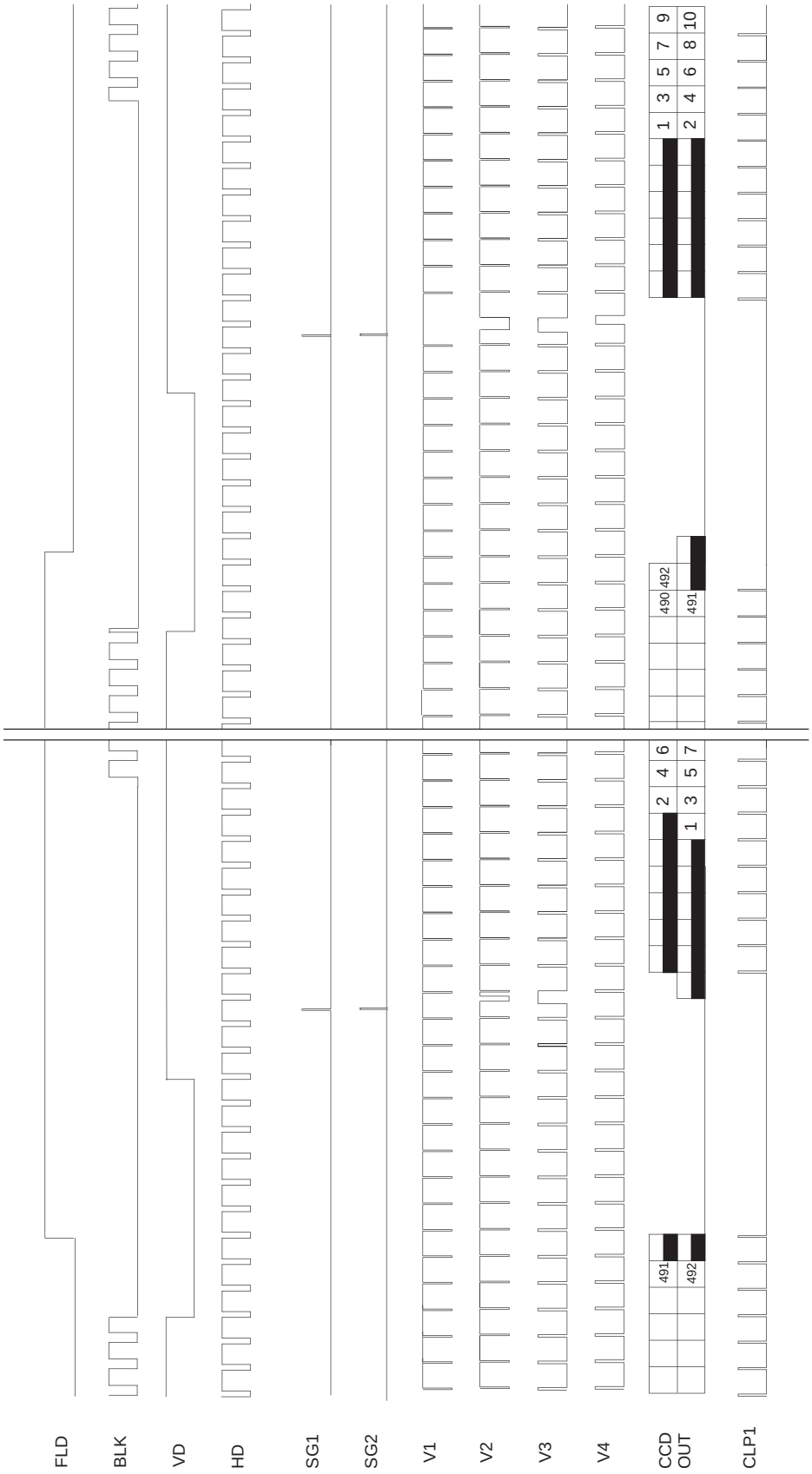
(includes lens characteristics, excludes light source characteristics)



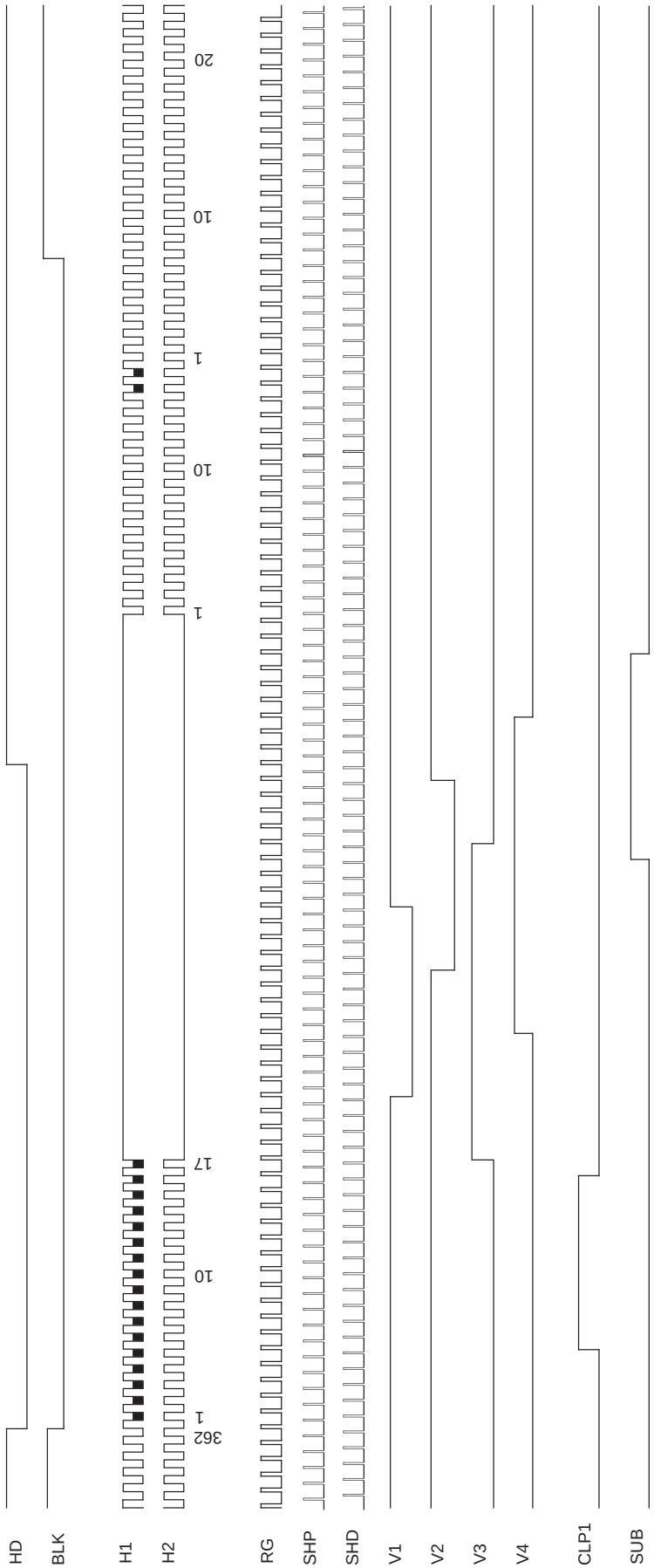
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

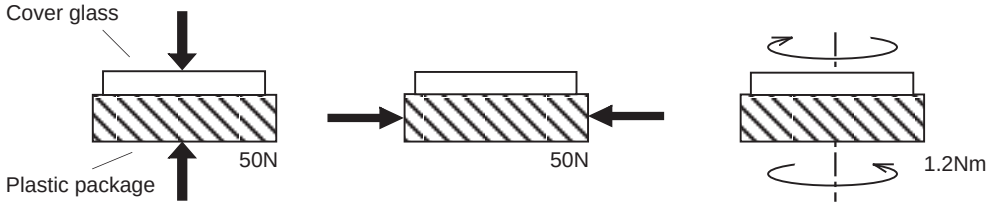
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.

d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.

f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

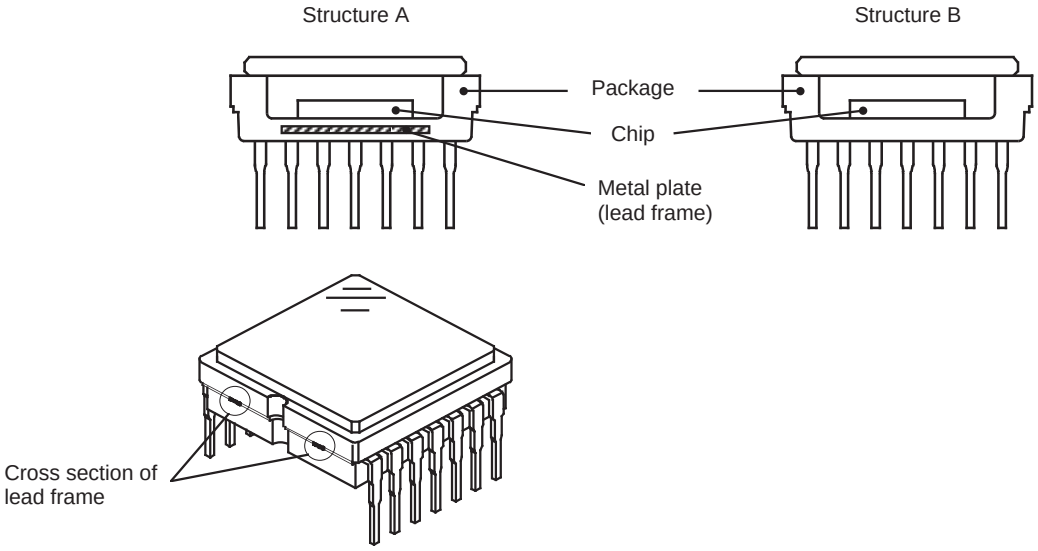
5) Others

a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

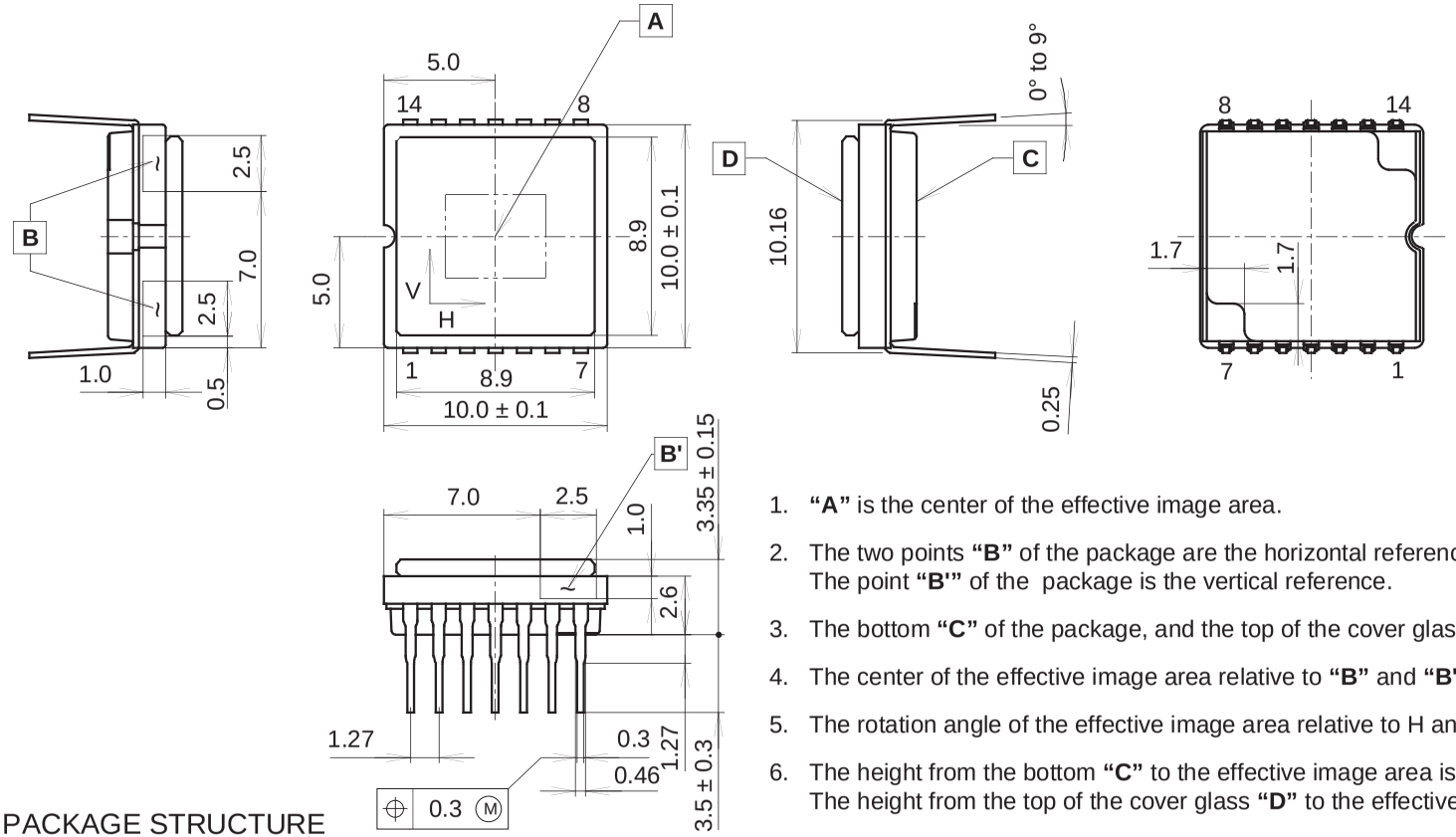
d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

14 pin DIP (400mil)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (5.0, 5.0) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 40µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 40µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.6g