

Diagonal 11mm (Type 2/3) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

Description

The ICX085AL is a diagonal 11mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array. Progressive scan allows all pixels signals to be output independently within approximately 1/12 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

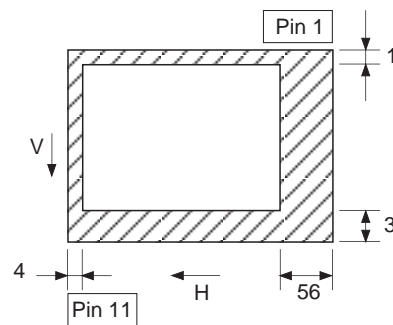
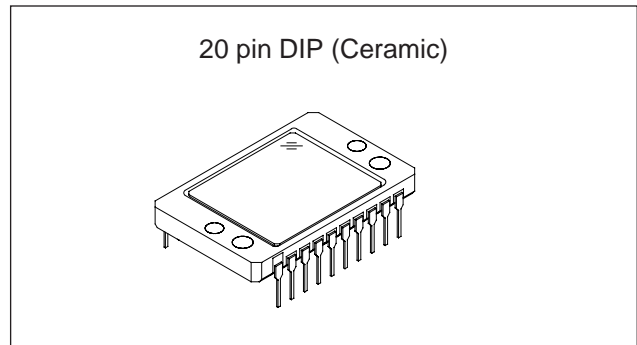
This chip is suitable for image input applications such as still cameras which require high resolution.

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High vertical resolution (1024TV-lines) still image without a mechanical shutter.
- Square pixel unit cell
- Aspect ratio 5:4
- Horizontal drive frequency: 20.25MHz
- Reset gate bias is not adjusted.
- Substrate voltage: 5.5 to 12.5V
- Continuous variable-speed shutter
- High resolution, high sensitivity, low dark current
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 5V drive

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 11mm (Type 2/3)
- Number of effective pixels: 1300 (H) x 1030 (V) approx. 1.3M pixels
- Total number of pixels: 1360 (H) x 1034 (V) approx. 1.4M pixels
- Chip size: 10.0mm (H) x 8.7mm (V)
- Unit cell size: 6.7µm (H) x 6.7µm (V)
- Optical black: Horizontal (H) direction: Front 4 pixels, rear 56 pixels
Vertical (V) direction: Front 3 pixels, rear 1 pixel
- Number of dummy bits: Horizontal 24
Vertical 1
- Substrate material: Silicon

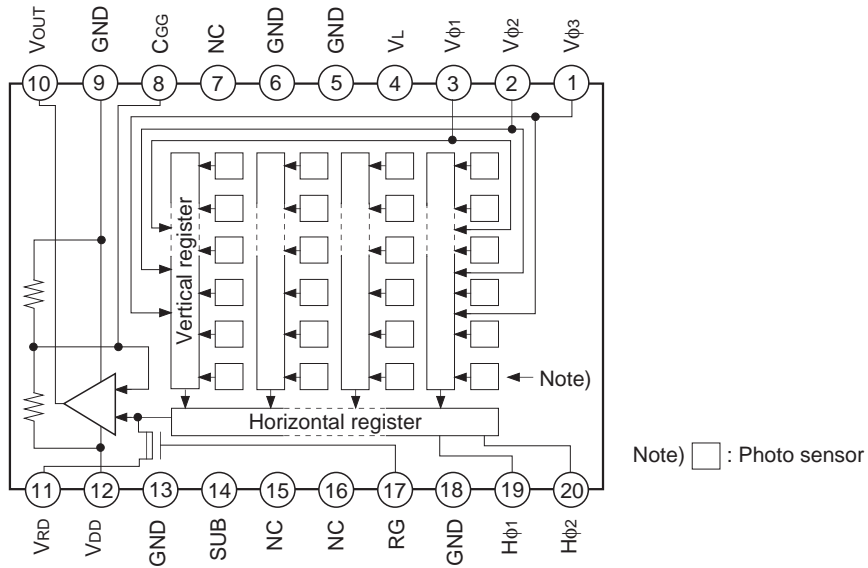


**Optical black position
(Top View)**

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Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_3$	Vertical register transfer clock	11	V_{RD}	Reset drain power supply
2	$V\phi_2$	Vertical register transfer clock	12	V_{DD}	Supply voltage
3	$V\phi_1$	Vertical register transfer clock	13	GND	GND
4	V_L	Protective transistor bias	14	SUB	Substrate (overflow drain)
5	GND	GND	15	NC	
6	GND	GND	16	NC	
7	NC		17	RG	Reset gate clock
8	C_{GG}	Output amplifier gate*1	18	GND	GND
9	GND	GND	19	$H\phi_1$	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	$H\phi_2$	Horizontal register transfer clock

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1 μ F or more.

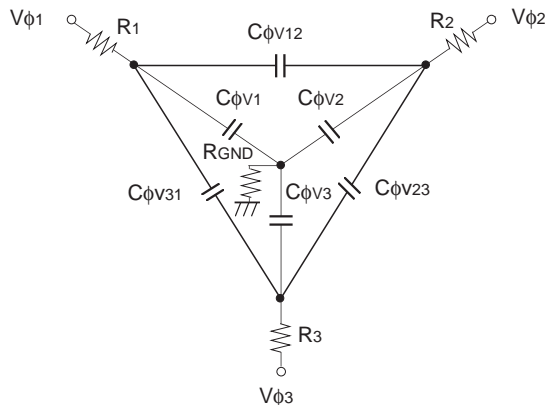
Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		-0.3 to +55	V	
Supply voltage	VDD, VOUT, VRD, CGG-GND	-0.3 to +18	V	
	VDD, VOUT, VRD, CGG-SUB	-55 to +9	V	
Vertical clock input voltage	V ϕ 1, V ϕ 2, V ϕ 3-GND	-15 to +16	V	
	V ϕ 1, V ϕ 2, V ϕ 3-SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +16	V	
H ϕ 1, H ϕ 2-V ϕ 3		-16 to +16	V	
H ϕ 1, H ϕ 2-GND		-10 to +15	V	
H ϕ 1, H ϕ 2-SUB		-55 to +10	V	
VL-SUB		-65 to +0.3	V	
V ϕ 2, V ϕ 3-VL		-0.3 to +27.5	V	
RG-GND		-0.3 to +20.5	V	
V ϕ 1, H ϕ 1, H ϕ 2, GND-VL		-0.3 to +17.5	V	
Storage temperature		-30 to +80	°C	
Operating temperature		-10 to +60	°C	

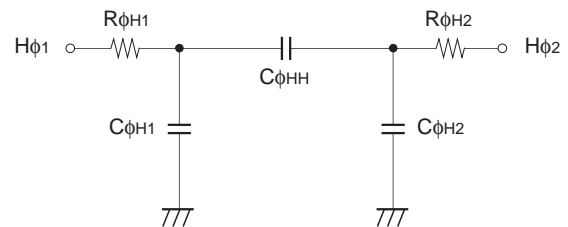
*1 +24V (Max.) when clock width < 10 μ s, clock duty factor < 0.1%.

Clock Equivalent Circuit Constant

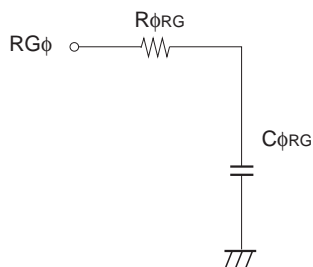
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		5000		pF	
	$C_{\phi V2}, C_{\phi V3}$		10000		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$		1200		pF	
	$C_{\phi V23}$		100		pF	
	$C_{\phi V31}$		3300		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		82		pF	
	$C_{\phi H2}$		68		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		22		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		6		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		800		pF	
Vertical transfer clock series resistor	R_1, R_2, R_3		30		Ω	
Vertical transfer clock ground resistor	R_{GND}		30		Ω	
Horizontal transfer clock series resistor	$R_{\phi H1}, R_{\phi H2}$		10		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		20		Ω	



Vertical transfer clock equivalent circuit



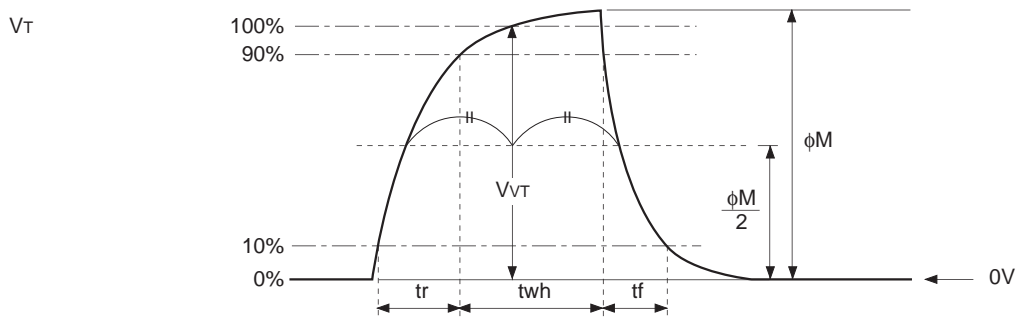
Horizontal transfer clock equivalent circuit



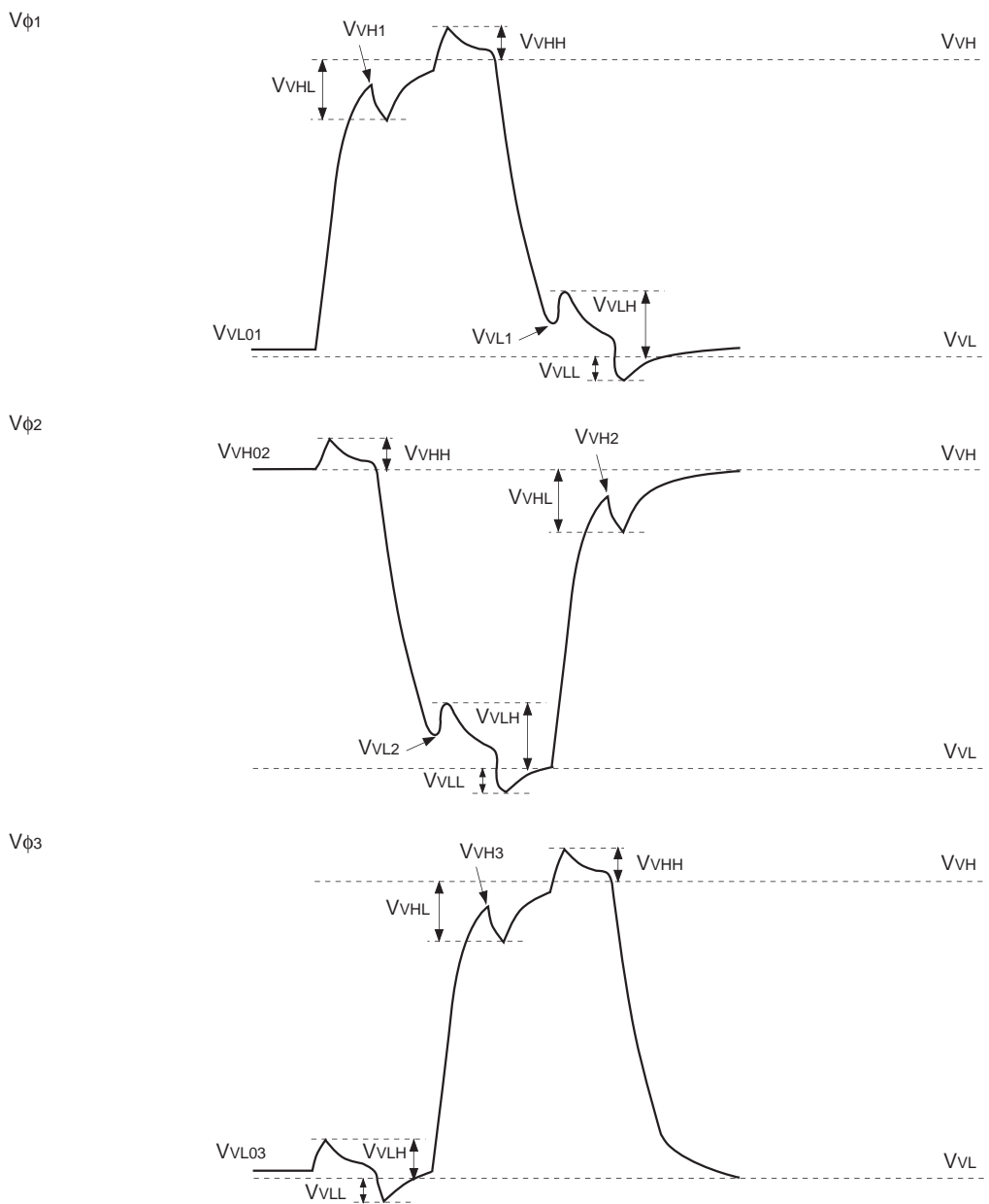
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform



$$V_{VH} = V_{VH02}$$

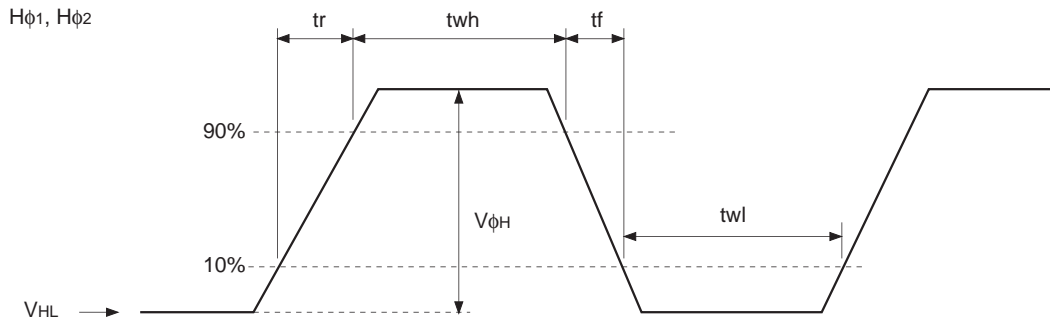
$$V_{VL} = (V_{VL01} + V_{VL03}) / 2$$

$$V_{\phi 1} = V_{VH1} - V_{VL01}$$

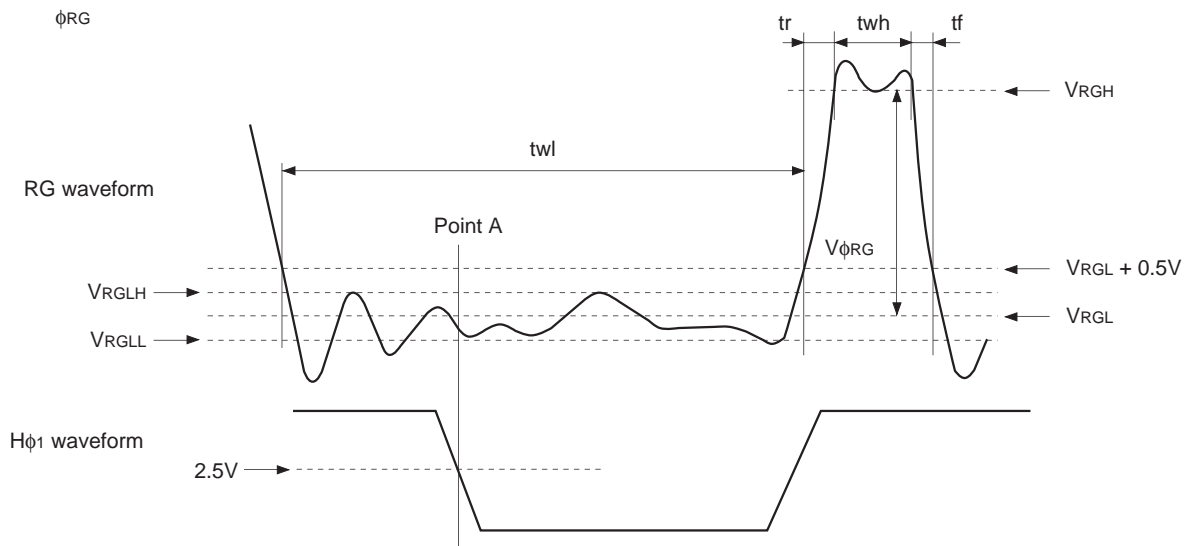
$$V_{\phi 2} = V_{VH02} - V_{VL2}$$

$$V_{\phi 3} = V_{VH3} - V_{VL03}$$

(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



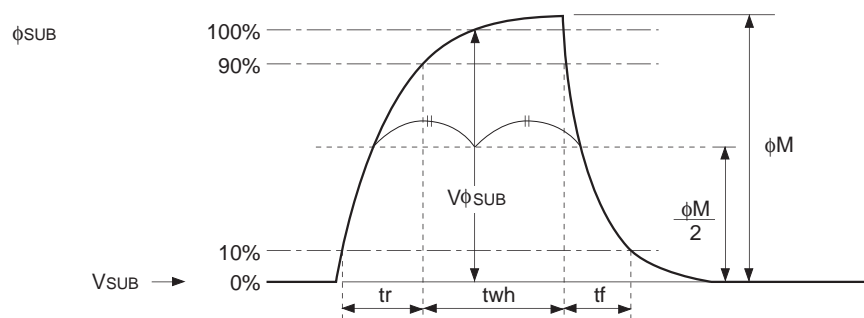
V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL} .

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

Assuming V_{RGH} is the minimum value during the interval t_{wh} , then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Readout clock	V _T	4.6	5.0						0.5			0.5		μs	During readout	
Vertical transfer clock	V _{φ1} , V _{φ2} , V _{φ3}											52.5	110	ns	*1	
Horizontal transfer clock	During imaging	H _{φ1}	15	18		15	19			6	10.6		6	10.6	ns	*2
		H _{φ2}	16	19		15	18			6	10.6		6	10.6		
	During parallel-serial conversion	H _{φ1}								0.01			0.01		μs	
		H _{φ2}								0.01			0.01			
Reset gate clock	φ _{RG}	7	8			37.9			2.5			2.5		ns		
Substrate clock	φ _{SUB}	1.8	2.1							0.5			0.5	μs	During drain charge	

*1 When vertical transfer clock driver CXD1268M × 2 is used.

*2 $t_f \geq t_r - 2\text{ns}$, and the cross-point voltage (V_{CR}) for the H_{φ1} rising side of the H_{φ1} and H_{φ2} waveforms must be at least 2.5V.

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H _{φ1} , H _{φ2}	13.0	15.5		ns	*3

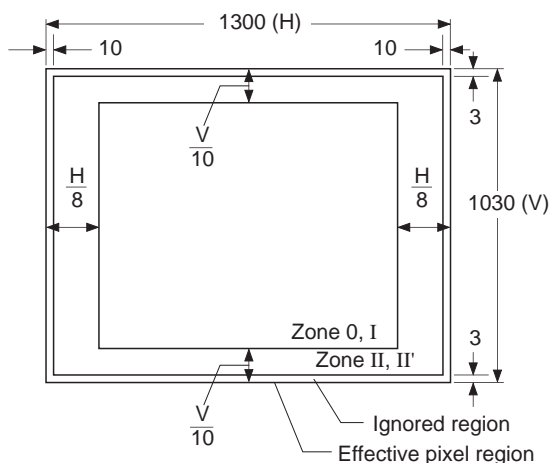
*3 The overlap period for twh and twl of horizontal transfer clocks H_{φ1} and H_{φ2} is two.

Image Sensor Characteristics

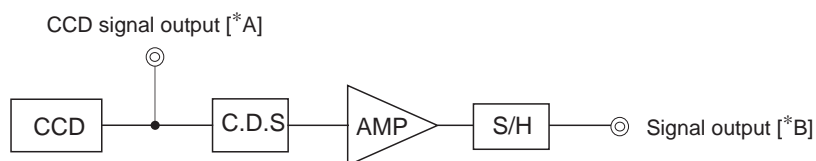
(1/12 second accumulation mode, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	1300	1600		mV	1	
Saturation signal	Vsat	400			mV	2	Ta = 60°C
Smear	Sm		0.005	0.008	%	3	
Video signal shading	SH			20	%	4	Zone 0 and I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			8	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			4	mV	6	Ta = 60°C
Lag	Lag			0.5	%	7	

Zone Definition of Video Signal Shading



Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

Image Sensor Characteristics Measurement Method

Measurement conditions

- 1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.
- 2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [*B] of the measurement system.

Definition of standard imaging conditions

- 1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.
- 2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/80s, measure the signal output (Vs) at the center of the screen, and substitute the value into the following formula.

$$S = V_s \times \frac{80}{12} \text{ [mV]}$$

2. Saturation signal

Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

3. Smear

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm [mV]) of the signal output and substitute the value into the following formula.

$$S_m = \frac{V_{Sm}}{150} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [%]} \text{ (1/10 V method conversion value)}$$

4. Video signal shading

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum (V_{max} [mV]) and minimum (V_{min} [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min})/150 \times 100 [\%]$$

5. Dark signal

Measure the average value of the signal output (V_{dt} [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

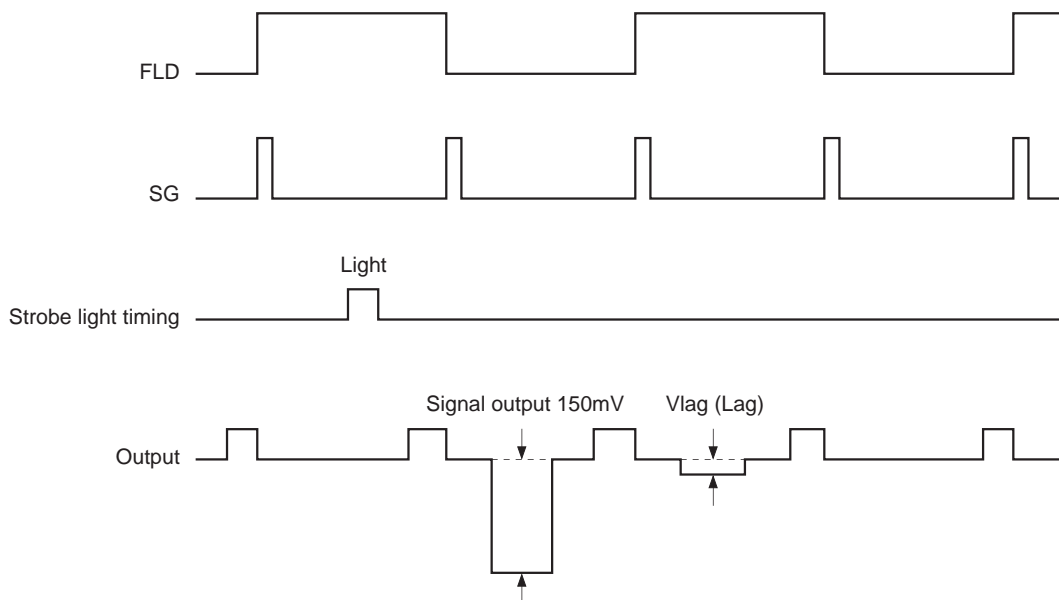
After measuring 5, measure the maximum (V_{dmax} [mV]) and minimum (V_{dmin} [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} [\text{mV}]$$

7. Lag

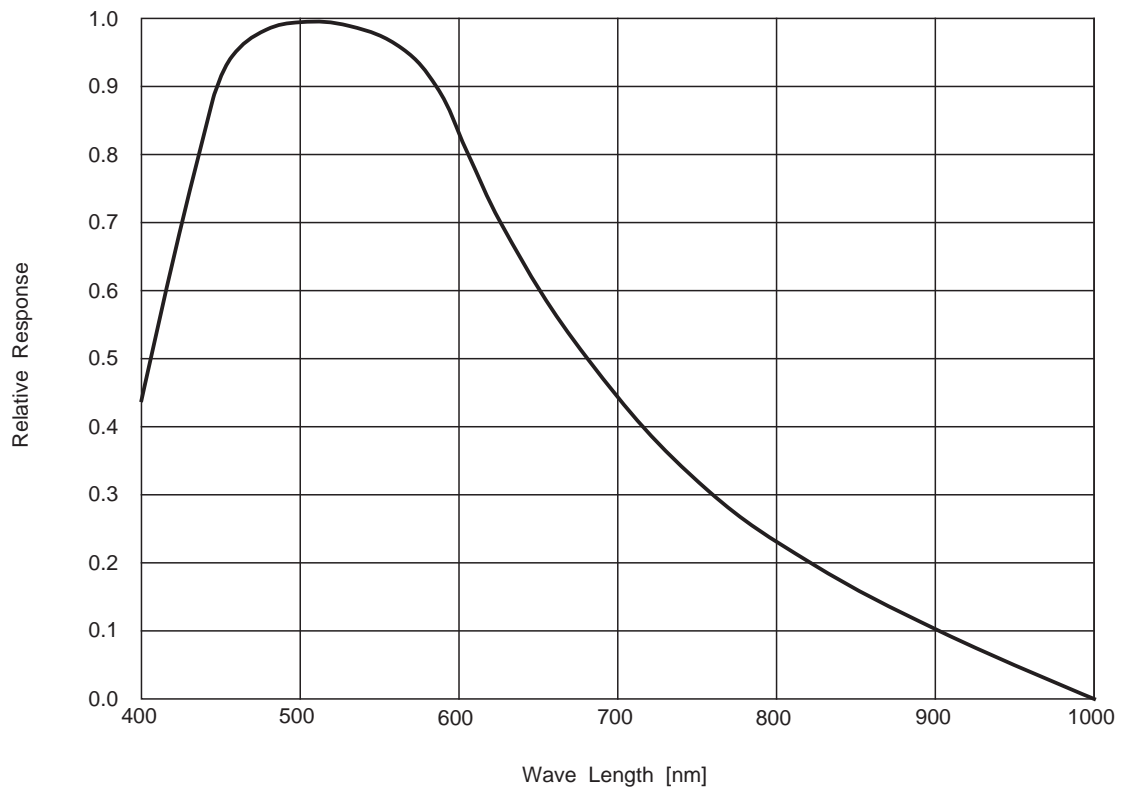
Adjust the signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobescs with the following timing, measure the residual signal (V_{lag}). Substitute the value into the following formula.

$$Lag = (V_{lag}/150) \times 100 [\%]$$

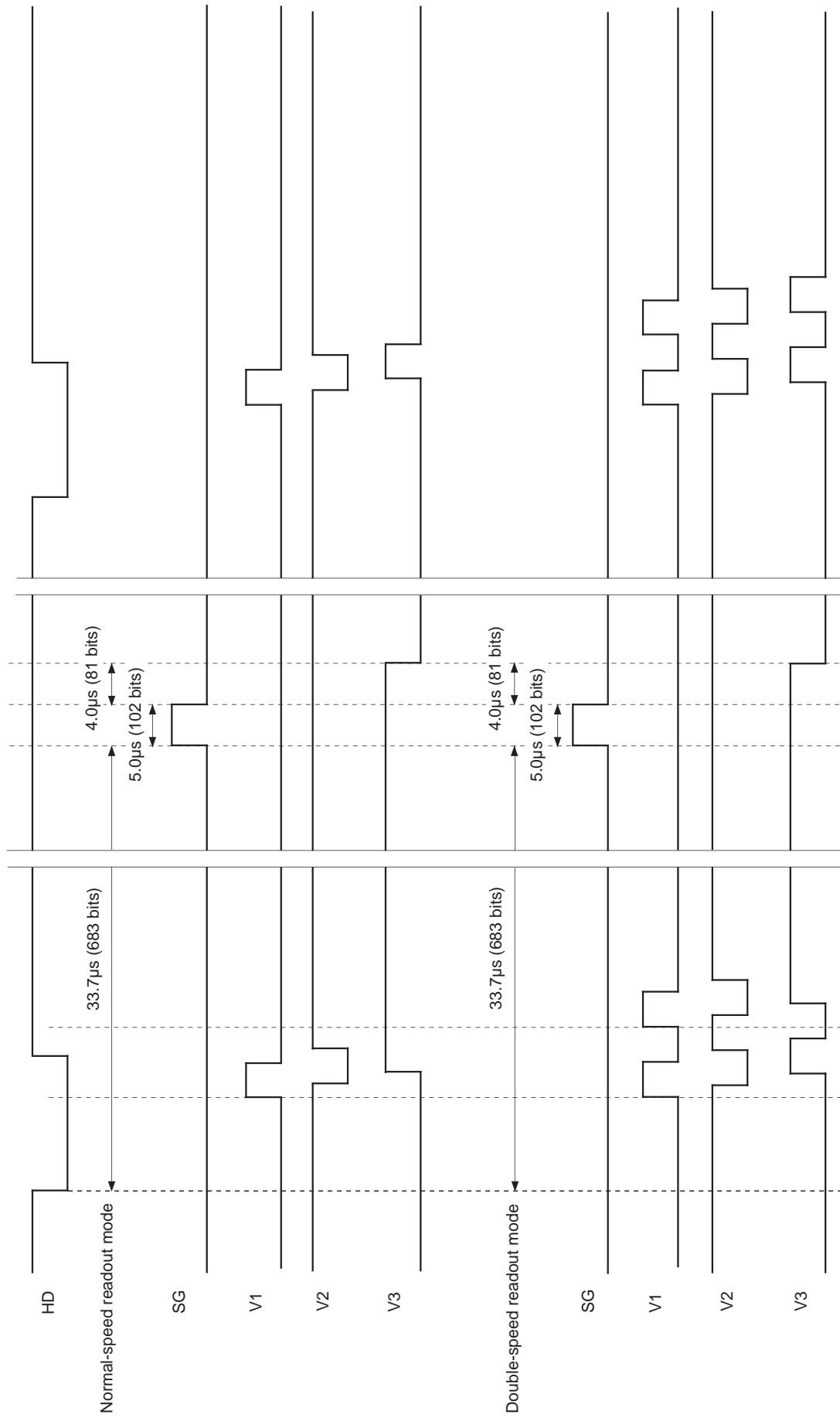


Spectral Sensitivity Characteristics

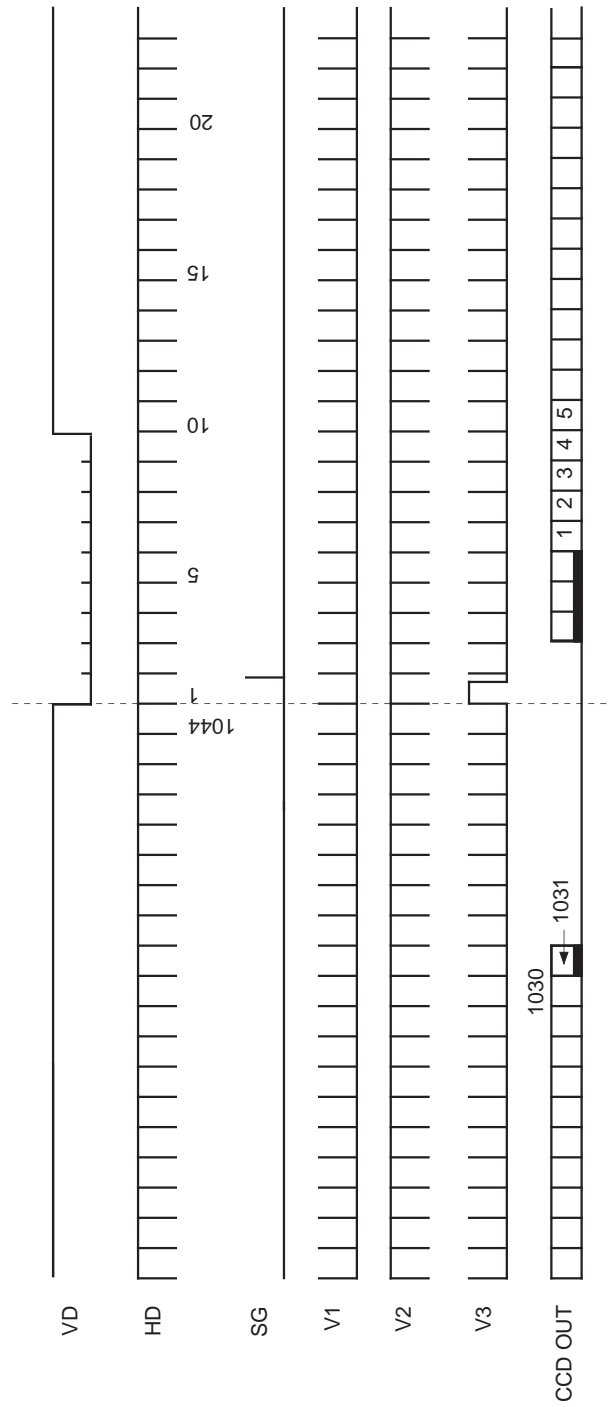
(Includes lens characteristics, excludes light source characteristics)



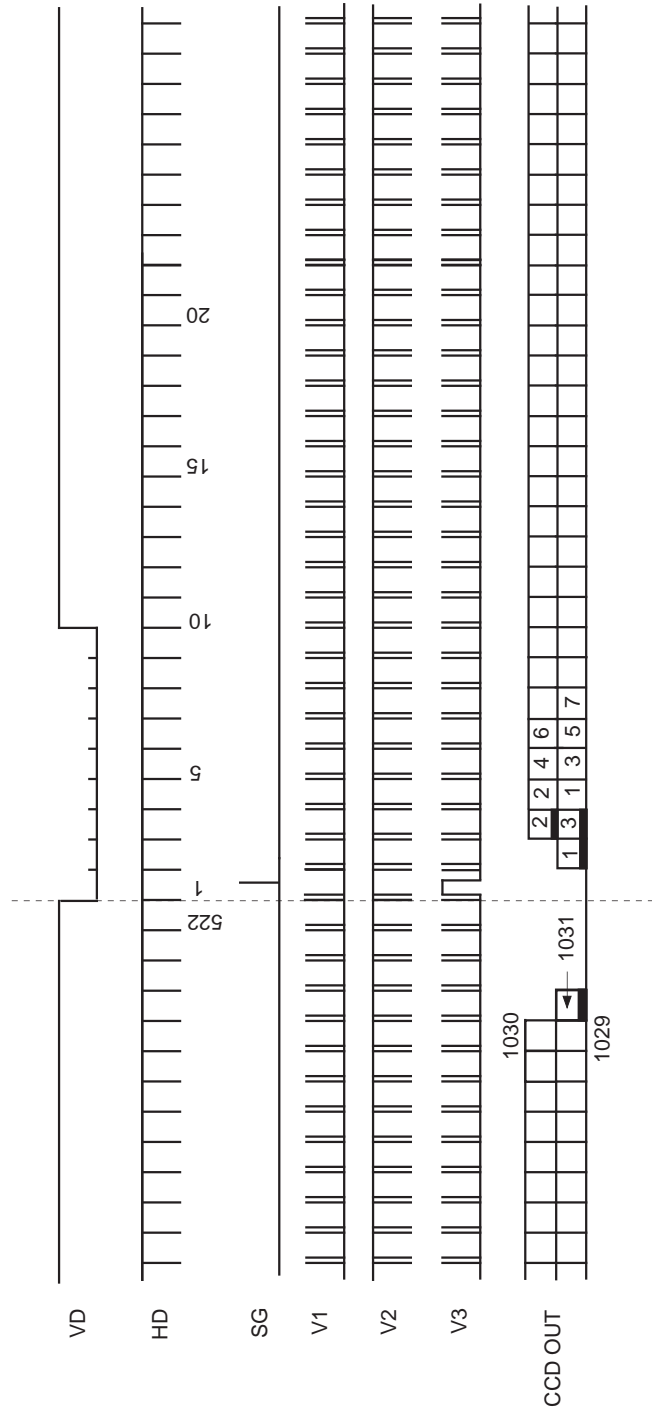
Sensor Readout Clock Timing Chart



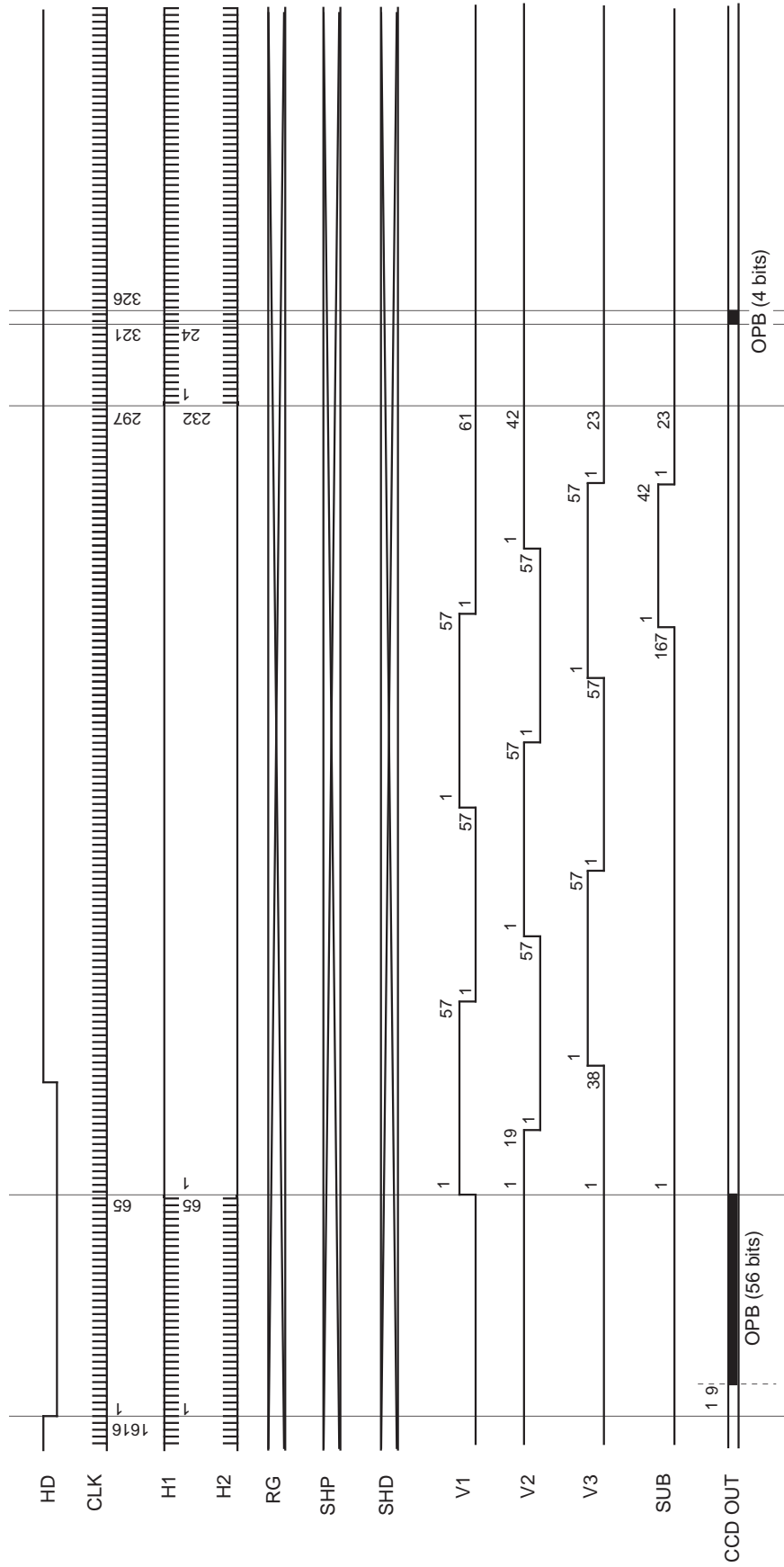
Drive Timing Chart (Vertical Sync) Normal-speed readout mode



Drive Timing Chart (Vertical Sync) Double-speed readout mode



Drive Timing Chart (Horizontal Sync) Double-speed readout mode



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

- a) Operate in clean environments (around class 1000 is appropriate).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

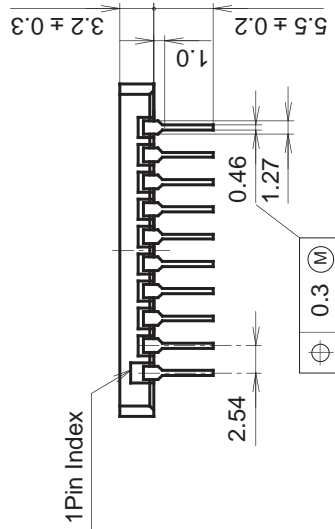
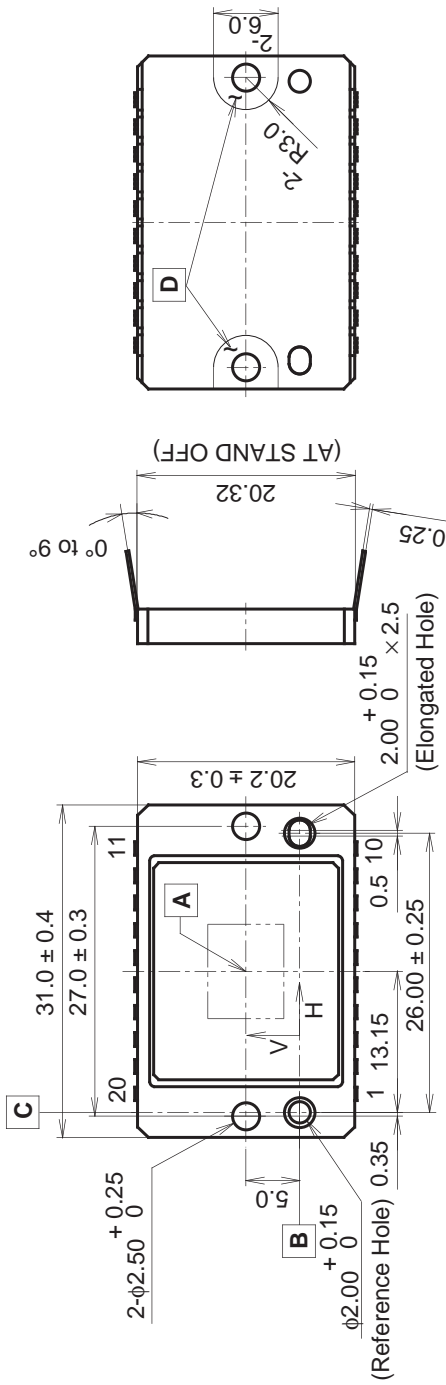
4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

20pin DIP (800mil)



1. "A" is the center of the effective image sensor area.
2. A straight line "B" which passes through the centers of the reference hole and the elongated hole is the reference axis of vertical direction.
3. A straight line "C" which passes through the center of the reference hole at right angles to vertical reference line "B" is the reference axis of horizontal direction.
4. The bottom "D" is the height reference. (Two points are specified.)
5. The center of the effective image area, specified relative to the reference hole is (H, V) = (13.15, 5.0) ± 0.15mm.
6. The angle of rotation relative to the reference line "B" is less than ± 1°.
7. The height from the bottom "D" to the effective image area is 1.46 ± 0.15mm.
8. Planar orientation of the effective image area relative to the bottom "D" is less than 60µm.
9. The thickness of the cover glass is 0.75mm and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.9g