Product Overview

SHARP®

Integrated Circuits Group

ID242 Series

Flash Memory Card

(Model Numbers: ID242xxx)

Spec No.: CPS0002-002
Issue Date: May, 1998

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  - Machine tools
  - Audiovisual equipment
  - Home appliances
  - Communication equipment other than for trunk lines

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  - Mainframe computers
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  - Gas leak detectors and automatic cutoff devices
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  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
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Contents

1. Introduction

This datasheet is for SHARP's ID242 series flash memory card. This datasheet provides all AC and DC characteristics (including timing waveforms) and a convenient reference for the device command set and the card's integrated registers(including the Flash Memory's status registers). This datasheet provides description of the methods which are very helpful for customer to use the card.

2. Features

2.1 Type Flash Memory Card

2.2 Overview

		ID242Dxx	ID242Exx	ID242Gxx	ID242Hxx	ID242Kxx	ID242Lxx
Common Memory Capacity	Byte	2Mbyte	4Mbyte	8Mbyte	10Mbyte	16Mbyte	20Mbyte
	Word	1Mword	2Mword	4Mword	5Mword	8Mword	10Mword
Device		LH28F008SC 2devices	LH28F008SC 4devices	LH28F008SC 8devices	LH28F008SC 10devices	LH28F016SC 8devices	LH28F016SC 10devices
Attribute Memory Capasity		2Kbyte (Note:standard CIS is not writable)					
Supply Voltage		Smart Voltage					
Access time		150ns(@Vcc=5v) 250ns(@Vcc=3.3v)					
Erase Unit		64K word blocks					
Program/Erase Cycles		100,000cycles/Block					
External Dimensions		PCMCIA Type 1 54.0× 85.6× 3.3mm					

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2.3 Interface Parallel I/O Interface

2.4 Function Table See Function Table in page. 9

2.5 Pin Connections See Pin Connections in page. 6

(Card connector: JC20-J68S-NB3 JAE or FCN-568J068-G/0 Fujitsu)

2.7 Operating Temperature 0 to 60°C

2.8 Storage Temperature -20 to 65°C

2.9 Not designed for rated radiation hardened.

3. Block Diagram

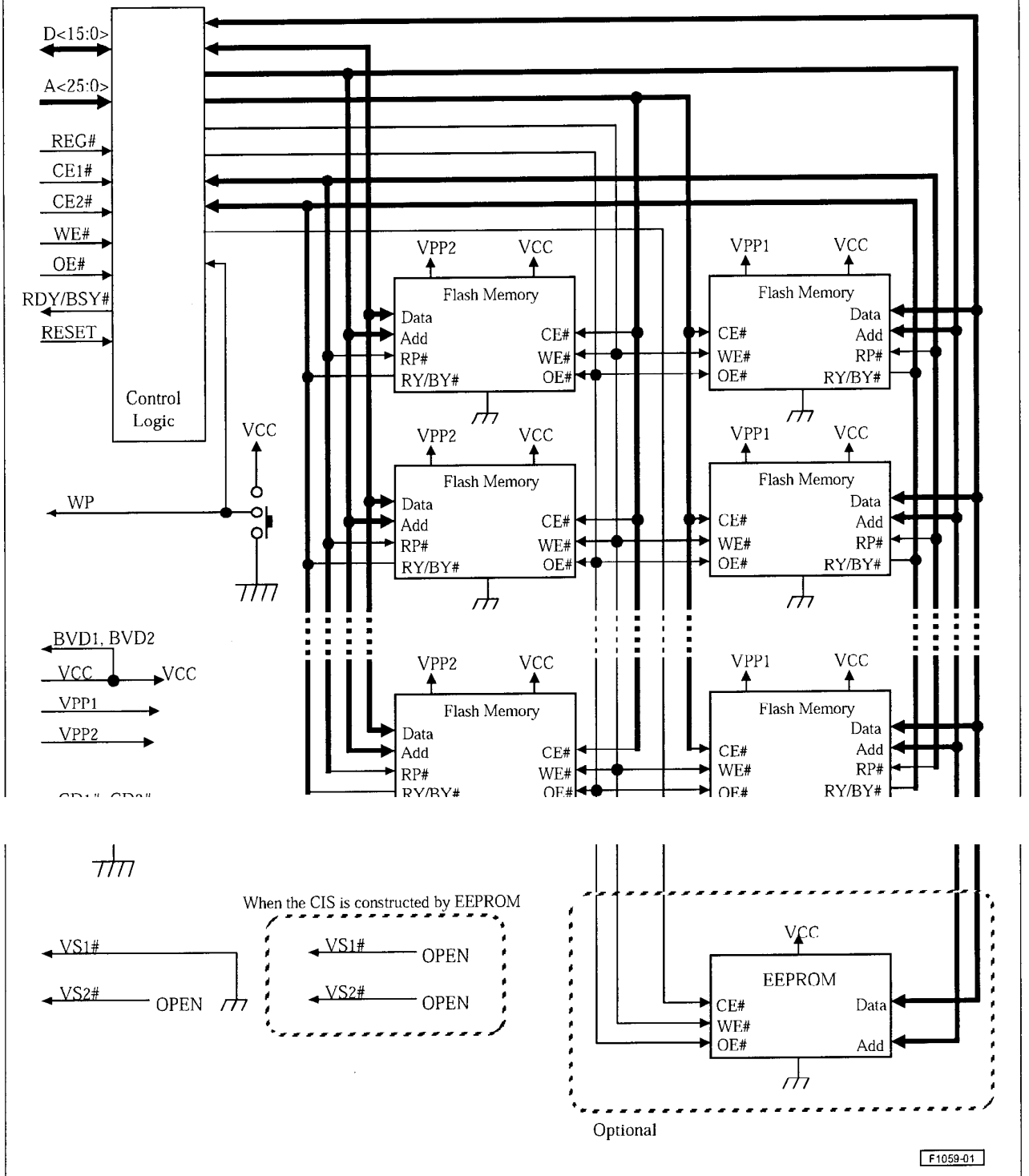

Figure 1. Block Diagram

4. Pin Connections

Table 1. Pin Connections

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
1	GND		Ground	
2	D_3	I/O	Data Bit 3	
3	D_4	I/O	Data Bit 4	
4	D_5	I/O	Data Bit 5	
5	D_6	I/O	Data Bit 6	
6	D_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Program Voltage	
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	
30	D_0	I/O	Data Bit 0	
31	D_1	I/O	Data Bit 1	
32	D_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	D_{11}	I/O	Data Bit 11	
38	D_{12}	I/O	Data Bit 12	
39	D_{13}	I/O	Data Bit 13	
40	D_{14}	I/O	Data Bit 14	
41	D_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1#	O	Voltage Sense 1	
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Program Voltage	
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	
58	RESET	I	Reset	HIGH
59	RFU		Reserved	
60	RFU		Reserved	
61	REG#	I	Atribute Memory Select	LOW
62	BVD_2	O	Battery Boltage Detect 2	
63	BVD_1	O	Battery Boltage Detect 1	
64	D_8	I/O	Data Bit 8	
65	D_9	I/O	Data Bit 9	
66	D_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

5. Signal Description

Table 2. Signal Description

Symbol	I/O	Electrical Interface	Function
A_0-A_{25}	I	Pull-down (250kΩ@Vcc=5v)	ADDRESS INPUTS: These are address bus lines which enable direct addressing of memory on the card. Signal A_0 is not used in word access mode. The system should NOT access memory beyond the card's density, because the upper addresses are not decoded.
D_0-D_{15}	I/O	Pull-down (250kΩ@Vcc=5v)	DATA INPUT/OUTPUT: D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CE_1#,CE_2#	I	Pull-up (250kΩ@Vcc=5v)	CARD ENABLE 1 & 2: CE_1# enables D_0-D_7, CE_2# enables D_8-D_{15}.
OE#	I	Pull-up (250kΩ@Vcc=5v)	OUTPUT ENABLE: Active low signal gating read data from the memory card.
WE#	I	Pull-up (250kΩ@Vcc=5v)	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/BSY#	O		READY/BUSY OUTPUT: Indicates status of internally timed erase or write activities. ID242 series has two types of Ready/Busy output mode; PCMCIA mode and High-Performance mode. In PCMCIA mode, a high output indicates the memory card is ready to accept accesses. A low output indicates that a device in the memory card is busy. In High-Performance mode, the card outputs low when the card is in default state. A high output indicates at least one of flash memory devices in the card comes to be ready to accept accesses.
CD_1#, CD_2#	O	Pull-down 0W	CARD DETECT 1 & 2: These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	O	Low:Pull-down 0W High:Pull-up 100kW	WRITE PROTECT: Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected.
V_{PP1}, V_{PP2}			WRITE/ERASE POWER SUPPLY 1 & 2:
V_{CC}			CARD POWER SUPPLY:
GND			GROUND:
REG#	I	Pull-up (250kW@Vcc=5v)	REGISTER SELECT: Provides access to attribute memory when REG# is low.
RESET	I	Pull-up (250kW@Vcc=5v)	RESET: Active high signal for placing card in Power-On Default State.
BVD_1, BVD_2	O	Pull-up 100kW	BATTERY VOLTAGE DETECT 1 & 2: These signals are pulled high to maintain SRAM card compatibility.
VS_1#, VS_2#	O	VS_1#: Pull-down or N.C. VS_2#: N.C.	VOLTAGE SENSE 1 & 2: Notifies the host socket of the CIS's VCC requirements. VS_1# is pulled-down to ground when using the standard CIS, that indicate 3.3V operating is available. And when using the EEPROM for CIS, the VS_2# is open. That indicate the available operation voltage is 5V only.
RFU			RESERVED FOR FUTURE USE

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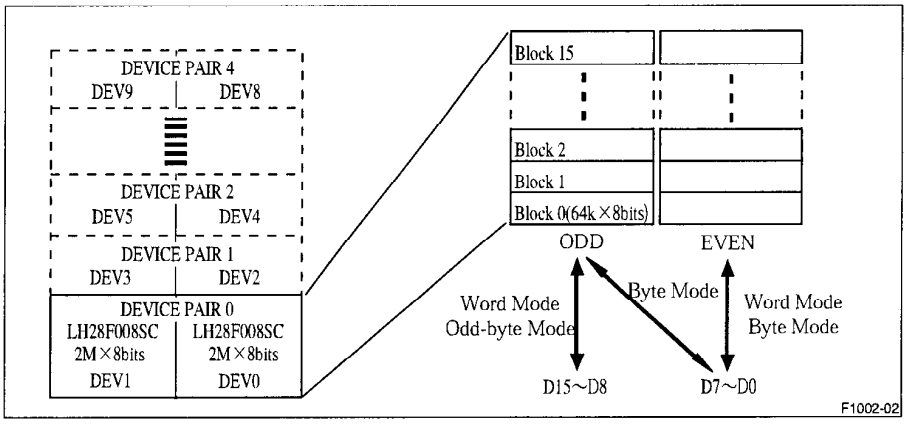
6. Functions

6. 1 Common Memory

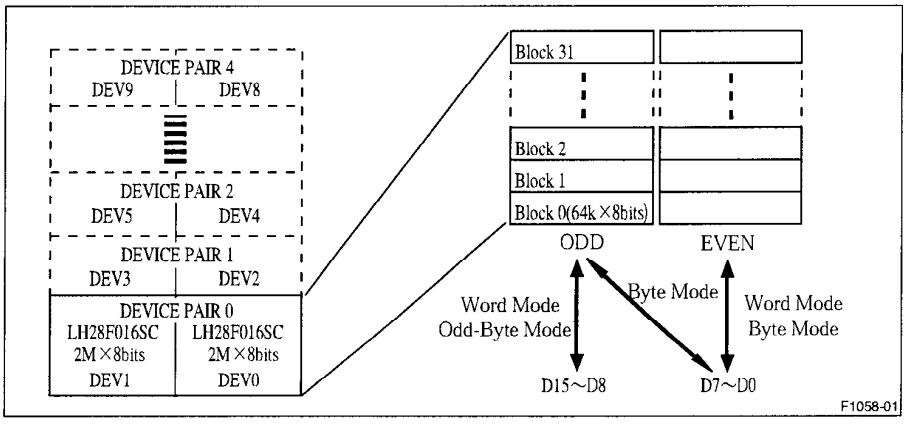
6. 1. 1 Common Memory Architecture

Figure 2 shows common memory architecture of ID242 series flash memory card. Device pair is consisted of two pieces of flash memory devices. Each device has individually erasable and lockable blocks. All blocks are divided into odd bytes and even bytes.

Each device pair and block is selected by address bits. Table 3 shows definitions of address bits.



(a) For 2, 4, 8, 10MB



(b) For 16MB, 20MB

Figure 2. Common Memory Architecture

Table 3. Address Difinitions

Address Pifinitions	2MB - 10MB	16MB , 20MB
Select Even / Odd byte in the byte access mode.	A0	
Select address in the block.	A16~A1	
Select a block.	A20~A17	A21~A17
Select a device pair.	A25~A21	A25~A22

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6. 1. 2 Erase

Erase is executed one block at a time. Erasable block size is 64K bytes in byte access mode and 128K bytes in word access mode.

6. 1. 3 Address Decoding

The higher address area of ID242 serics flash memory card which goes beyond common memory area is not decoded in common memory access. It means that the system will access to random memory address of the memory card even if system will try to access to the memory address which exceeds memory capacity of the card. Please do not access to the memory address which goes beyond memory capacity of the card.

As an enhanced function, the memory card enables to output invalid data (either of 0000h or FFFFh) when system will access to the memory address which exceeds memory capacity of the card. Please contact our sales & marketing support to find concrete way of setting.

6. 2 Attribute Memory

Figure 3 shows attribute memory map of ID242 series flash memory card. Attribute memory is contained within the Card Control Logic. Attribute memory contains the Card Information Structure (CIS) and Component Management Registers (CMRs). The CIS contains tuple information and is located at even byte addresses beginning with address 0000h (Please refer to section 7). The standard CIS of ID242 series flash memory card is hardwired and is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing support to find concrete way of setting. The CMRs are located at even byte addresses beginning with address 4000h (Please refer to section 9).

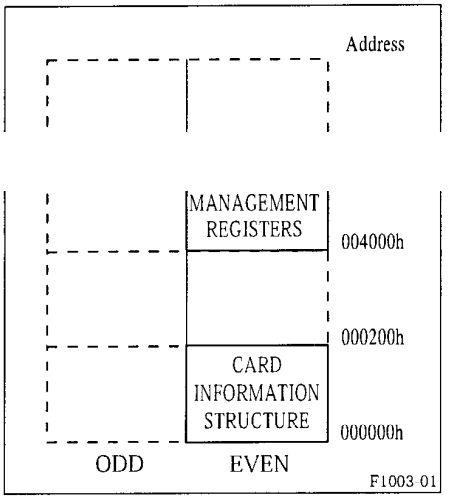

Figure 3. Attribute Memory Map

6.3 Function Table

6.3.1 Common Memory Access

Table 4. Common Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D_{15-8}	D_{7-0}
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	H	H	L	L	L	H	High-Z	Even
	H	H	L	H	L	H	High-Z	Odd
Word Read	H	L	L	X	L	H	Odd	Even
Odd Byte Read	H	L	H	X	L	H	Odd	High-Z
Byte Write	H	H	L	L	H	L	Don't care	Even
	H	H	L	H	H	L	Don't care	Odd
Word Write	H	L	L	X	H	L	Odd	Even
Odd Byte write	H	L	H	X	H	L	Odd	Don't care

6.3.2 Attribute Memory Access

Table 5. Attribute Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D_{15-8}	D_{7-0}
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	L	H	L	L	L	H	High-Z	Even
	L	H	L	H	L	H	High-Z	XXX
Word Read	L	L	L	X	L	H	XXX	Even
Odd Byte Read	L	L	H	X	L	H	XXX	High-Z
Byte Write	L	H	L	L	H	L	Don't care	Even
	L	H	L	H	H	L	Don't care	Don't care
Word Write	L	L	L	X	H	L	Don't care	Even
Odd Byte write	L	L	H	X	H	L	Don't care	Don't care

The standard CIS is for read only. Write operation is only for CMRs and CIS on EEPROM

7. Card Information Structure (CIS)

The CIS is contained within attribute memory (Please refer to section 6.2). Table 6 shows standard CIS tuples, but it is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing support to find concrete way of setting.

Table 6. Standard CIS

Address	Value	Description
00h	01h	Device Info (Common Memory)
02h	04h	Tuple Link
04h	57h	Flash Memory
06h	22h	Access Time 150ns
08h		Capacity
	06h	2MB
	0Eh	4MB
	1Eh	8MB
	26h	10MB
	3Eh	16MB
	4Eh	20MB
0Ah	FFh	End of Tuple
0Ch	1Ch	Device Info (Common Memory Other Conditions)
0Eh	05h	Tuple Link
10h	02h	Conditions 3Vcc
12h	57h	Flash Memory
14h	32h	Access Time 250ns
16h		Capacity
	06h	2MB
	0Eh	4MB
	1Eh	8MB
	26h	10MB
	3Eh	16MB
	4Eh	20MB
18h	FFh	End of Tuple
1Ah	17h	Device Info ID (Attribute Memory)
1Ch	04h	Tuple Link
1Eh	1Fh	ROM
20h	2Ah	Access Time 200ns
22h	01h	Capacity 2KB
24h	FFh	End of Tuple
26h	1Dh	Device Info ID (Attribute Memory)
28h	05h	Tuple Link
2Ah	02h	Conditions 3Vcc
2Ch	17h	ROM
2Eh	2Ah	Access Time 200ns
30h	01h	Capacity 2KB
32h	FFh	End of Tuple
34h	18h	JEDEC Code ID
36h	02h	Tuple Link
38h	89h	Manufacture Code
3Ah	A6h	Device Code
3Ch	00h	End of Tuple
3Eh	15h	Version Info Level 1
40h	23h	Tuple Link
42h	04h	Major Version
44h	01h	Minor Version

Address	Value	Description
46h	53h	S :Product Info
48h	48h	H
4Ah	41h	A
4Ch	52h	R
4Eh	50h	P
50h	00h	END TEXT
52h	49h	I
54h	44h	D
56h	32h	2
58h	34h	4
5Ah	53h	S
5Ch	52h	R
5Eh	20h	SPACE
60h	00h	END TEXT
62h	53h	S :Maker Info
64h	48h	H
66h	41h	A
68h	52h	R
6Ah	50h	P
6Ch	20h	SPACE
6Eh	43h	C
70h	4Fh	O
72h	52h	R
74h	50h	P
76h	4Fh	O
78h	52h	R
7Ah	41h	A
7Ch	54h	T
7Eh	49h	I
80h	4Fh	O
82h	4Eh	N
84h	00h	END TEXT
86h	FFh	End of Tuple
88h	1Ah	Configuration Info
8Ah	05h	Tuple Link
8Ch	01h	2 Bytes Field
8Eh	06h	Last Index of Configuration Table
90h	00h	CMRs Base Adress(LSB)
92h	40h	CMRs Base Adress(MSB)
94h	0Bh	CMR Mask
96h	00h	Null
98h	1Bh	Configuration Table Entry 1
9Ah	0Fh	Tuple Link
9Ch	01h	Index
9Eh	02h	Vcc & Vpp
A0h	79h	Parameter Selection
A2h	55h	Vcc Voltage 5V

Table 8. Standard CIS (Continued)

Address	Value	Description
A4h	0Ch	Icc Static 1.2mA
A6h	06h	Icc Average 100mA
A8h	06h	Icc Peak 100mA
AAh	23h	Icc Powerdown 50mA
ACh	79h	Parameter Selection
AEh	D5h	Vpp Voltage 5V
B0h	7Dh	NC OK
B2h	1Bh	Ipp Static 150mA
B4h	75h	Ipp Average 80mA
B6h	75h	Ipp Peak 80mA
B8h	52h	Ipp Powerdown 50mA
BAh	1Bh	Configuration Table Entry 2
BCh	0Fh	Tuple Link
BEh	02h	Index
C0h	02h	Vcc & Vpp
C2h	79h	Parameter Selection
C4h	55h	Vcc Voltage 5V
C6h	0Ch	Icc Static 1.2mA
C8h	06h	Icc Average 100mA
CAh	06h	Icc Peak 100mA
CCh	23h	Icc Powerdown 50mA
CEh	79h	Parameter Selection
D0h	8Eh	Vpp Voltage 12V
D2h	7Dh	NC OK
D4h	1Bh	Ipp Static 150mA
D6h	35h	Ipp Average 30mA
D8h	35h	Ipp Peak 30mA
DAh	52h	Ipp Powerdown 50mA
DCh	1Bh	Configuration Table Entry 3
DEh	11h	Tuple Link
E0h	03h	Index
E2h	02h	Vcc & Vpp
E4h	79h	Parameter Selection
E6h	B5h	Vcc Voltage 3.3V
E8h	1Eh	
EAh	0Ch	Icc Static 1.2mA
ECh	7Dh	Icc Average 90mA
EEh	7Dh	Icc Peak 90mA
F0h	1Bh	Icc Powerdown 150mA
F2h	79h	Parameter Selection
F4h	B5h	Vpp Voltage 3.3V
F6h	9Eh	
FAh	1Bh	Ipp Static 150mA
FCh	75h	Ipp Average 80mA
FEh	75h	Ipp Peak 80mA
100h	52h	Ipp Powerdown 50mA
102h	1Bh	Configuration Table Entry 4

Address	Value	Description
104h	10h	Tuple Link
106h	04h	Index
108h	02h	Vcc & Vpp
10Ah	79h	Parameter Selection
10Ch	B5h	Vcc Voltage 3.3V
10Eh	1Eh	
110h	0Ch	Icc Static 1.2mA
112h	7Dh	Icc Average 90mA
114h	7Dh	Icc Peak 90mA
116h	1Bh	Icc Powerdown 150mA
118h	79h	Parameter Selection
11Ah	8Eh	Vpp Voltage 12V
11Ch	7Dh	NC OK
11Eh	1Bh	Ipp Static 150mA
120h	35h	Ipp Average 30mA
122h	35h	Ipp Peak 30mA
124h	52h	Ipp Powerdown 50mA
126h	00h	Null
128h	00h	Null
12Ah	1Eh	Device Geometry
12Ch	06h	Tuple Link
12Eh	02h	Bus: 2bytes
130h	11h	Erase Block: 64Kbytes
132h	01h	Read size: 1byte
134h	01h	Write size: 1byte
136h	01h	Partation: 1block
138h	01h	Non-interleaved
13Ah	20h	Manufacturer ID
13Ch	04h	Tuple Link
13Eh	B0h	Manufacturer Code
140h	00h	
142h		Manufacturer Info: 06h 2MB 07h 4MB 09h 8MB 0Ah 10MB 0Dh 16MB 0Eh 20MB
144h	33h	Manufacturer Info: DVO
146h	21h	Function Identification
148h	02h	Tuple Link
14Ah	01h	Function: MEMORY
14Ch	00h	System Init: None
14Eh	FFh	End of CIS

8. Card Control

8. 1 Reset

The card is in initial state directly after power-up. But we recommend to do reset operation after power-up to make sure to initialize the card.

During block erase, byte write, or lock-bit configuration modes, an active RESET will abort the operation. RDY/BSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET goes to logic-Low (V_{IL}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET to the card during a system reset. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs.

For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data. Sharp's ID242 Series Flash Memory Card allows proper card reset following a system reset through the use of the RESET input.

8. 2 Status Register

Each flash memory device in the card has status register. The status register may be read to determine when a write, block erase, or lock-bits configuration is complete, and whether that operation completed successfully (please refer to Table 10). It may be read at any time by writing the Read Status Register command (70h, 7070h) into the CUI. In word access mode, the status register data of even byte devices are output to D7~0,and the status register data of odd byte devices are output to D15~8.

8. 3 Write Protect Switch

The ID242 Series Flash Memory Card has a write protect switch on the back of the card. When the switch is in the write protect position, the card blocks all writes to the common and attribute memory without Card Management Registers region (see Figure 5).

8. 4 Read Identifier Codes / Lock bits Information

Manufacture Code and Device Code are contained within each flash memory device in the memory card. The identifier code operation is initiated by writing the Read Identifier Codes command (90h, 9090h) into the CUI of each memory device. The specific address of each device is necessary to be selected to read these codes (Table 8).

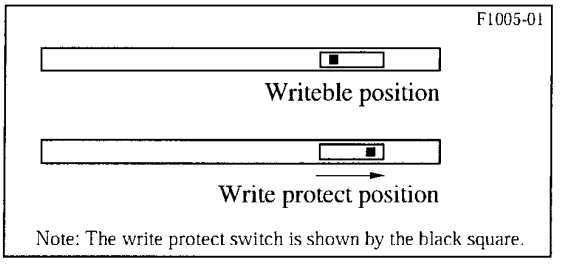

Figure 4. Write Protect Switch

Table 7. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	RFU

SR.7 =WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy SR.6 =ERASE-SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed SR.5 =ERASE AND CLEAR LOCK-BITS STATUS 1 = Error In Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits SR.4 =BYTE WRITE AND SET LOCK-BIT STATUS 1 = Error in Byte Write or Set Block/Master Lock-Bit 0 = Successful Byte Write or Set Block/Master Lock-Bit SR.3 =VPP STATUS 1 = VPP Low Detect, Operation Abort 0 = VPP OK SR.2 =BYTE WRITE SUSPEND STATUS 1 = Byte Write Suspended 0 = Byte Write in Progress/Completed SR.1 =DEVICE PROTECT STATUS 1 = Master Lock-bit,Block Lock-bit and/or RP# Lock Detected, Operation Abort 0 = Unlock SR.0 =Reserved for Future Enhancements	Notes: Chech RDY/BSY# or SR.7 to determine block erase, word/byte write, or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0". If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entred. SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Word/Byte Write, Set Block/Master Lock-bit, or Clear Lock-bits command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP}=V_{PPH1/2/3}$. SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after Block Erase, Word/Byte Write, or Lock-bit configuration command sequences. If informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# is not 12V. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes commnad indicates master and block lock-bit status. SR.0 is reserved for future use and should be masked out when polling the status register.

Table 8. Identifier Codes / Lock bits

	Select Device-pair A25-A21	Address in Device A20-A1	Even/Odd A0	Data Output D7-D0	
				2MB - 10MB	16MB , 20MB
Manufacture Identifier Code	DPA	00000h	0:Even 1:Odd	89h	89h
Device Identifier Code	DPA	00001h	0:Even 1:Odd	A6h	AAh
Block Lock Configuration	DPA	X0002h (X: Select Block)	0:Even 1:Odd	BLKD D0: 0=Unlock, 1=Lock D7-D1: Reserved	
Master Lock Configuration	DPA	00003h	0:Even 1:Odd	MLKD D0: 0=Unlock, 1=Lock D7-D1: Reserved	

NOTE: A0 is ignored in word access mode, and D15-D8 outputs the Odd byte data. T1052-01

DPA: Address as select device pair
BLKD: Block Lock Configuration Data
MLKD: Master Lock Configuration Data

9. Component Management Registers (CMR)

Component Management Registers (CMR) are mapped at even byte locations beginning at address 4000h in attribute memory.

9. 1 Configuration Option Register (Address:4000h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4000h	SRESET	Reserved						
SRESET: 1=Reset State 0=End Reset Cycle								

9. 2 Card Configuration Register (Address:4002h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4002h	Reserved					PWDN	Reserved	
PWDN: 1=Power-Down Device pairs that apointed by Sleep Control Register(4118h-411Ah) are in Power-Down. 0=Power-Up								

9. 3 Socket and Copy Register (Address:4006h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4006h	Reserved	Copy No.			Soket No.			
Soket No.: Socket Number Copy No.: Copy Number The card may use to distinguish between similar cards installed in a system.								

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9. 4 Card Status Register (Address:4100h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4100h	ADM	ADS	SRESET	CMWP	PWDN	CISWP	WP	RDY/BSY

ADM: ORed value of the Ready/Busy Mask Register.
1 = Any device is masked. 0 = All Devices are not Masked.
ADS: ORed value of the Sleep Control Register.
1 = Any device-pair is Controled power-down by bit.2 of the Card Configuration Register.
SRESET: Reflects the bit.7 of the Configuration Option Register.
CMWP: Reflects the bit.1 of the Write Protection Register.
PWDN: Reflects the bit.2 of the Card Configuration Register.
CISWP: Reflects the bit.0 of the Write Protection Register.
WP: Indicates the Write Protect Switch status.
1 = Write Protect Switch: ON 1 = Write Protect Switch: OFF
RDY/BSY: Reflects the Ready/Busy Status Register.
1 = All devices are READY. 0 = Any device is BUSY.

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9. 5 Write Protection Register (Address:4104h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4104h	Reserved					BLKEN	CMWP	CISWP

BLKEN: Block Locking Enable
1 = Enable Block Locking 0 = All Blocks Unlocked
CMWP: Common Memory Write Protect
1 = Common Memory without CIS region in Write Protect Status
CISWP: Common Memory CIS Write Protect
1 = Common Memory CIS in Write Protect Status

NOTE: ID242 series ignores BLKEN bit. Block Locking is always enable.

9. 6 Sleep Control Register (Address:4118h~411Ah)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
411Ah	Reserved							
4118h	Reserved		DEV10/11	DEV8/9	DEV6/7	DEV4/5	DEV2/3	DEV0/1

1= Select sleep mode device-pair
If set to "1", the corresponding device-pairs are putted into deep power-down mode by PWDN bit of Configuration Status Register.

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9. 7 Ready/Busy Mask Register (Address:4120h~4122h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4122h	Reserved				DEV11	DEV10	DEV9	DEV8
4120h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1 =Mask the Rdy/Bsy#
The corresponding device's Rdy/Bsy# signals to set bit are ignored for card's RDY/BSY# output.

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9. 8 Ready/Busy Status Register (Address:4130h~4132h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4132h	Reserved				DEV11	DEV10	DEV9	DEV8
4130h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1=READY 0=BUSY
Each bit indicates the corresponding device's Rdy/Bsy# signal.

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9. 9 Ready/Busy Mode Register (Address:4140h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4140h	Reserved						RACK	MODE

RACK: Ready Acknowledge Bit
Must clear this bit after receiving ready status to prepare for next device's ready transition.
MODE: RDY/BSY# Mode
1 = High-Performance Mode 0 = PCMCIA Mode

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10. Command Definitions

Device operations are determined by writing specific commands to the Command User Interface. Table 9 defines the commands.

Table 9. Command Definitions

Command	Note	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array / Reset		Write	DA	FFh (FFFFh)	-	-	-
Read Identifier Codes	1	Write	DA	90h (9090h)	Read	IA	ID
Read Status Register	2	Write	DA	70h (7070h)	Read	DA	SRD
Clear Status Register		Write	DA	50h (5050h)	-	-	-
Word/Byte Write	3	Write	WA	40h (4040h) or 10h (1010h)	Read	WA	WD
Block Erase	3	Write	BA	20h (2020h)	Write	BA	D0h (D0D0h)
Block Erase and Word/Byte Write Suspend	3	Write	DA	B0h (B0B0h)	-	-	-
Block Erase and Word/Byte Write Resume	3	Write	DA	D0h (D0D0h)	-	-	-
Set Block Lock-Bit		Write	BA	60h (6060h)	Write	BA	01h (0101h)
Set Master Lock-Bit	4	Write	DA	60h (6060h)	Write	DA	F1h (F1F1h)
Clear Block Lock-Bit		Write	DA	60h (6060h)	Write	DA	D0h (D0D0h)

Address

IA =Identifier code Address

WA =Write Address

BA =Block Address

DA =Device Address

Data

ID =Identifier Codes

WD =Write Data

SRD =Data from Status Register

Note:

1. Following the Read Identifier Codes command, read operations access manufacture, device, block lock, and master lock codes.
2. Status Register may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully.
3. If the block is locked, block erase or write operations are desabled.
4. This command is not available.

11. Electrical Specifications

11. 1 Absolute Maximum Ratings

PARAMETER	NOTE	SYMBOL	RATING	UNIT
Supply Voltage	2	V_{CC}	-0.3 to 6.0	V
Program Voltage	2	V_{PP}	-2.0 to 14.0	V
Input Voltage	2	V_{IN}	-0.3 to Vcc+0.3(Max:6.0)	V
Operating Temperature	1	T_{OPR}	0 to 60	℃
Storage Temperature		T_{STG}	-20 to 65	℃

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. During transitions, this level may undershoot to -2.0v for periods <20ns or overshoot to Vcc+2.0v for periods <20ns.

11. 2 Recommended Operating Conditions

PARAMETER	NOTE	SYMBOL	MIN	MAX	UNIT
Supply Voltage		V_{CC1}	3.0	3.6	V
		V_{CC2}	4.75	5.25	V
		V_{CC3}	4.5	5.5	V
Program Voltage		V_{PP1}	3.0	3.6	V
		V_{PP2}	4.5	5.5	V
		V_{PP3}	11.4	12.6	V
Operating Temperature		T_{OPR}	0	60	℃

11. 3 Capacitance

Ta=25℃, f=1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	-	15	-	pF	V_{IN}=0.0V
Input/Output Capacitance	C_{IO}	-	25	-	pF	V_{OUT}=0.0V

11. 4 AC Input/Output Test Conditions

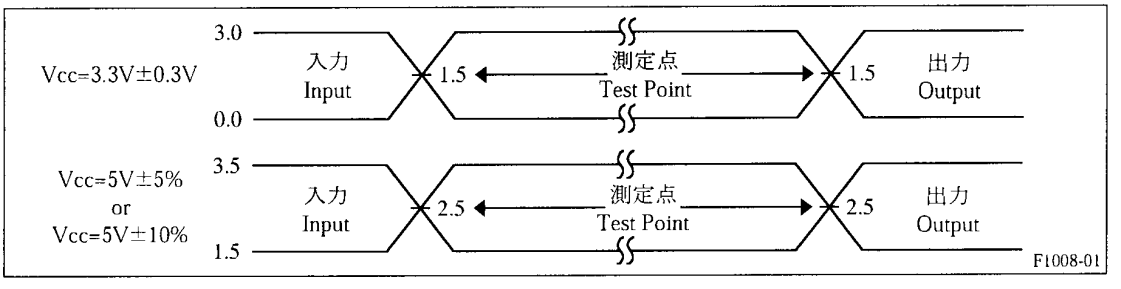

Figure 5. Transient Input/Output Reference Waveform

Figure 8 shows Input/Output level and test level for AC test. Input rise and fall times (10% to 90%) < 10ns.

12. DC Characteristics

(Ta = 0 to 60°C)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V± 0.3V		Vcc=5V± 5% Vcc=5V± 10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
Input Low Voltage	V_{IL}	1			0.3Vcc		1.5	V	
Input High Voltage	V_{IH}	1		0.7Vcc		3.5		V	
Input Low Current	$-I_{IL1}$	2			± 2.0		± 2.0	μA	V_I = 0V
	$-I_{IL2}$	3		2.0	30.0	8.0	60.0	μA	V_I = 0V
Input High Current	I_{IH1}	3			± 2.0		± 2.0	μA	V_I = Vcc
	I_{IH2}	2		2.0	30.0	8.0	60.0	μA	V_I = Vcc
Output Low Voltage	V_{OL1}	4,5			-		0.4	V	I_{OL} = 6mA
					0.4		-	V	I_{OL} = 3mA
Output High Voltage	V_{OH1}	4		-		4.0		V	I_{OH} = -3mA
				Vcc-0.5		-		V	I_{OH} = -1.5mA
	V_{OH2}	5		-		4.0		V	I_{OH} = -6mA
				Vcc-0.5		-		V	I_{OH} = -3mA
Vcc Stand-by Current	I_{CCS}	6	2MB		240		240	μA	CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			4MB		450		450	μA	
			8MB		850		850	μA	
			10MB		1050		1050	μA	
			16MB		850		850	μA	
			20MB		1050		1050	μA	
Vcc Deep Power-Down Current	I_{CCD}	6	2MB		45		75	μA	RESET=Vcc CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			4MB		70		110	μA	
			8MB		120		170	μA	
			10MB		145		205	μA	
			16MB		185		205	μA	
			20MB		225		250	μA	
Vcc Read Current	I_{CCR}	6,8			90		100	mA	CE_1#,CE_2#=GND I_{OUT}=0mA
Vcc Word Write or Set Lock-Bit Current	I_{CCW}	6,9			35		-	mA	V_{PP}=3.3V± 0.3V
					35		75	mA	V_{PP}=5.0V± 10%
					25		65	mA	V_{PP}=12.0V± 5%
Vcc Block Erase or Clear Lock-Bit Current	I_{CCE}	6,9			35		-	mA	V_{PP}=3.3V± 0.3V
					35		65	mA	V_{PP}=5.0V± 10%
					25		55	mA	V_{PP}=12.0V± 5%
VccWord Write or Block Erase Suspend Current	I_{CCWS} I_{CCES}	6			13		21	mA	
Vcc Lockout Voltage	V_{LKO}			2.0		2.0		V	

(Continue to next page)

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DC Characteristics (Continued) (Ta = 0 to 60℃)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V± 0.3V		Vcc=5V± 5% Vcc=5V± 10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
V_{PP} Stand-by or Read Current	I_{PPS} I_{PPR}	6	2MB		± 30		± 30	μA	$V_{PP} \leqq V_{CC}$
			4MB		± 60		± 60	μA	
			8MB		± 120		± 120	μA	
			10MB		± 150		± 150	μA	
			16MB		± 120		± 120	μA	
			20MB		± 150		± 150	μA	
			2MB		0.4		0.4	mA	$V_{PP}>V_{CC}$
			4MB		0.8		0.8	mA	
			8MB		1.6		1.6	mA	
			10MB		2.0		2.0	mA	
			16MB		1.6		1.6	mA	
			20MB		2.0		2.0	mA	
V_{PP} Deep Power-Down Current	I_{PPD}	6	2MB		10		10	μA	
			4MB		20		20	μA	
			8MB		40		40	μA	
			10MB		50		50	μA	
			16MB		40		40	μA	
			20MB		50		50	μA	
V_{PP} Word Write or Set Lock-Bit Current	I_{PPW}	6,9			80		-	mA	V_{PP}=3.3V± 0.3V
					80		80	mA	V_{PP}=5.0V± 10%
					32		32	mA	V_{PP}=12.0V± 5%
V_{PP} Block Erase or Clear Lock-Bit Current	I_{PPE}	6,9			40		-	mA	V_{PP}=3.3V± 0.3V
					40		40	mA	V_{PP}=5.0V± 10%
					32		32	mA	V_{PP}=12.0V± 5%
V_{PP} Word Write or Block Erase Suspend Current	I_{PPWS} I_{PPES}	6	2MB		400		400	μA	$V_{PP} \leqq V_{CC}$
			4MB		430		430	μA	
			8MB		500		500	μA	
			10MB		530		530	μA	
			16MB		500		500	μA	
			20MB		530		530	μA	
			2MB		0.4		0.4	mA	
			10MB		2.0		2.0	mA	$V_{PP}>V_{CC}$
			16MB		1.6		1.6	mA	
			20MB		2.0		2.0	mA	
V_{PP} Lockout Voltage	V_{PPLK}	7,9			1.5		1.5	V	

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NOTE:

1. These parameters are applied to all input pins and all i/put/output pins in input mode.
2. These parameters are applied to A_0~A_{25} and D_0~D_{15} in input mode.
3. These parameters are applied to CE_1#,CE_2#,WE#,OE#,REG# and RESET.
4. These parameters are applied to RDY/BSY#.
5. These parameters are applied to D_0~D_{15} in output mode.
6. All currents are in RMS unless otherwise notes.
7. Block erase, word/byte write, and lock-bit configurations are inhibited when $V_{PP} \leqq V_{PPLK}$, and guaranteed in the V_{PP} Voltage is V_{PP1}, V_{PP2} or V_{PP3}.
8. Automatic Power Savings(APS) reduces typical I_{CCR} to 30mA at Vcc=5V and 20mA at Vcc=3.3V in static operation.
9. Sampled.

13. AC Characteristics

Testing Conditions :

1) Input Pulse Level : 1.5 to 3.5V (@Vcc=5V±5%,Vcc=5V±10%)
   0 to 3.0V (@Vcc=3.3±0.3V)
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 2.5V (@Vcc=5V±5%,Vcc=5V±10%)
   1.5V (@Vcc=3.3V±0.3V)
4) Output Load : 1TTL+100pF (@Vcc=5V±5%,Vcc=5V±10%)
   (including scope and jig capacitance) 1TTL+50pF (@Vcc=3.3V±0.3V)

13. 1 Common Memory Read Operations

(Ta = 0 to 60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 5%		Vcc=5V± 10%		Unit
	IEEE	JEIDA/ PCMCIA	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	250	-	150	-	160	-	ns
Address Access Time	t_{AVQV}	t_a(A)	-	250	-	150	-	160	
CE# Access Time	t_{ELQV}	t_a(CE)	-	250	-	150	-	160	
OE# Access Time	t_{GLQV}	t_a(OE)	-	125	-	75	-	80	
Output Disable Time from CE1#,CE2# *	t_{EHQZ}	t_{dis}(CE)	-	100	-	75	-	80	
Output Disable Time from OE# *	t_{GHQZ}	t_{dis}(OE)	-	100	-	75	-	80	
Output Enable Time from CE1#,CE2#	t_{ELQNZ}	t_{en}(CE)	5	-	5	-	5	-	
Output Enable Time from OE#	t_{GLQNZ}	t_{en}(OE)	5	-	5	-	5	-	
Data Valid Time from Address Change		t_v(A)	0	-	0	-	0	-	

*:Time until output becomes floating. (The output voltage is not defined.)

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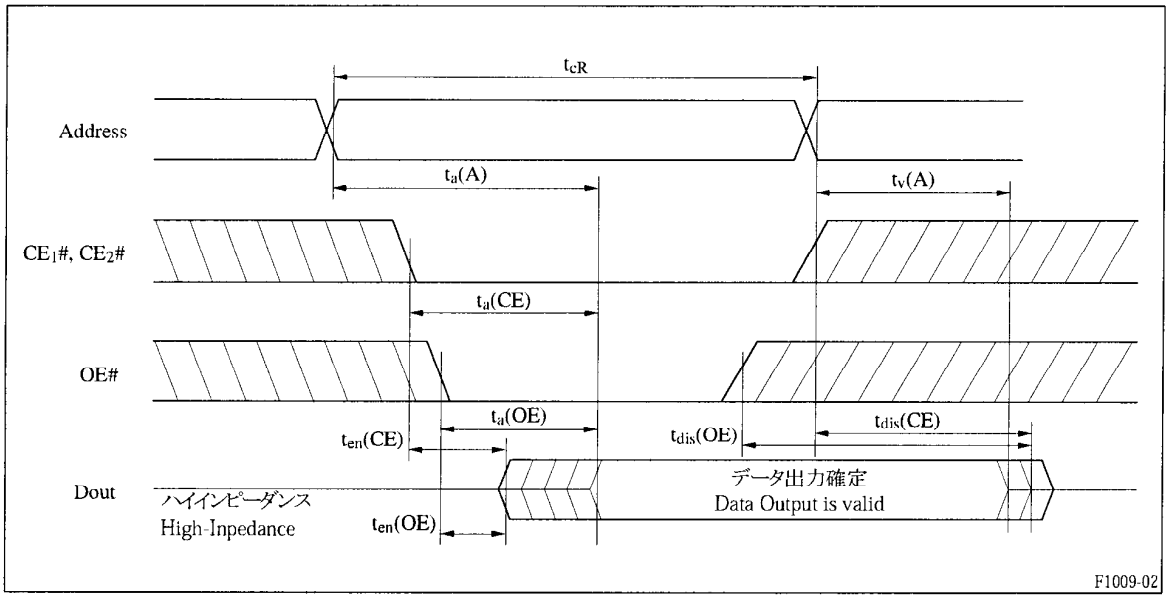

Figure 6. AC Waveforms for Read Operations

Note) 1. WE# = "HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, ta (A), ta (CE) or ta (OE) have concluded.

13. 2 Command Write Operations : Common Memory

13. 2. 1 WE# Controlled Write Operations

(Vcc=3.3V± 0.3V,Ta=0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=3.3V± 0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		30	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		80	-	ns
Data Hold Time	t_{WHDX}	t_{h}(D)		30	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_{h}(OE-WE)		120	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		180	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		180	-	ns
Write Pulse Width	t_{WLWH}	t_{w}(WE)		150	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	ns
RESET Recovery Time	t_{PHWL}			1	-	μs
V_{PP} Setup Time	t_{VPWH}			180	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=3.3V± 0.3V	15	-	μs
			V_{PP}=5V± 10%	8.2	-	μs
			V_{PP}=12V± 5%	6.7	-	μs
Block Erase Time	t_{WHQV2}		V_{PP}=3.3V± 0.3V	1.5	-	s
			V_{PP}=5V± 10%	1.0	-	s
			V_{PP}=12V± 5%	0.8	-	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=3.3V± 0.3V	18	-	μs
			V_{PP}=5V± 10%	11.2	-	μs
			V_{PP}=12V± 5%	9.7	-	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=3.3V± 0.3%	1.5	-	s
			V_{PP}=5V± 10%	1.0	-	s
			V_{PP}=12V± 5%	0.8	-	s
Word / byte Suspend Latency Time to Read	t_{WHRH1}		V_{PP}=3.3V± 0.3%	-	10.0	μs
			V_{PP}=5V± 10%	-	9.3	μs
			V_{PP}=12V± 5%	-	10.4	μs
Erase Suspend Latency Time to Read	t_{WHRH2}		V_{PP}=3.3V± 0.3%	-	21.1	μs
			V_{PP}=5V± 10%	-	17.2	μs
			V_{PP}=12V± 5%	-	17.2	μs

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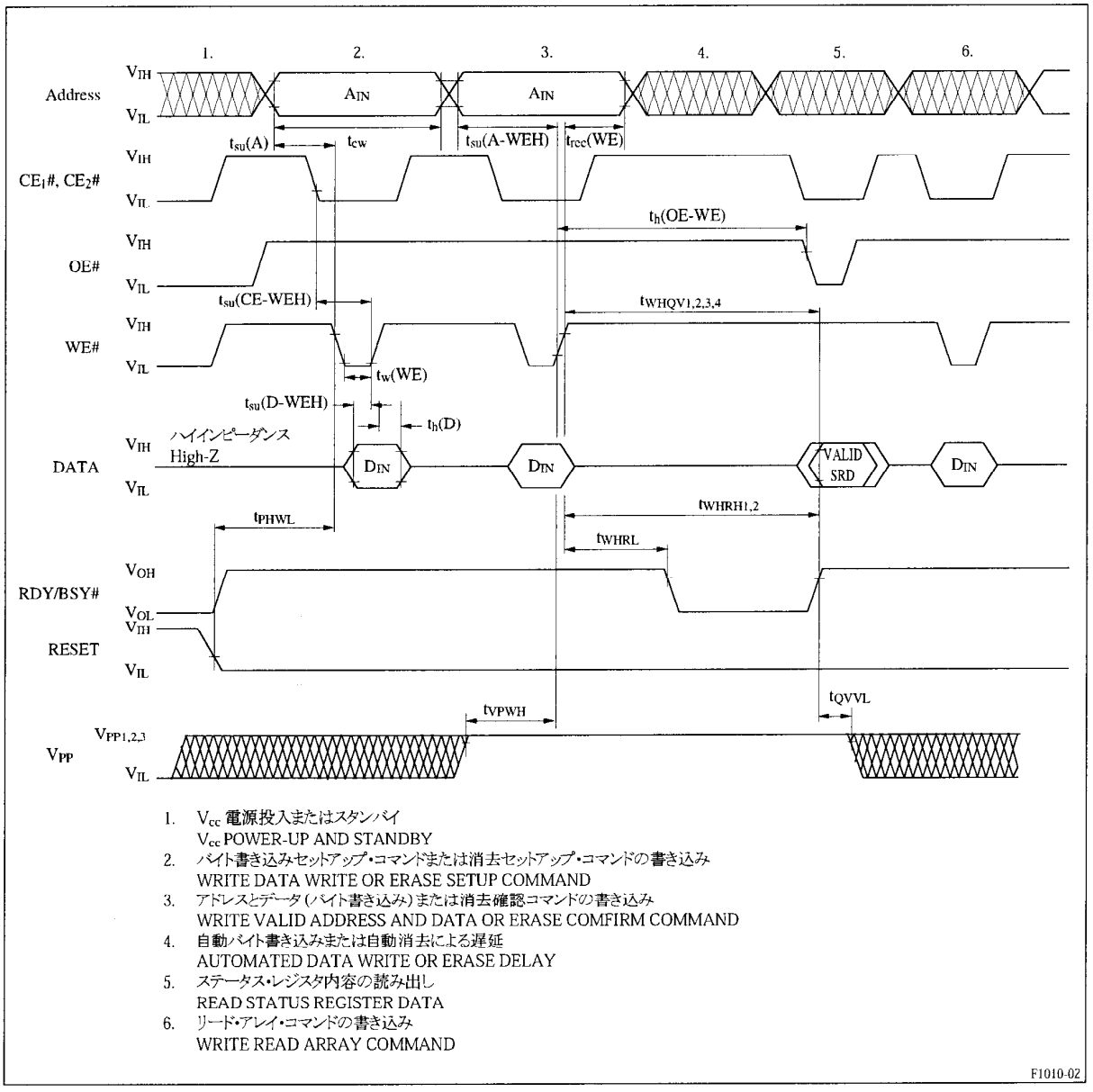
(Vcc=5V± 5%, Vcc=5V± 10%,Ta = 0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=5V± 5%		Vcc=5V± 10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		20	-	20	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		50	-	50	-	ns
Data Hold Time	t_{WHDX}	t_h(D)		20	-	20	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_h(OE-WE)		80	-	80	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		100	-	100	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		100	-	100	-	ns
Write Pulse Width	t_{WLWH}	t_w(WE)		80	-	80	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHWL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPWH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=5V± 10%	6.5	-	6.5	-	μs
			V_{PP}=12V± 5%	4.8	-	4.8	-	μs
Block Erase Time	t_{WHQV2}		V_{PP}=5V± 10%	0.9	-	0.9	-	s
			V_{PP}=12V± 5%	0.3	-	0.3	-	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=5V± 10%	9.5	-	9.5	-	μs
			V_{PP}=12V± 5%	7.8	-	7.8	-	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=5V± 10%	0.9	-	0.9	-	s
			V_{PP}=12V± 5%	0.3	-	0.3	-	s
Word / byte Suspend Latency Time to Read	t_{WHRH1}		V_{PP}=5V± 10%	-	7.0	-	7.0	μs
			V_{PP}=12V± 5%	-	7.5	-	7.5	μs
Erase Suspend Latency Time to Read	t_{WHRH2}		V_{PP}=5V± 10%	-	13.1	-	13.1	μs
			V_{PP}=12V± 5%	-	12.6	-	12.6	μs

T1049-01



1. V_{CC} 電源投入またはスタンバイ
   V_{CC} POWER-UP AND STANDBY
2. バイト書き込みセットアップ・コマンドまたは消去セットアップ・コマンドの書き込み
   WRITE DATA WRITE OR ERASE SETUP COMMAND
3. アドレスとデータ(バイト書き込み)または消去確認コマンドの書き込み
   WRITE VALID ADDRESS AND DATA OR ERASE COMFIRM COMMAND
4. 自動バイト書き込みまたは自動消去による遅延
   AUTOMATED DATA WRITE OR ERASE DELAY
5. ステータス・レジスタ内容の読み出し
   READ STATUS REGISTER DATA
6. リード・アレイ・コマンドの書き込み
   WRITE READ ARRAY COMMAND

F1010-02

Figure 7. AC Waveforms for Write Operations (WE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 2. 2 CE# Controlled Write Operations

(Vcc=3.3V± 0.3V, Ta = 0 to 60℃)

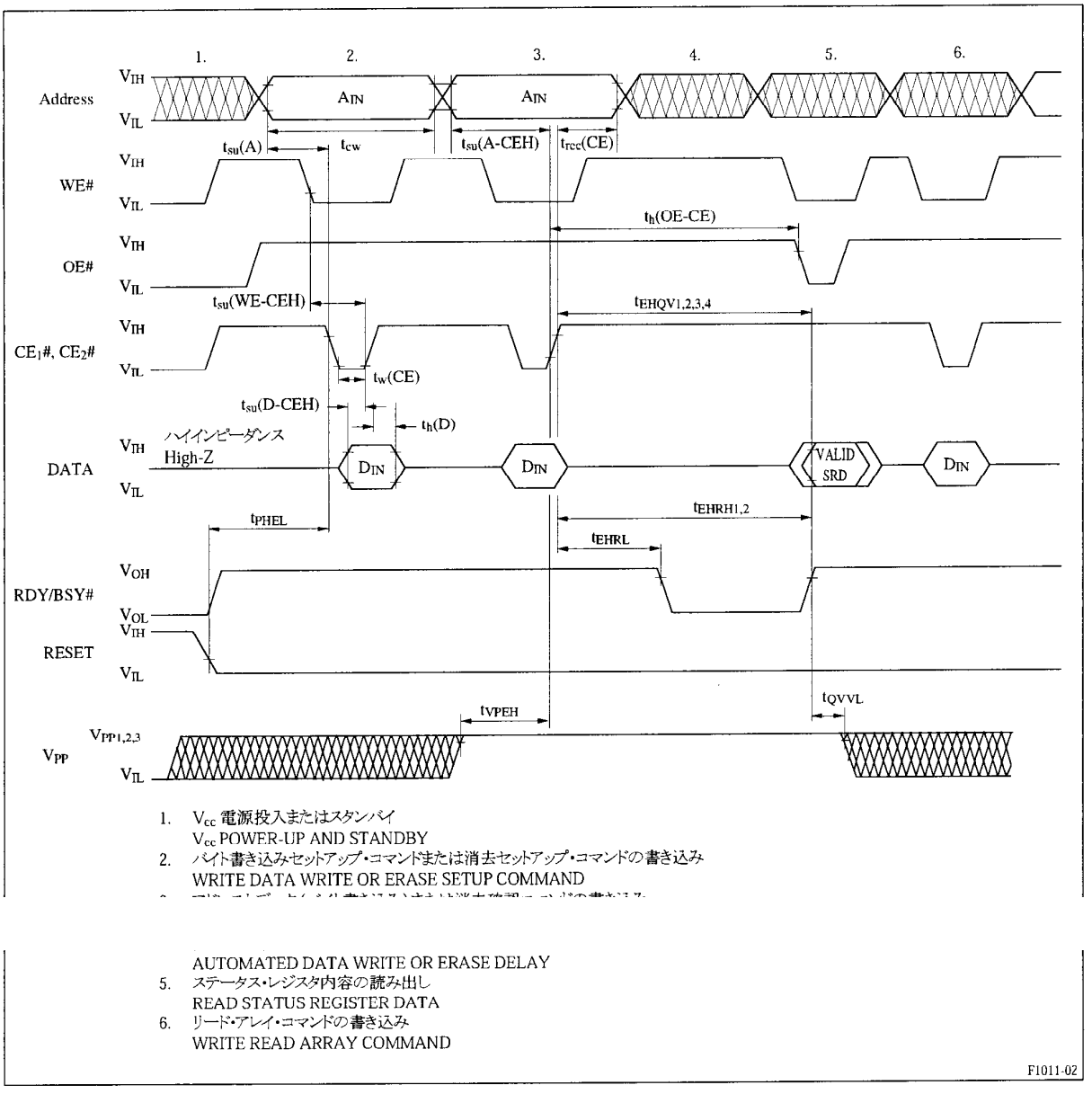
PARAMETER	SYMBOL		CONDITION	Vcc=3.3V± 0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		30	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		60	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		30	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		120	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		180	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		180	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		150	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	μs
V_{PP} Setup Time	t_{VPEH}			180	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=3.3V± 0.3V	15	-	μs
			V_{PP}=5V± 10%	8.2	-	μs
			V_{PP}=12V± 5%	6.7	-	μs
Block Erase Time	t_{EHQV2}		V_{PP}=3.3V± 0.3V	1.5	-	s
			V_{PP}=5V± 10%	1.0	-	s
			V_{PP}=12V± 5%	0.8	-	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=3.3V± 0.3V	18	-	μs
			V_{PP}=5V± 10%	11.2	-	μs
			V_{PP}=12V± 5%	9.7	-	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=3.3V± 0.3V	1.5	-	s
			V_{PP}=5V± 10%	1.0	-	s
			V_{PP}=12V± 5%	0.8	-	s
Word / byte Suspend Latency Time to Read	t_{EHRH1}		V_{PP}=3.3V± 0.3V	-	10.0	μs
			V_{PP}=5V± 10%	-	9.3	μs
			V_{PP}=12V± 5%	-	10.4	μs
Erase Suspend Latency Time to Read	t_{EHRH2}		V_{PP}=3.3V± 0.3V	-	21.1	μs
			V_{PP}=5V± 10%	-	17.2	μs
			V_{PP}=12V± 5%	-	17.2	μs

T1045-01

(Vcc=5V± 5%, Vcc=5V± 10%, Ta=0 to 60℃

PARAMETER	SYMBOL		CONDITION	Vcc=5V± 5%		Vcc=5V± 10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		20	-	20	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		50	-	50	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		20	-	20	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		80	-	80	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		100	-	100	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		100	-	100	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		80	-	80	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPEH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=5V± 10%	6.5	-	6.5	-	μs
			V_{PP}=12V± 5%	4.8	-	4.8	-	μs
Block Erase Time	t_{EHQV2}		V_{PP}=5V± 10%	0.9	-	0.9	-	s
			V_{PP}=12V± 5%	0.3	-	0.3	-	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=5V± 10%	9.5	-	9.5	-	μs
			V_{PP}=12V± 5%	7.8	-	7.8	-	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=5V± 10%	0.9	-	0.9	-	s
			V_{PP}=12V± 5%	0.3	-	0.3	-	s
Word / Byte Suspend Latency Time to Read	t_{EHRH1}		V_{PP}=5V± 10%	-	7.0	-	7.0	μs
			V_{PP}=12V± 5%	-	7.5	-	7.5	μs
Erase Suspend Latency Time to Read	t_{EHRH2}		V_{PP}=5V± 10%	-	13.1	-	13.1	μs
			V_{PP}=12V± 5%	-	12.6	-	12.6	μs

T1046-01



1. V_{CC} 電源投入またはスタンバイ
   V_{CC} POWER-UP AND STANDBY
2. バイト書き込みセットアップ・コマンドまたは消去セットアップ・コマンドの書き込み
   WRITE DATA WRITE OR ERASE SETUP COMMAND

   AUTOMATED DATA WRITE OR ERASE DELAY
5. ステータス・レジスタ内容の読み出し
   READ STATUS REGISTER DATA
6. リード・アレイ・コマンドの書き込み
   WRITE READ ARRAY COMMAND

F1011-02

Figure 8. AC Waveforms for Write Operations (CE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 3 Attribute Memory Read Operation

(Ta=0～60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 10%		Unit
	IEEE	JEIDA/ PCMCIA	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	600	—	300	—	ns
Address Access Time	t_{AVQV}	t_a(A)	—	600	—	300	
CE# Access Time	t_{ELQV}	t_a(CE)	—	600	—	300	
OE# Access Time	t_{GLQV}	t_a(OE)	—	300	—	150	
Output Disable Time from CE1#,CE2# *	t_{EHQZ}	t_{dis}(CE)	—	150	—	100	
Output Disable Time from CE#	t_{GHQZ}	t_{dis}(OE)	—	150	—	100	
Output Disable Time from CE1#,CE2#	t_{ELQNZ}	t_{en}(CE)	5	—	5	—	
Output Disable Time from OE#	t_{GLQNZ}	t_{en}(OE)	5	—	5	—	
Data Valid Time from Address Change		t_v(A)	0	—	0	—	

*: Time until becomes floating. (The output voltage is not defined)

T1056-01

Note) When the CIS constructed by EEPROM, this card requires 5V voltage for Vcc.

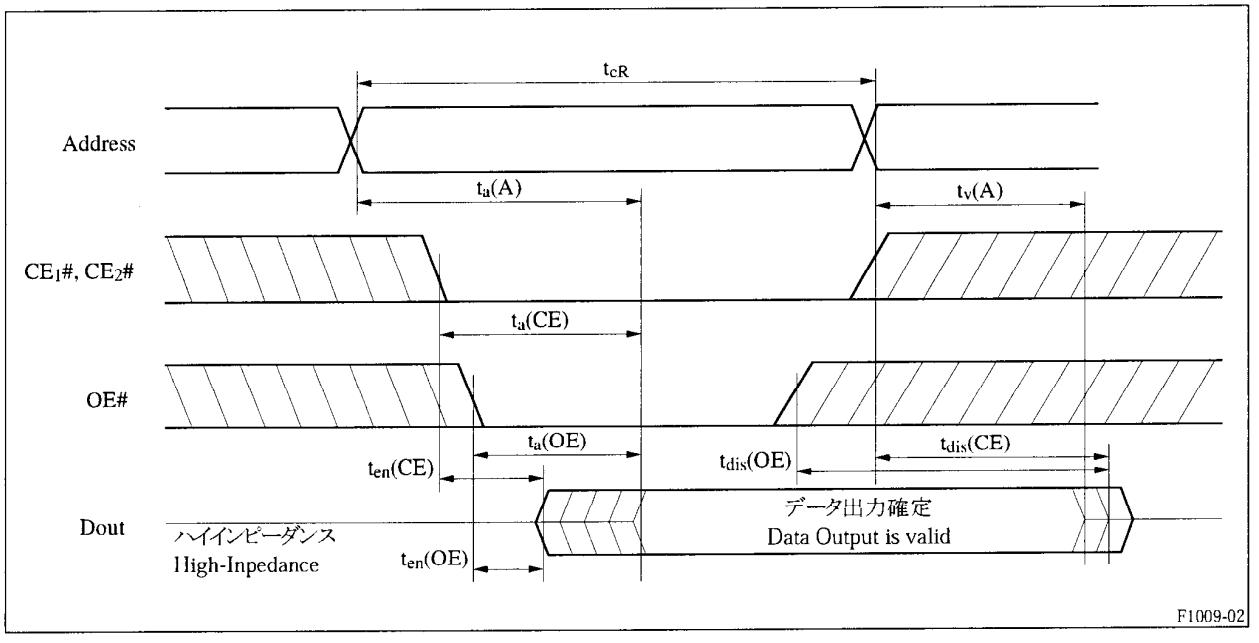


Figure 9. Attribute Memory Read Operation

13. 4 Attribute Memory Write Operation

(Ta=0~60℃)

PARAMETER	SYMBOL		Vcc=3.3V± 0.3V		Vcc=5V± 10%		Unit
	IEEE	JEIDA/ PCMCIA	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}	600	—	250	—	ns
Address Setup Time	t_{AVWL}	t_{su}(A)	50	—	30	—	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)	70	—	30	—	ns
Data Setup Time	t_{DVWH}	t_{su}(D-WEH)	150	—	80	—	ns
Data Hold Time	t_{WHDX}	t_h(D)	70	—	30	—	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)	350	—	180	—	ns
Write Pulse Width	t_{WLWH}	t_w(WE)	300	—	150	—	ns
Setup Time for OE#	t_{GHWL}	t_{su}(OE-WE)	35	—	10	—	ns
Hold Time for OE#	t_{WHGL}	t_h(OE-WE)	35	—	10	—	ns
Setup Time for CE#	t_{ELWH}	t_{su}(CE)	0	—	0	—	ns
Hold Time for CE#	t_{GHEH}	t_h(CE)	35	—	20	—	ns

T1057-01

Note) When the CIS constructed by EEPROM, this card requires 5V voltage for Vcc.

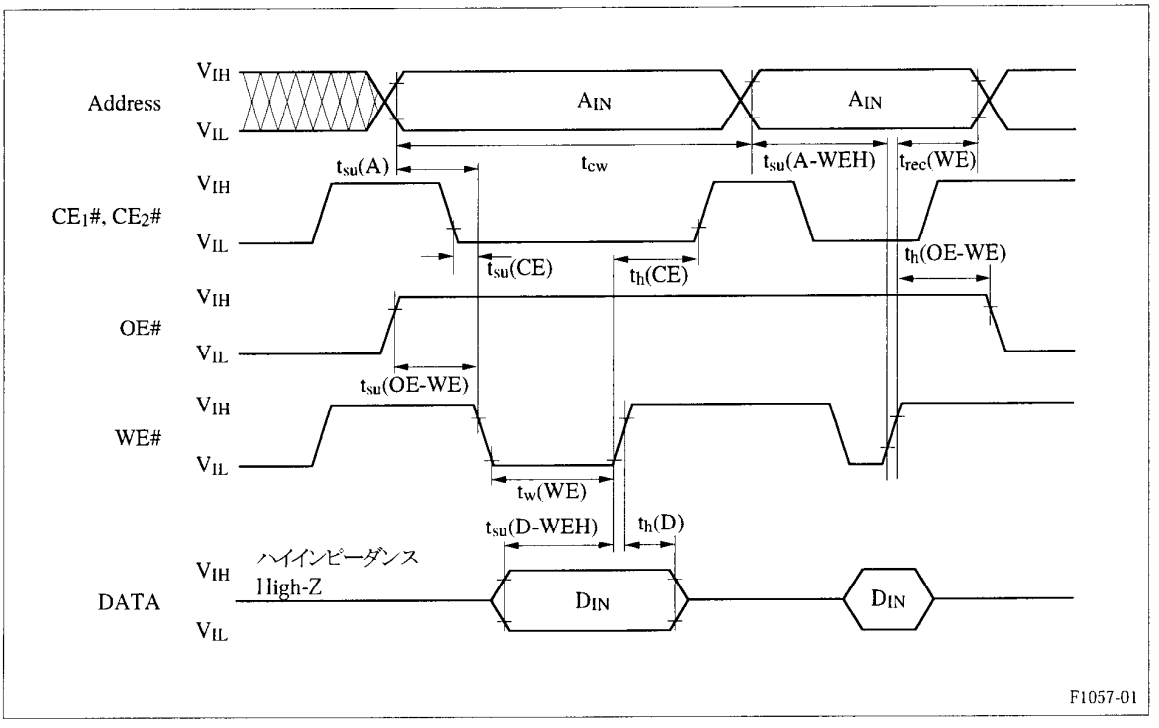


Figure 10. Attribute Memory Write Operation

13. 5 Power-Up/Power Down

PARAMETER	SYMBOL PCMCIA	NOTES	MIN	MAX	UNITS
CE# Signal Level (0.0V < V_{CC} < 2.0V)	V_i (CE)	1	0	V_{iMAX}	V
CE# Signal Level (2.0V < V_{CC} < V_{IH})		1	V_{CC}–0.1	V_{iMAX}	V
CE# Signal Level (V_{IH} < V_{CC})		1	V_{IH}	V_{iMAX}	V
CE# Setup Time	t_{su} (V_{CC})	—	20	—	ms
RESET Setup Time	t_{su} (RESET)	—	20	—	ms
CE# Recover Time	t_{rec} (V_{CC})	—	1.0	—	µs
V_{CC} Rising Time	t_{pr}	2	0.1	300	ms
V_{CC} Falling Time	t_{pf}	2	3.0	300	ms
RESET Width	t_w (RESET)	—	10	—	µs
RESET Width	t_h (Hi–Z RESET)	—	1	—	ms
RESET Width	t_s (Hi–Z RESET)	—	0	—	ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0V < V_{CC} < 2.0 V, Vi (CE#) is only 0.00V-V_{iMAX}
2. The t_{pr} and t_{pf} are defined as "linear waveforms" in the period of 10% to 90%, or vice-versa. Even if the waveform is not a "liner waveform," its rising and falling time must meet this specification.

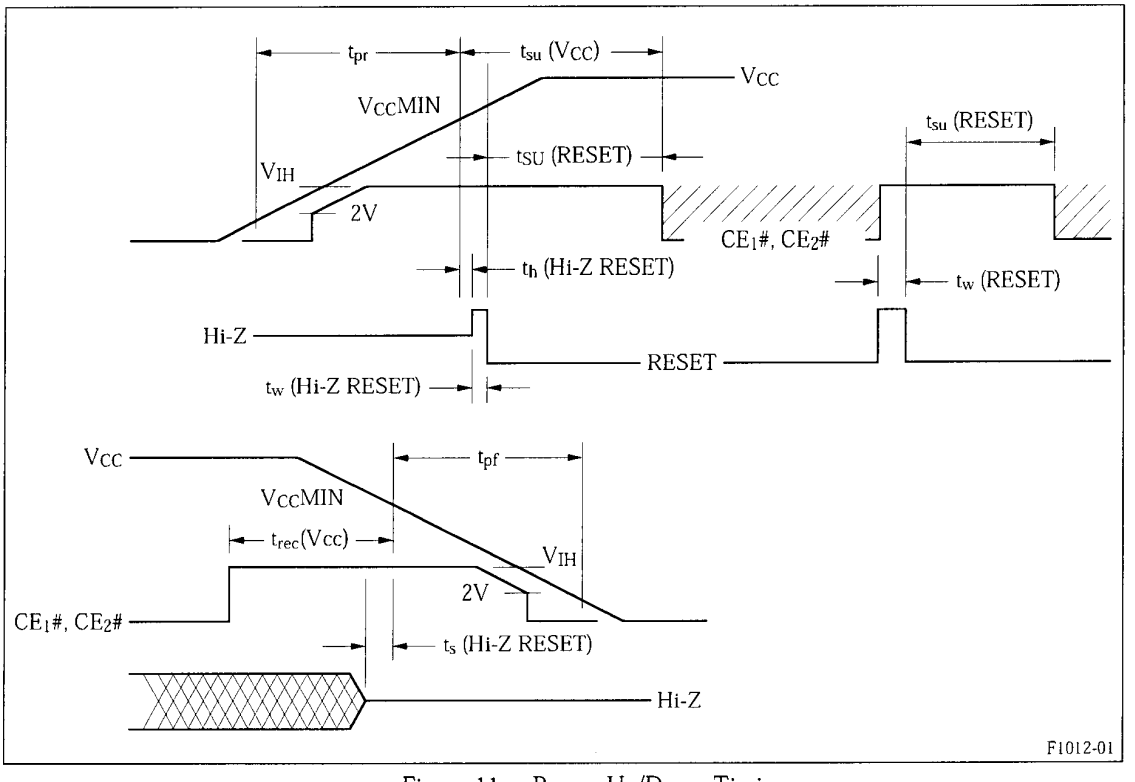


Figure 11. Power-Up/Down Timing

14. Specification Changes

This datasheet is for ID242 series product overview, and final specifications will be submitted for qualification of the memory card. Please note that contents of this datasheet may be revised without announcement beforehand. Please do NOT finalize a system design with this information.

15. Other Precautions

- Permanent damage occurs if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

16. External Diagrams