PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

ID244D01

2MB Flash Memory Card

(Model No.: ID244D01)

Spec No.: EL093106

Issue Date: March 25, 1997

SHARP

ID244D01

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  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliances
  - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
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  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

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Contents

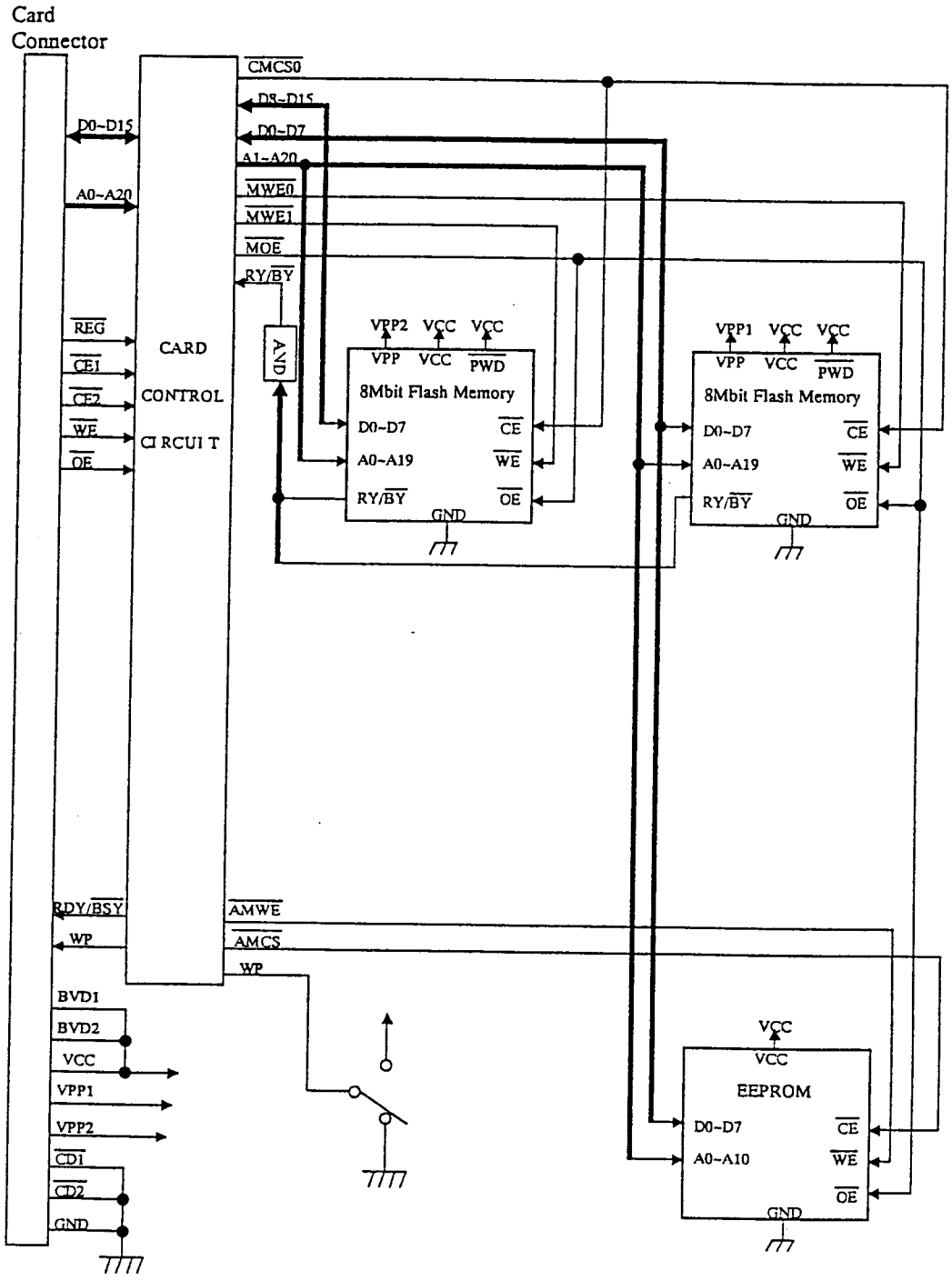
1. General Descriptions

The SHARP ID244D01, which panel design is SHARP standard, is a 2MB Flash Memory PC Card conforms to PCMCIA Release 2.0 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

2.1	Type	2MB Flash Memory Card (Conforms to PCMCIA Rel. 2.0)
2.2	Memory Capacity	
	Common Memory	2M words×8 bits or 1M words×16 bits
	Attribute Memory	EEPROM Model 2k words×8 bits read/write
	Note) We have another type of attribute memory as follows, No EEPROM Model. (5 words×8 bits read only in card's control circuit) Sample card name: ID244D02. Customers can choose one model from two.	
2.3	Supply Voltage	
	Read Cycle	Vcc=5±0.5V, Vpp1, Vpp2=0~1.5V
	Read/Program/Erase Cycle	Vcc=5±0.5V, Vpp1, Vpp2=5.0V±0.5V/12.0V±0.6V
2.4	Erase Unit	Block(64k bytes/byte access, 128k bytes/word access)
2.5	Program/Erase Cycles	100,000 cycles
2.6	Interface	Parallel I/O Interface
2.7	Function Table	See Function Table in page. 6
2.8	External Dimensions	54×85.6×3.3 mm
2.9	Pin Connections	See Pin Connections in page. 4
2.10	Type of Connector	Conforms to PCMCIA Rel. 2.0 Card Use Connector (Card connector: JC20-J68S-NB3 JAE or FCN-568J068-G/0 Fujitsu)
2.11	Average Weight	30g
2.12	Operating Temp Range	0 to 60℃
2.13	Storage Temp Range	-20 to 65℃
2.14	External Appearance	External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales.
2.15	Manufacturer's Code	The manufacturer's code shall be printed on the memory card directly or on the seal which is then attached to the memory card.
2.16	Brand Name	The user's brand name will be used.
2.17	Not designed or rated radiation hardened.	

3. Block Diagram



4. Pin Connections

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	18	Vpp1	35	GND	52	Vpp2
2	D3	19	A16	36	$\overline{CD1}$	53	A22(NC)
3	D4	20	A15	37	D11	54	A23(NC)
4	D5	21	A12	38	D12	55	A24(NC)
5	D6	22	A7	39	D13	56	A25(NC)
6	D7	23	A6	40	D14	57	NC
7	$\overline{CE1}$	24	A5	41	D15	58	NC
8	A10	25	A4	42	$\overline{CE2}$	59	NC
9	$\overline{OE}$	26	A3	43	NC	60	NC
10	A11	27	A2	44	NC	61	$\overline{REG}$
11	A9	28	A1	45	NC	62	BVD2
12	A8	29	A0	46	A17	63	BVD1
13	A13	30	D0	47	A18	64	D8
14	A14	31	D1	48	A19	65	D9
15	$\overline{WE}$ / $\overline{PGM}$	32	D2	49	A20	66	D10
16	RDY/ $\overline{BSY}$	33	WP	50	A21(NC)	67	$\overline{CD2}$
17	Vcc	34	GND	51	Vcc	68	GND

Pin Descriptions:

D0~D7	Data Bus (Input/Output)
D8~D15	Data Bus (Input/Output)
$\overline{A0}$~A20	Address Bus (Input)
$\overline{CE1}$, $\overline{CE2}$	Card Enable (Input)
$\overline{OE}$	Output Enable (Input)
$\overline{WE}$/$\overline{PGM}$	Write Enable/Program (Input)
$\overline{CD1}$, $\overline{CD2}$	Card Detect (Output)(Card Inserted Detection Signal)
WP	Write Protect (Output)(in write protect mode, the WP output signal is "HIGH")
Vpp1	Program/Erase Power Supply(Even Byte)
$\overline{Vpp2}$	Program/Erase Power Supply(Odd Byte)
$\overline{REG}$	Register Select (Input)
BVD1, $\overline{BVD2}$	Battery Voltage Detect(Always"HIGH")
RDY/$\overline{BSY}$	Ready/Busy (Output)

Notes:Pin 50:Address bit 21, Pin 53: Address bit 22, Pin 54 Address bit 23, Pin 55:Address bit 24 and Pin 56:Address bit 25 are no connection.

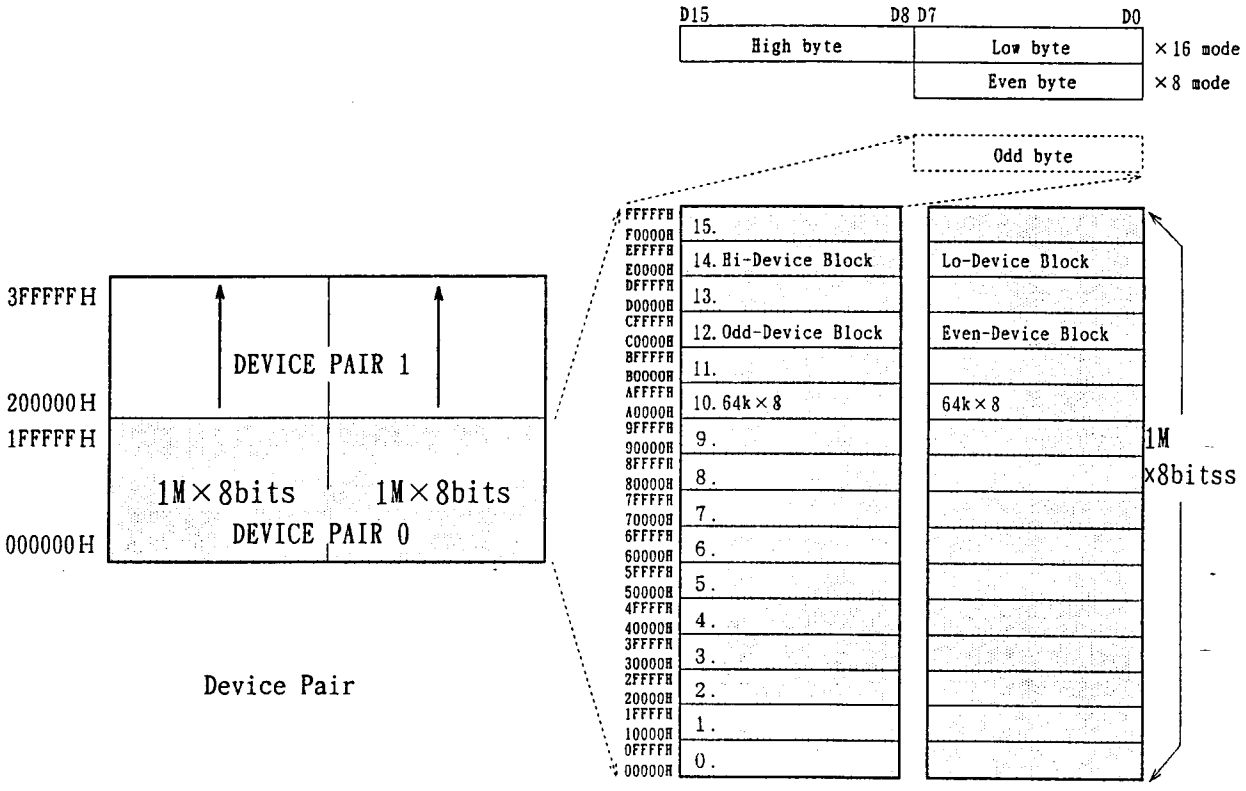
5. Function

5.1Memory Block

5.1.1 Memory Configuration 8Mbits Flash Memory x 2 Devices.

5.1.2 Memory Erase Unit Block Erase

Block : Byte Mode 64k bytes
Word Mode 128k bytes



5.2 Function Table

$\overline{CE1}$	$\overline{CE2}$	A0	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	Vpp1	Vpp2	Vcc	Operation	D0-D7	D8-D15	Status
H	H	×	×	×	H	VppL	VppL	Vcc		Hi-Z	Hi-Z	Standby
L	H	L	H	L	H	VppL	VppL	Vcc	Read(x8)	D_o(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppL	VppL	Vcc	Read(x8)	D_o(Odd))	Hi-Z	Byte
L	L	×	H	L	H	VppL	VppL	Vcc	Read(x16)	D_o(Even)	D_o(Odd)	Word
H	L	×	H	L	H	VppL	VppL	Vcc	Read(x8)	Hi-Z	D_o(Odd)	Byte
L	×	×	×	H	H	VppL	VppL	Vcc	Outpu Disable	Hi-Z	Hi-Z	Byte
H	L	×	×	H	H	VppL	VppL	Vcc	Outpu Disable	Hi-Z	Hi-Z	Byte
L	H	L	L	H	H	VppH	VppX	Vcc	Program(x8)	Di(Even)	Don't care	Byte
L	H	H	L	H	H	VppX	VppH	Vcc	Program(x8)	Di(Odd)	Don't care	Byte
L	L	×	L	H	H	VppH	VppH	Vcc	Program(x16)	Di(Even)	Di(Odd)	Word
H	L	×	L	H	H	VppX	VppH	Vcc	Program(x8)	Don't care	Di(Odd)	Byte
L	H	L	H	L	H	VppH	VppX	Vcc	Verify(x8)	Do(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppX	VppH	Vcc	Verify(x8)	Do(Odd)	Hi-Z	Byte
L	L	×	H	L	H	VppH	VppH	Vcc	Verify(x16)	Do(Even)	Do(Odd)	Word
H	L	×	H	L	H	VppX	VppH	Vcc	Verify(x8)	Hi-Z	Do(Odd)	Byte
L	H	H	L	L	H	VppH	VppX	Vcc	*1 Prohibited	———	———	———
L	H	L	L	L	H	VppX	VppH	Vcc	*1 Prohibited	———	———	———
L	L	×	L	L	H	VppH	VppH	Vcc	*1 Prohibited	———	———	———
H	L	×	L	L	H	VppX	VppH	Vcc	*1 Prohibited	———	———	———

*1. Do not use this mode as it will result in write errors.

H : High　　L : Low　　× : Don't care
Di : Input Data　　Do : Output Data　　Hi-Z : High Impedance
Vcc : 4.5～5.5V　　VppL : 0.0～1.5V　　VppH : 4.5~5.5V/11.4~12.6V
VppX : VppL or VppH

Caution: When the write protect switch is in protect-mode, the WP signal is "HIGH" and write operation are not allowed.

5.3 Software Command(8/16 Bits Operation ():16 Bits Operation)

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle			
		Operation	Address	Data	Operation	Address	Data Input	Data Output
Read Array /Reset	1	Write	RA	FFH/ (FFFFH)	——	——	——	——
Read Intelligent Identifier	3	Write	DA	90H/ (9090H)	Read	IA	——	IID
Read Status Register	2	Write	DA	70H/ (7070H)	Read	DA	——	SRD
Clear Status Register	1	Write	DA	50H/ (5050H)	——	——	——	——
Erase Setup /Erase Confirm	2	Write	BA	20H/ (2020H)	Write	BA	D0H/ (D0D0H)	——
Erase Suspend/ Erase Resume	2	Write	BA	B0H/ (B0B0H)	Write	BA	D0H/ (D0D0H)	——
Byte Write Setup/Write	2	Write	WA	40H/ (4040H)	Write	WA	WD	——
Alternate Byte Write Setup/Write	2	Write	WA	10H/ (1010H)	Write	WA	WD	——

Note) 1. This Table shows the basic form of Erase, Verify and Program Verify. Refer Programming Flowchart, Erase Algorithm in detail.
2. Bus operations are defined in function table in page.
3. IA:Device Identifier Address IID:Device Identifier Data

	DA	IA			IID	
		8Bits (Even Device)	8Bits (Odd Device)	16Bits	Byte (8Bits)	Word (16Bits)
Manufacturer Code	000000H~1FFFFFH	000000H	000001H	000000H	89H	8989H
Device Code	000000H~1FFFFFH	000002H	000003H	000001H	A6H	A6A6H

RA : Read Address WA : Write Address WD : Write Data
DA : Device Address (Any Address in device is acceptable.)
BA : Erase Block Address (Erase Size is 64k Bytes.)
SRD : Status Register Data

4. Either 40H(4040H) or 10H(1010H) are recognized by the WSM as the Byte Write Setup Command.

a) Read Array/Reset Command:(FFH/FFFFH)
By writing this command, device/devices pair become read mode. The device remains enable for reads until the Command User Interface contents are altered.

b) Intelligent Identifier Command:(90H/9090H):
After writing this command into the Commnand User Interface, a read cycle retrieves the manufacturer Code and device Code. To terminate the Operation, it is necessary to write another valid command into the register.

c) Read Status Register Command:(70H/7070H):
By Writing this command, the Status Register may be read at any time to determine when a byte or block erase operation is complete, and whether that operation completed successfully. Refer to Status Register definition in page. 9 . After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface.

d) Clear Status Register Command:(50H/5050H)
Status bits which show error, the Erase Status(SR. 5), Byte Write Status(SR. 4) bits and the Vpp Status bit(SR. 3) can be reset by the Clear Status Machine Register Command.

e) Erase Setup/Erase Command:(20H/2020H)/(D0H/D0D0H):
Erase is executed one block(64kB for 1 device, 128kB for 2 devices) at a time.
This command is functional when Vpp=VppH and an Erase Setup Command is first written to the Command User Interface, followed by the Erase Confirm Command. After that, the device automatically outputs Status Register data when read. The CPU can detect the completion of the erase event by analyzing the output of the RDY/$\overline{BSY}$ pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked.
If erase error is detected, the Status Register should be cleared.

f) Erase Suspend/Erase Resume Command:(B0H/B0B0H)/(D0H/D0D0H)
The Erase Suspend command allows block erase interruption in order to read data from another block of memory. The device continues to output Status Register data when read, after the Erase Suspend Command is written. Polling the WSM Status and Erase Suspend Statu Status bits will determine when the erase operation has been suspended. RDY/$\overline{BSY}$ pin will also transition to V_{OH}. At this point, a Read Array Command can be written to the Command User Interface to read data from blocks other than that which is suspended. Vpp must remain at V_{PPH} while device is in Erase Suspend. Erase Resume Command , at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RDY/$\overline{BSY}$ pin will return to V_{OL}. After the Erase Resume is written, the device automatically output Status Register data when read.

g) Byte Write Setup/Write Command:(40H/4040H) or (10H/1010H)
This command is functional when Vpp=VppH and an Byte Write Setup Command is first written to the Command User Interface, followed by a second write specifying the address and data to be written. The WSM then take over, controlling the byte write and write verify algorithms internally. After the two command byte sequence is written to it, the device automatically outputs Status Register data when read. The CPU can detect the completion of the byte write event by analyzing the output of the RDY/$\overline{BSY}$ pin , or the WSM Status bits of the Status Register.

5.4 Status Register

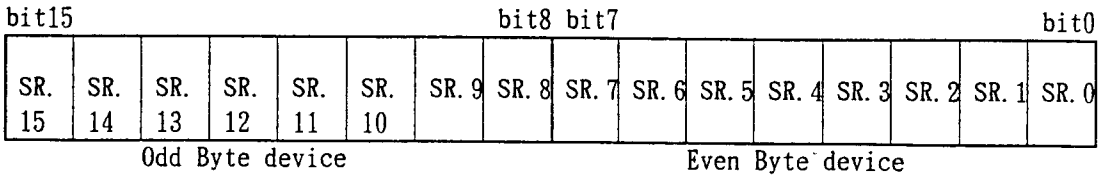
The memory devices in this card have Status Register which shows state of the device.

Byte Access x8 Bits

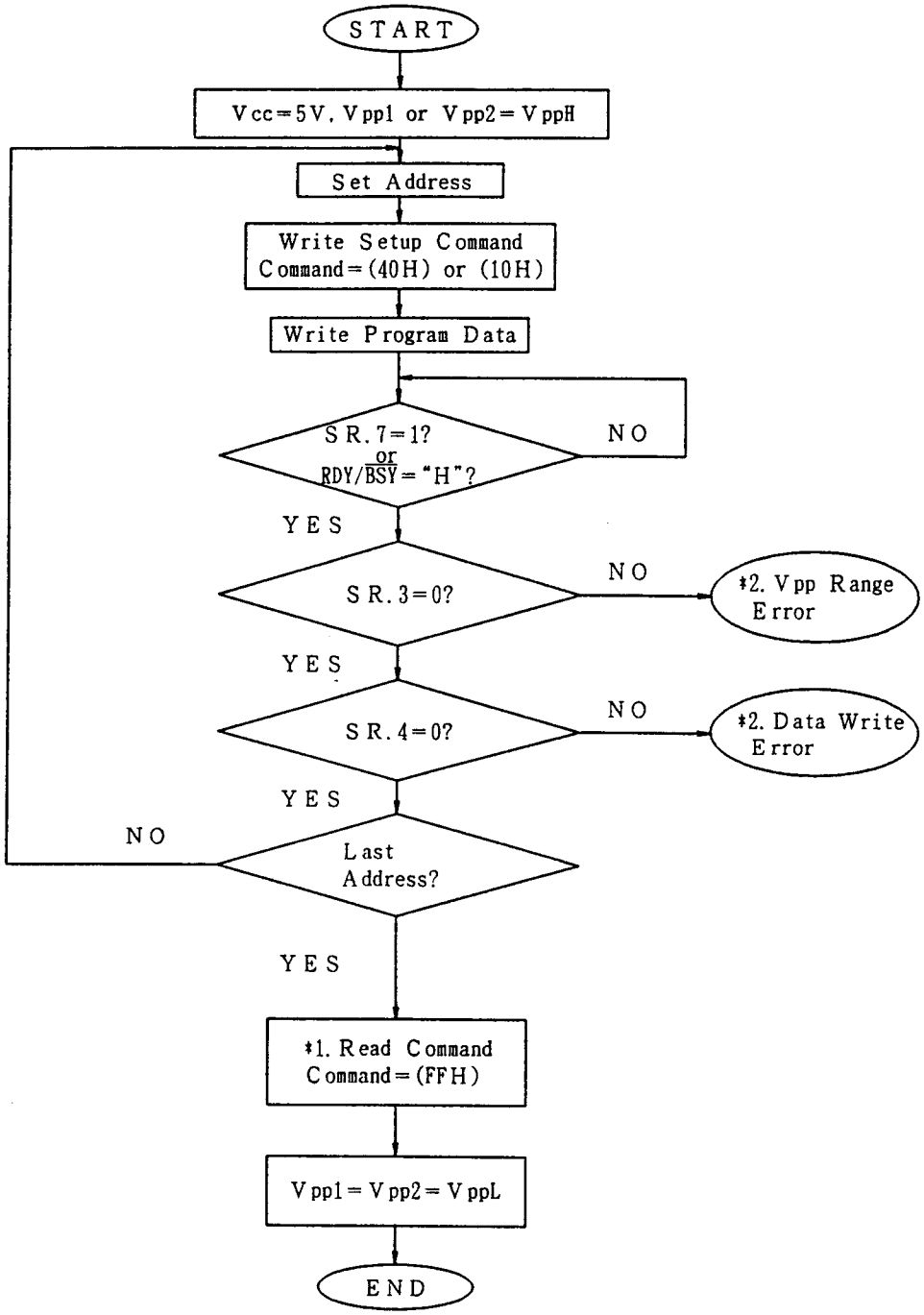
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
WSMS	ESS	ES	BWS	VPPS	RFU	RFU	RFU

Register	Contents
SR. 7 = Write State Machine Status 1 = Ready 0 = Busy	When set "1"s, read, erase, data write is acceptable.
SR. 6 = Erase Suspend Status 1 = Erase Suspend 0 = Erase In Progress/Completed	Check whether Erase Suspend Command is executed or not.
SR. 5 = Erase Status 1 = Error In Block Erase 0 = Successful Block Erase	Set "1"s when fail to Erase. Reset by the Clear Status Register Command.
SR. 4 = Byte Write Status 1 = Error In Byte Write 0 = Successful Byte Write	Set "1"s when fail to Byte write. Reset by the Clear Status Register Command.
SR. 3 = Vpp Status 1 = Vpp Low Detect; Operation Abort 0 = Vpp OK	Set "1"s when Vpp, which is needed in Byte Write or Erase operation, is below VppH. Reset by the Clear Status Register Command.
SR. 2~SR. 0 = Reserved for Future Use	

Word Access x16 bits

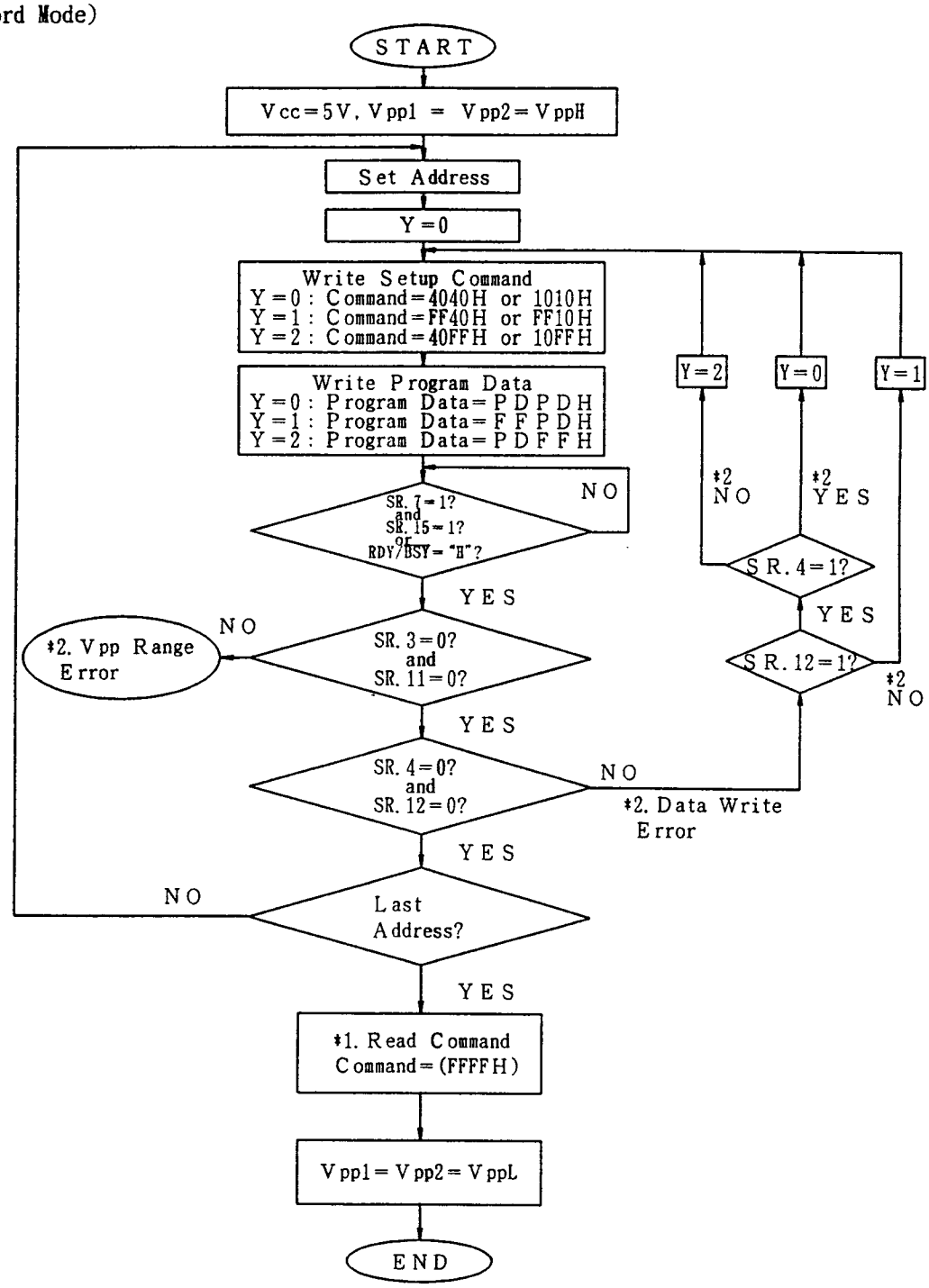


5.5 Programming Flowchart
(Byte Mode)



Note) *1. Write FFH after the last block write operation to reset the device to Read Array Mode.
*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

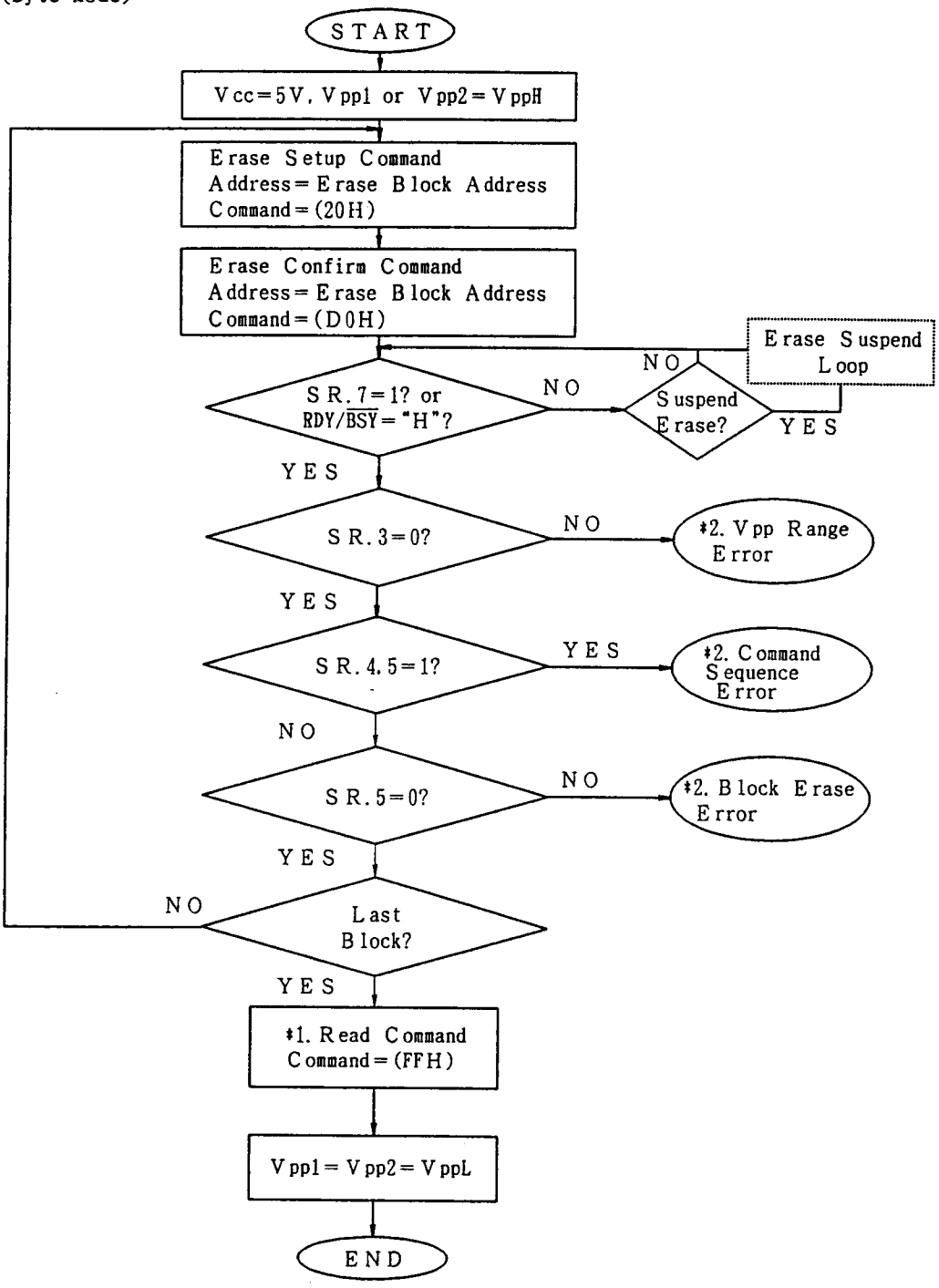
Programming Flowchart
(Word Mode)



Note) *1. Write FFFFH after the last block write operation to reset the device to Read Array Mode.

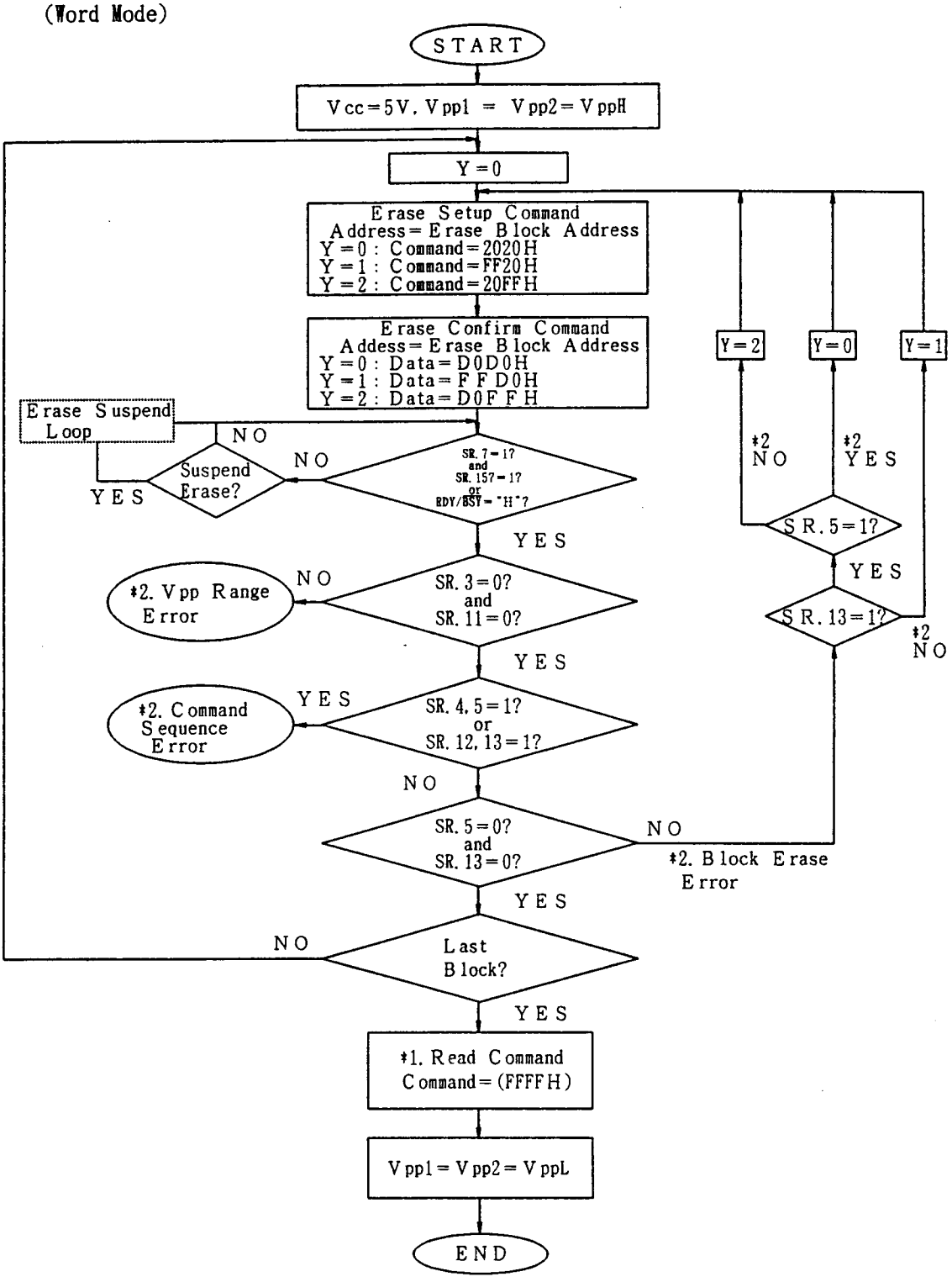
*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

5.6 Erase Algorithm
(Byte Mode)



Note) *1. Write FFH after the last block erase operation to reset the device to Read Array Mode.
*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

Erase Algorithm
(Word Mode)



Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

6. Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-0.3 to Vcc+0.3(Max:7.0)	V
Output Voltage	V_{OUT}	-0.3 to Vcc+0.3(Max:7.0)	V
Operating Temperature	T_{OPR}	0 to +60	℃
Storage Temperature	T_{STG}	-20 to +65	℃

7. Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Operating Temperature	T_{OPR}	0	+60	℃
Supply Voltage	V_{CC}	4.5	5.5	V
Input Voltage High	V_{IH}	3.5	V_{CC}+0.3	V
Input Voltage Low	V_{IL}	-0.3	1.5	V

8. Capacitance

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	—	17	—	pF	V_{CC}=5V±10%
Input/Output Capacitance	C_{IO}	—	17	—	pF	f=1MHz, Ta=25℃

9. Read Operation

9.1 D C Characteristics (Vcc=4.5~5.5V, Ta=0~60℃)

	PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
1	Operating Voltage	High Temperature / Low Temperature	V_{CC}	4.50	—	5.50	V	
*1 2	Current Consumption	Static Operatin Current	I_{SB}	—	—	2.0	mA	X16, Address :PingPong
		Dynamic Operating Current	I_{CC}	—	—	80		
3	Input Voltage	Input Voltage Level High	V_{IH}	3.5	—	Vcc+0.3	V	Vcc= 4.5~5.5V
		Input Voltage Level Low	V_{IL}	-0.3	—	1.5		
4	Input Current	A0~A20, D0~D15	I_{LI}	-10	—	70	μA	V_I=Vcc, 0V
		$\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$, $\overline{REG}$		-70		10		
5	Output Voltage	High	V_{OH}	Vcc-0.5	—	—	V	I_{OH}=-2mA(*2) I_{OH}=-4μA(*3)
		Low	V_{OL}	—	—	0.4		I_{OL}= 4mA

PingPong: Scan the target address, with accessing the target and another address alternately.

*1 (1) Static Operating Current: With the memory card's voltage at 5.5V and the $\overline{CE1}$, $\overline{CE2}$ $\overline{OE}$, $\overline{WE}$ and $\overline{REG}$ signals "HIGH" (V_{IH}=V_{CC}-0.2V), A0 signal "LOW" (V_{IL}≦0.2V) the current consumption is measured with the output open.

(2) Dynamic Operating Current : With the memory card's Vcc at 5.5V and Vpp1=Vpp2 at 12.6V, current consumption during access is measured with the output open. (Access time: 200ns) The current depends on addressing.

*2 D0~D15

*3 BVD1, BVD2, RDY/$\overline{BSY}$, WP

9.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=0.0~1.5V, Ta=0~60℃)

Testing Conditions:

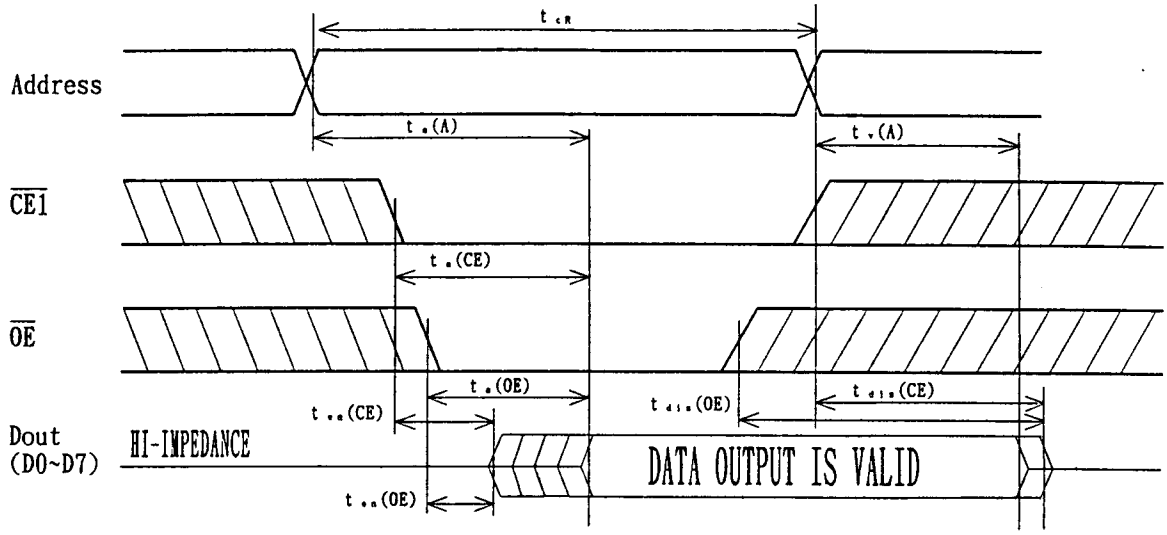
1) Input Pulse Level : 0.8~3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+C_L(100pF) (including scope and jig capacitance)

9.2.1 Read Cycle (Vcc=4.5~5.5V, Vpp=0.0~1.5V, Ta=0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Read Cycle Time	t_{AVAV}	t_{cR}	200	—	ns
Address Access Time	t_{AVQV}	t_a(A)	—	200	
Card Enable Access Time	t_{ELQV}	t_a(CE)	—	200	
Output Enable Access Time	t_{GLQV}	t_a(OE)	—	100	
Output Disable Time from $\overline{CE}$*	t_{EHQV}	t_{dis}(CE)	—	90	
Output Disable Time from $\overline{OE}$*	t_{GHQZ}	t_{dis}(OE)	—	90	
Output Enable Time from $\overline{CE}$	t_{ELQX}	t_{en}(CE)	5	—	
Output Enable Time from $\overline{OE}$	t_{GLQX}	t_{en}(OE)	5	—	
Data Valid from Add Change		t_v(A)	0	—	

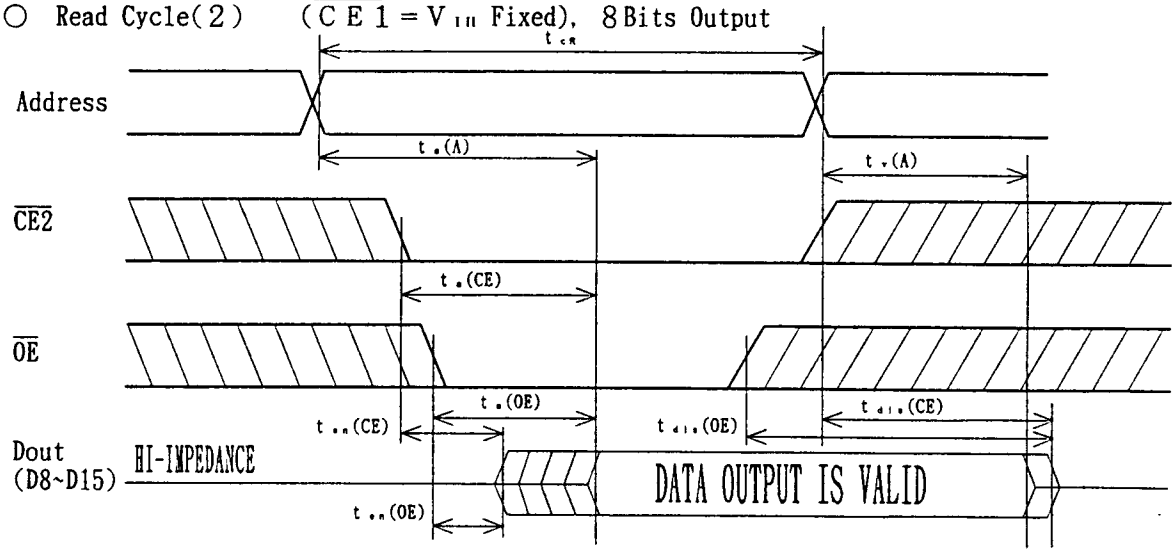
*Time until output becomes floating. (The output voltage is not defined.)

○ Read CYCLE(1) ($\overline{CE2}$ = V_{IH} Fixed), 8 Bits Output



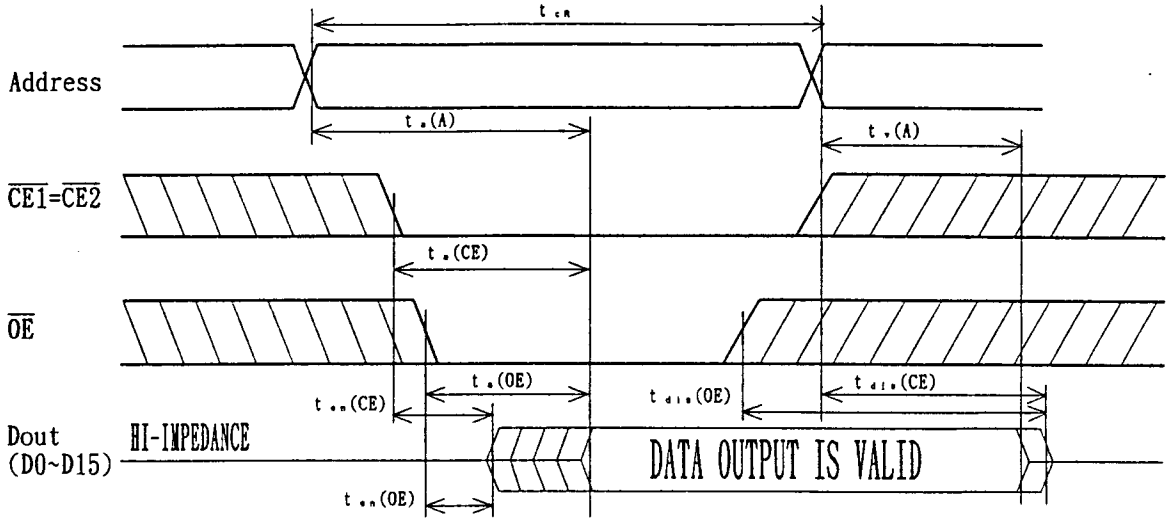
Note) 1. $\overline{WE}$="HIGH", during a read cycle.
2. Either "HIGH" or "LOW" in diagonal areas.
3. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE) have concluded.

○ Read Cycle(2) ($\overline{CE1}$ = V_{IH} Fixed), 8 Bits Output



Note) 1. $\overline{WE}$="HIGH", during a read cycle.
2. Either "HIGH" or "LOW" in diagonal areas.
3. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE) have concluded.

○ Read Cycle (3), 16Bits Output



Note) 1. $\overline{WE}$="HIGH", during a read cycle.
2. Either "HIGH" or "LOW" in diagonal areas.
3. Change $\overline{CE1}$ and $\overline{CE2}$ at the same time.
4. The output data becomes valid when last interval, ta(A), ta(CE) or ta(CE) have concluded.

10. Programming Operation

10.1 D C Characteristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Vpp1, Vpp2 operating Voltage	Read	V_{PPL}	0	1.5	V	
	Program	V_{PPH}	4.5	5.5		Vpp=4.5~5.5V
			11.4	12.6		Vpp=11.4~12.6V
Vpp1, Vpp2 operating Current (X16 Mode)	Read	I_{SB2}	–	1.6	mA	Input open
	Program	I_{PP}	–	45		RMS Vpp=4.5~5.5V
			–	20		Vpp=11.4~12.6V
Vcc operating Current	Standby	I_{SB1}	–	2		Input open
	Program	I_{CC}	–	75		RMS X16 Mode
Input Voltage		V_{IL}	-0.3	1.5	V	
		V_{IH}	3.5	Vcc+0.3		
Output Votltage During Verify		V_{OL}	–	0.4		I_{OL}= 4mA
		V_{OH}	Vcc-0.5	–		I_{OH}=-2mA

Note) 1. Power on Vcc before power on Vcc, power off Vcc after power off Vpp.
2. Keep Vpp including its overshoot, below 13V.
3. Card insertion or removal while applying Vpp=12V may cause a loss of integrity.
4. Do not turn on or turn off during $\overline{CE}$="LOW".
5. If V_{IH} goes above Vcc+0.3V, normal operation is not assured.

10.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

Testing Conditions:

1) Input Pulse Level : 0.8～3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+C_L(100pF) (including scope and jig capacitance)

10.2.1 Program Cycle

$\overline{WE}$ Controlled (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

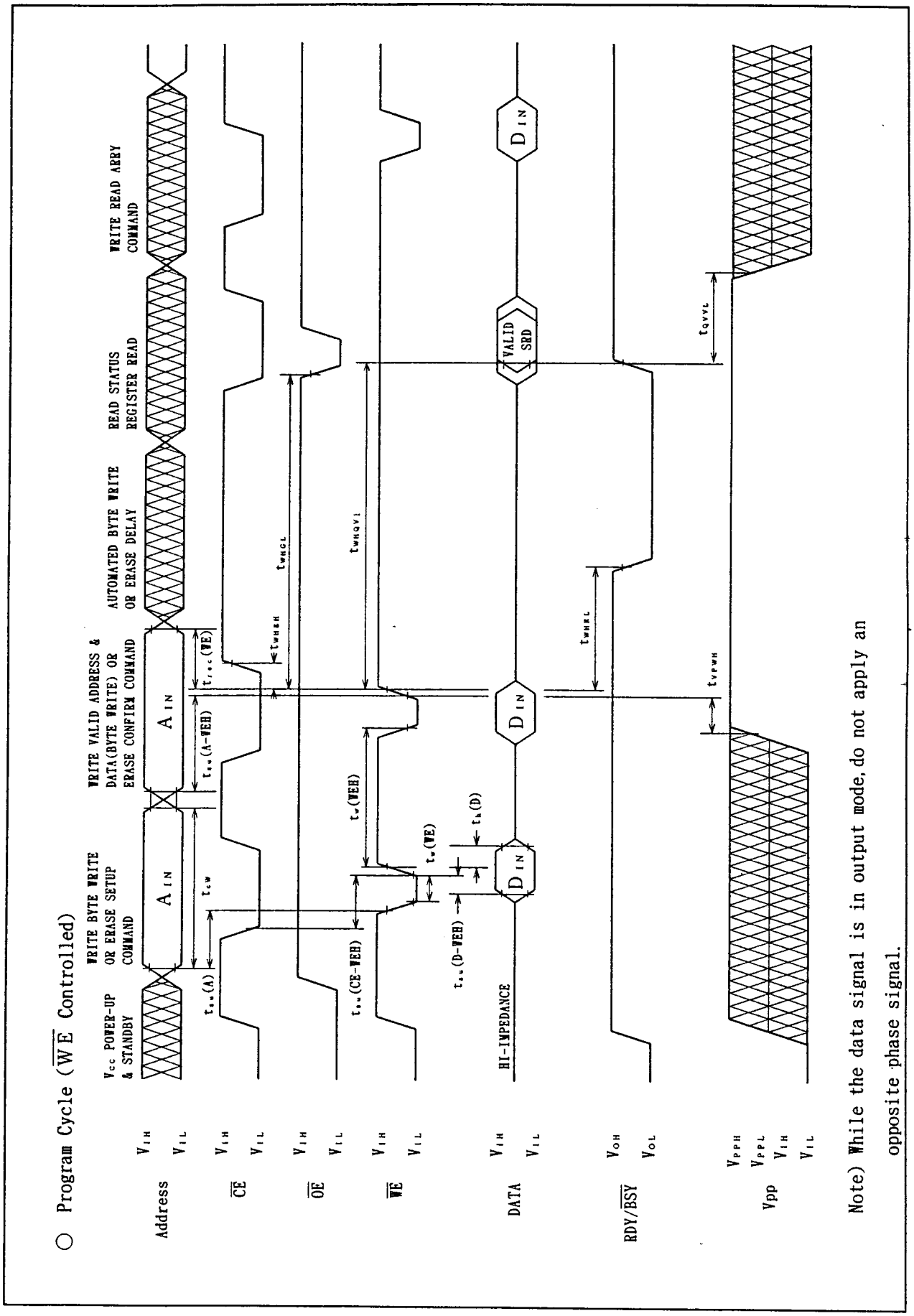
PARAMETER		SYMBOL		MIN	MAX	UNIT
		SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time		t_{AVAV}	t_{cw}	200	–	ns
Address Setup Time		t_{AVWL}	t_{su}(A)	20	–	
Write Recovery Time		t_{WHAX}	t_{rec}(WE)	30	–	
Data Setup Time for $\overline{WE}$		t_{DVWH}	t_{su}(D-WEH)	60	–	
Data Hold Time		t_{WHDX}	t_h(D)	30	–	
Write Recovery Before Read		t_{WHGL}		10	–	
Card Enable Setup time for $\overline{WE}$		t_{ELWH}	t_{su}(CE-WEH)	140	–	
Address Setup for $\overline{WE}$		t_{AVWH}	t_{su}(A-WEH)	140	–	
Card Enable Hold Time		t_{WHEH}		15	–	
Write Pulse Width		t_{WLWH}	t_w(WE)	120	–	
Write Pulse Width High		t_{WHWL}	t_w(WEH)	30	–	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t_{WHRL}		–	150	
Duration of write operation	Vpp=4.5~5.5V	t_{WHQV1}		6.5	–	μs
	Vpp=11.4~12.6V			4.8	–	
Vpp Setup to $\overline{WE}$ Going High		t_{VPWH}		100	–	ns
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t_{QVVL}		0	–	

$\overline{CE}$ Controlled (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL		MIN	MAX	UNIT
		SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time		t_{AVAV}	t_{cw}	200	–	ns
Address Setup Time		t_{AVEL}	t_{su}(A)	20	–	
Write Recovery Time		t_{EHAX}	t_{rec}(CE)	30	–	
Data Setup Time for $\overline{CE}$		t_{DVEH}	t_{su}(D-CEH)	60	–	
Data Hold Time		t_{EHDX}	t_h(D)	30	–	
Write Recovery Before Read		t_{EHGL}		10	–	
Write Enable Setup time for $\overline{CE}$		t_{WLEH}	t_{su}(WE-CEH)	140	–	
Address Setup for $\overline{CE}$		t_{AVEH}	t_{su}(A-CEH)	140	–	
Write Enable Hold Time		t_{EHWH}		0	–	
Write Pulse Width		t_{ELEH}	t_w(CE)	120	–	
Write Pulse Width High		t_{EHEL}	t_w(CEH)	30	–	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t_{EHRL}		–	150	
Duration of write operation	Vpp=4.5~5.5V	t_{EHQV1}		6.5	–	μs
	Vpp=11.4~12.6V			4.8	–	
Vpp Setup to $\overline{WE}$ Going High		t_{VPEH}		100	–	ns
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t_{QVVL}		0	–	

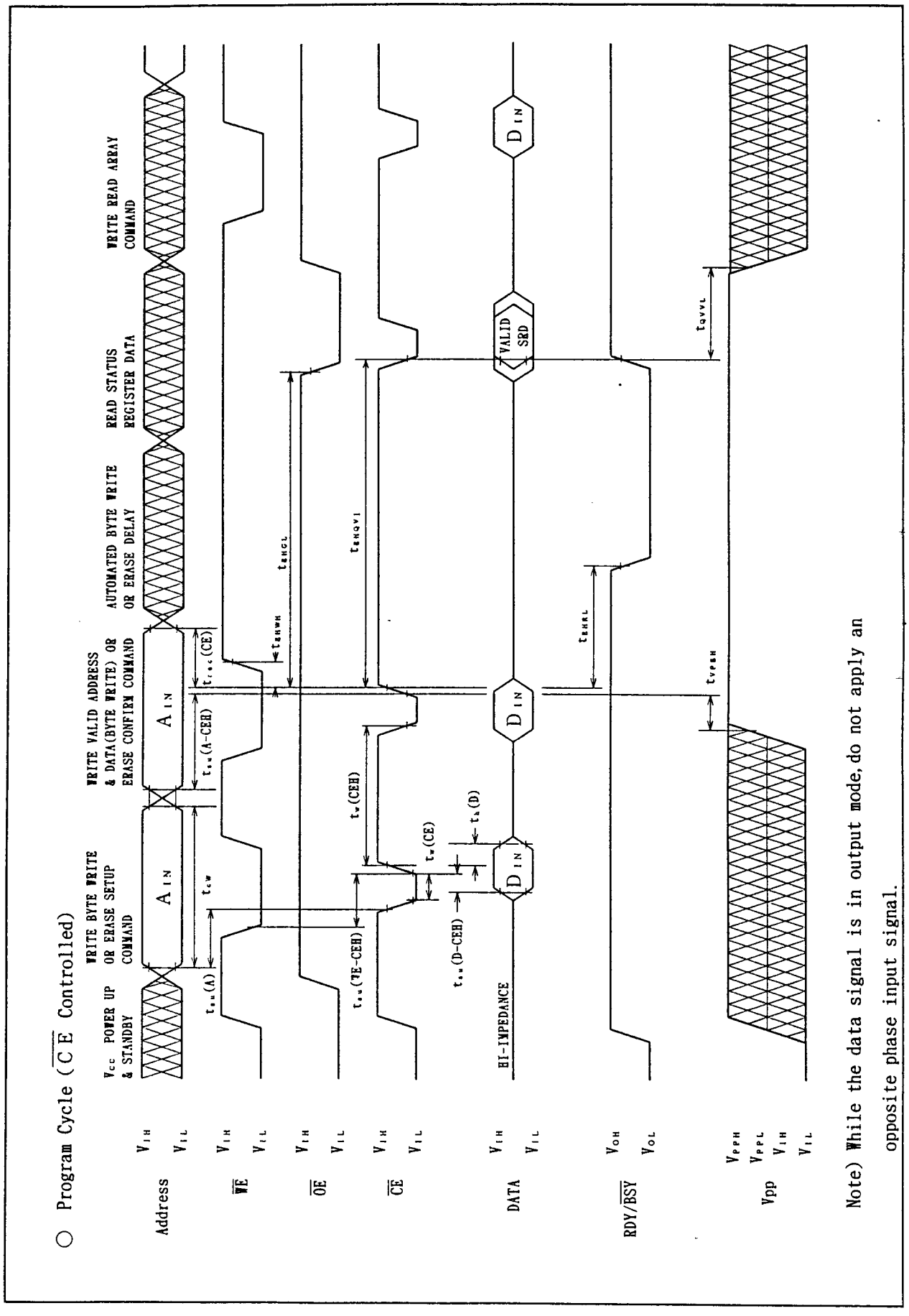
1. Set $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when Vpp changes from VppL to VppH or vice versa.

○ Program Cycle ($\overline{WE}$ Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase signal.

○ Program Cycle ($\overline{CE}$ Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11. Erase Operation

11.1 D C Charactristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION	
Vpp1, Vpp2 Operating Voltage	Read	V_{PPL}	0	1.5	V		
	Program	V_{PPHE}	4.5	5.5		Vpp=4.5~5.5V	
			11.4	12.6		Vpp=11.4~12.6V	
Vpp1, Vpp2 Operating Current (X16 Mode)	Standby	I_{SB2}	−	1.6	mA	I/O open	
	Erase	I_{PP}	−	45		RMS	Vpp=4.5~5.5V
			−	20			Vpp=11.4~12.6V
	Erase Suspend	I_{PPS}	−	1.6		$\overline{CE1}$, $\overline{CE2}$=V_{IH}, RMS	
Vcc Operating Current (X16 Mode)	Standby	I_{SB1}	−	2.0		I/O open	
	Erase	I_{CCE}	−	75	V	RMS	
	Erase Suspend	I_{CCES}	−	22		$\overline{CE1}$, $\overline{CE2}$=V_{IH}, RMS	
Input Voltage		V_{IL}	-0.3	1.5			
		V_{IH}	3.5	Vcc+0.3			
Output Voltage During Verify		V_{OL}	−	0.4		I_{OL}= 4mA	
		V_{OH}	Vcc-0.5	−		I_{OH}=-2mA	

Note) Power on Vcc before power on Vcc , power off Vcc after power off Vpp. Keep Vpp including its overshoot, below 13V. Card insertion or removal while applying Vpp=12V may cause a loss of integrity. Do not turn on or turn off during CE="LOW". If V_{IH} goes above Vcc+0.3V, normal operation is not assured.

11.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

Testing Conditions:

1) Input Pulse Level : 0.8～3.5V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 1TTL+C_L(100pF) (including scope and jig capacitance)

11.2.1 Erase Cycle

$\overline{WE}$ Controlled (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

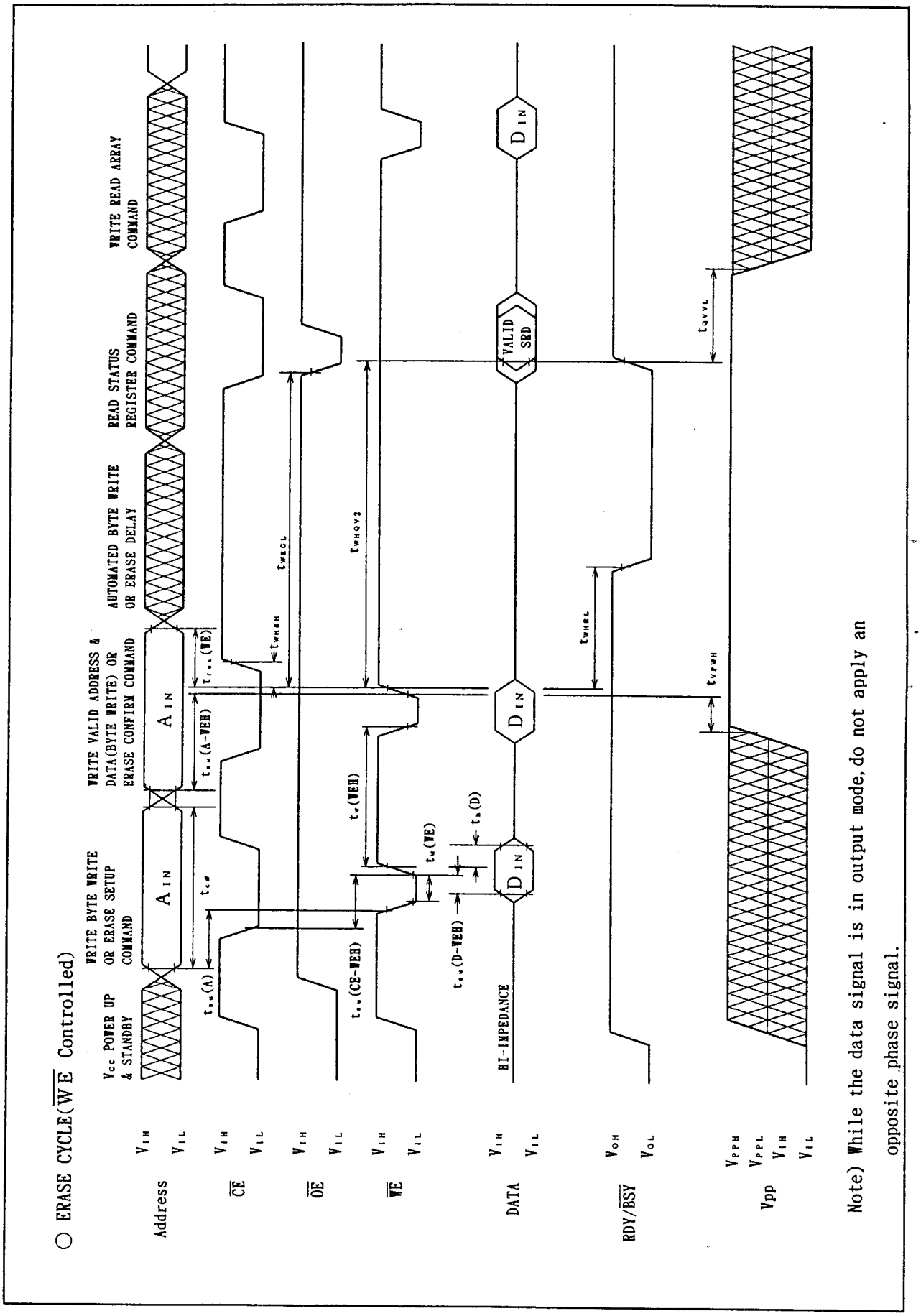
PARAMETER		SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time		t_{AVAV}	t_{cW}	200	−	ns
Address Setup Time		t_{AVWL}	t_{su}(A)	20	−	
Write Recovery Time		t_{WHAX}	t_{rec}(WE)	30	−	
Data Setup Time for $\overline{WE}$		t_{DVWH}	t_{su}(D-WEH)	60	−	
Data Hold Time		t_{WHDX}	t_h(D)	30	−	
Write Recovery Before Read		t_{WHGL}		10	−	
Card Enable Setup time for $\overline{WE}$		t_{ELWH}	t_{su}(CE-WEH)	140	−	
Address Setup for $\overline{WE}$		t_{AVWH}	t_{su}(A-WEH)	140	−	
Card Enable Hold Time		t_{WHEH}		15	−	
Write Pulse Width		t_{WLWH}	t_w(WE)	120	−	
Write Pulse Width High		t_{WHWL}	t_w(WEH)	30	−	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t_{WHRL}		−	150	
Duration of Erase operation	Vpp=4.5~5.5V	t_{WHQV2}		0.9	−	s
	Vpp=11.4~12.6V			0.3	−	
Vpp Setup to $\overline{WE}$ Going High		t_{VPWH}		100	−	ns
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t_{QVVL}		0	−	

$\overline{CE}$ Controlled (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time		t_{AVAV}	t_{cw}	200	–	ns
Address Setup Time		t_{AVEL}	t_{su}(A)	20	–	
Write Recovery Time		t_{EHAX}	t_{rec}(CE)	30	–	
Data Setup Time for $\overline{CE}$		t_{DVEH}	t_{su}(D-CEH)	60	–	
Data Hold Time		t_{EHDX}	t_h(D)	30	–	
Write Recovery Before Read		t_{EHGL}		10	–	
Write Enable Setup time for CE		t_{WLEH}	t_{su}(WE-CEH)	140	–	
Address Setup for $\overline{CE}$		t_{AVEH}	t_{su}(A-CEH)	140	–	
Write Enable Hold Time		t_{EHWH}		0	–	
Write Pulse Width		t_{ELEH}	t_w(CE)	120	–	
Write Pulse Width High		t_{EHEL}	t_w(CEH)	30	–	
$\overline{WE}$ High to RDY/$\overline{BSY}$ Going Low		t_{EHRL}		–	150	
Duration of Erase operation	Vpp=4.5~5.5V	t_{EHQV2}		0.9	–	s
	Vpp=11.4~12.6V			0.3	–	
Vpp Setup to $\overline{WE}$ Going High		t_{VPEH}		100	–	ns
Vpp Hold from Valid SRD, RDY/$\overline{BSY}$ High		t_{QVVL}		0	–	

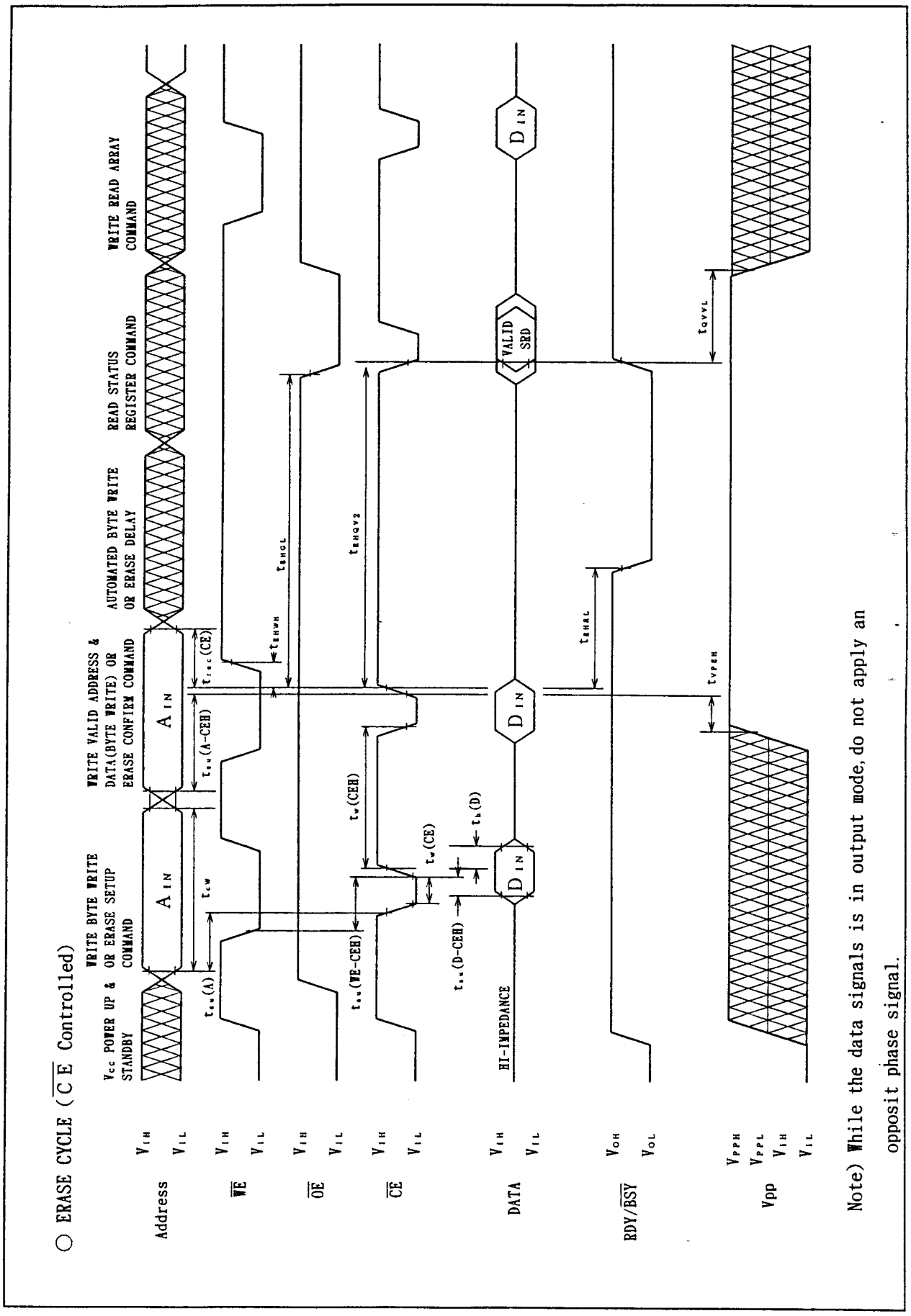
1. Set $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$ and $\overline{WE}$ "HIGH", when Vpp changes from PPr to PPH or vice versa.

○ ERASE CYCLE($\overline{WE}$ Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase signal.

○ ERASE CYCLE ($\overline{CE}$ Controlled)



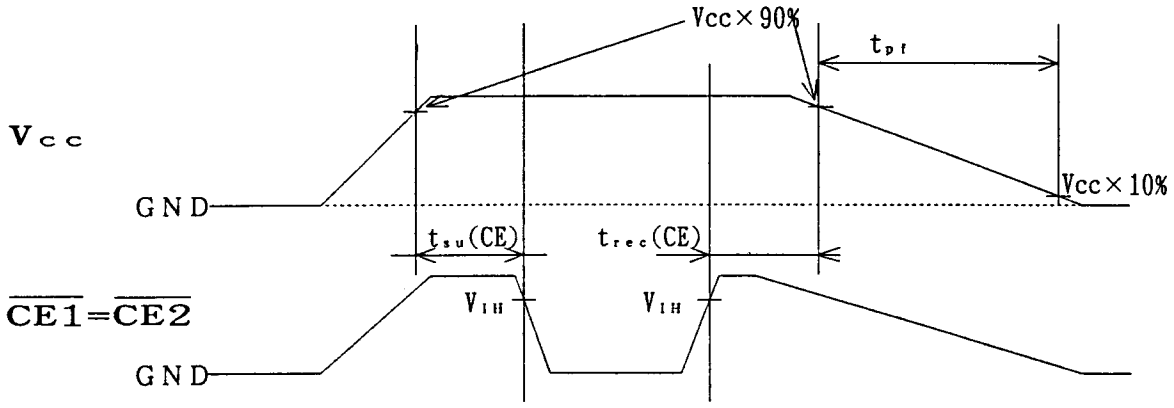
Note) While the data signals is in output mode, do not apply an opposit phase signal.

12. Block Erase and Data Write Characteristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60℃)

PARAMETER		MIN	TYP	MAX	UNIT
Block Pair Erase Time	Vpp=4.5~5.5V	–	1.1	10	s
	Vpp=11.4~12.6V	–	1.0	10	
Block Pair Write Time	Vpp=4.5~5.5V	–	0.5	2.1	
	Vpp=11.4~12.6V	–	0.4	2.1	

13. Voltage Timing (Ta = 25℃)



$3.5V < V_{IH} < Vcc+0.3$

PARAMETER	SYMBOL	MIN	MAX	UNIT
$\overline{CE}$ Setup Time	$t_{su}(CE)$	4.0	–	ms
$\overline{CE}$ Recovery Time	$t_{rec}(CE)$	1.0	–	μs
Vcc Falling Time	t_{pf}	3.0	300	ms

Note)

1. When Vcc(4.5~5.5V) is applied to the memory card and you are inserting or removing the card, $\overline{CE1}$, $\overline{CE2}$ should both be high-impedance. At such a time, other signal line should also be hi-impedance. After inserting the memory card, do not access it during the $\overline{CE}$ setup time(minimum of 4ms).
(During this time, neither $\overline{CE1}$ nor $\overline{CE2}$="LOW".)

2. When Vcc is turn on, if the condition(for example, Vcc rising time, etc) is not sufficient to as specified, it is possible that device's Status Register is not cleared or device not becomes to Read Array Mode. To prevent these, it is recommmended that using software command, reset the Status Register or set the device to Read Array Mode.
   ex.
   Reset the Status Register 50H(5050H)
   Set to Read Array Mode FFH(FFFFH)

14. Attribute Memory

The attribute memory holds the attribute informations of the card such as the type of card, bit configuration, speed and so on.

EEPROM Model

Card has 2k bytes of EEPROM attribute memory. To read the attribute memory, set $\overline{REG}$="LOW" and perform a read with the same access timming as common memory read. For this operation, access time is 300ns maximum. To allow 2k bytes of attribute memory, even addresses from 0 to 4096 are reserved. Since only the even-numbered bytes are used, reading odd-numbered bytes will result in invalid data.

Note)We have another type of attribute memory as follows,

No EEPROM Model. (Model no. ID244D02: 5 bytes device informations in even address 0 to 8, read only in card's control circuit, with the same access timming as common memory read)

14.1 Attribute Memory Read/Write Function Chart

CE1	CE2	AO	WE	OE	REG	MODE	$D_0 \sim D_7$	$D_8 \sim D_{15}$	STATUS
H	H	X	X	X	X		High-Z	High-Z	Standby
L	H	L	H	L	L	Read (×8)	D_0(even byte)	High-Z	Byte Access
L	H	H	H	L	L		High-Z	High-Z	Standby
L	L	X	H	L	L	Read (×8)	D_0(even byte)	High-Z	Byte Access
H	L	X	H	L	L		High-Z	High-Z	Standby
L	H	L	L	H	L	Write (×8)	D_i(even byte)	xxx	Byte Access
L	H	H	L	H	L		xxx	xxx	Standby
L	L	X	L	H	L	Write (×8)	D_i(even byte)	xxx	Byte Access
H	L	X	L	H	L		xxx	xxx	Standby
L	X	X	H	L	L	Attribute Memory Address 0~8	D_0	High-Z	Byte Access

H : High
L : Low
X : High/Low not applicable

D_i: Input Data
D_o: Output Data
High-Z: High Impedance
xxx: Don't Care

Notes:

1) When the write protect switch is in protect-mode, the WP output signal is "HIGH" and write operations (including attribute memory) are not allowed.
2) A0-A11 are attribute memory addresses. Addresses after A12 are not decoded, so care should be taken.

14.2 AC Characteristics (VCC=4.5V~5.5V, Ta=0~60℃)

Testing Conditions

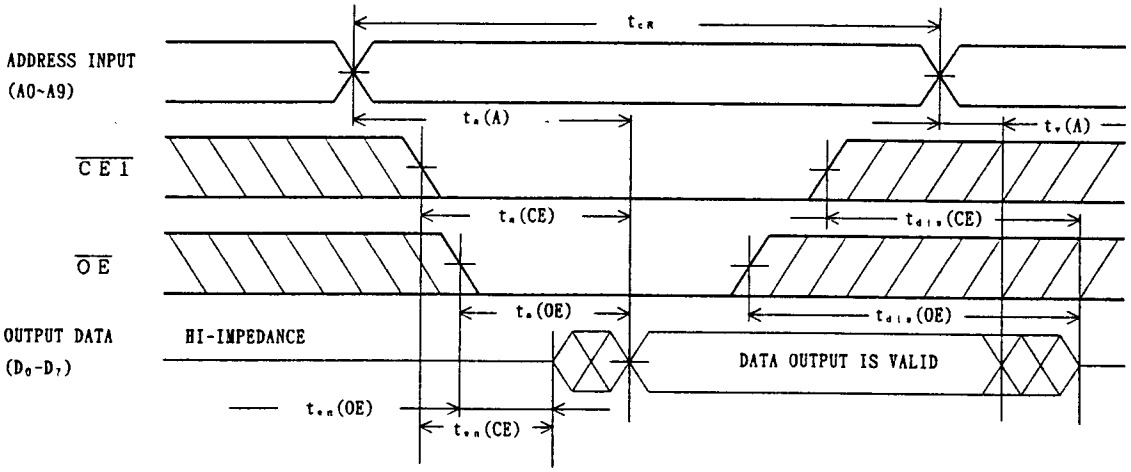
1)Input Pulse Level	:	0.8~3.5V
2)Input Rise/Fall Time	:	10ns
3)Input/Output Timing Reference Level	:	1.5V
4)Output Load Capacitance	:	1TTL+C_L (100pF) (including scope and jig capacitance)

14.3 Attribute Memory Read Cycle

(V_{CC}=4.5~5.5V, Ta=0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Read Cycle Time	t_{CR}	t_{cR}	300	–	ns
Address Access Time	t_{ACC}	t_a(A)	–	300	
Card Enable Access Time	t_{CE}	t_a(CE)	–	300	
Output Enable Access Time	t_{OE}	t_a(OE)	–	150	
Output Disable Time from $\overline{CE}$		t_{dis}(CE)	–	100	
Output Disable Time from $\overline{OE}$	t_{DF}	t_{dis}(OE)	–	100	
Output Enable Time from $\overline{CE}$		t_{en}(CE)	5	–	
Output Enable Time from $\overline{OE}$		t_{en}(OE)	5	–	
Data Valid from Add Change	t_{OH}	t_v(A)	0	–	

○ Attribute Memory Read Cycle



Note: 1. To read attribute memory, $\overline{REG}$="LOW", $\overline{WE}$="HIGH" and either $\overline{CE2}$="LOW" or else $\overline{CE2}$="HIGH" and A0="LOW".

2. The output data becomes valid when last interval, ta(A), ta(CE) or ta(OE) have concluded.

14.4 Attribute Memory Write Cycle

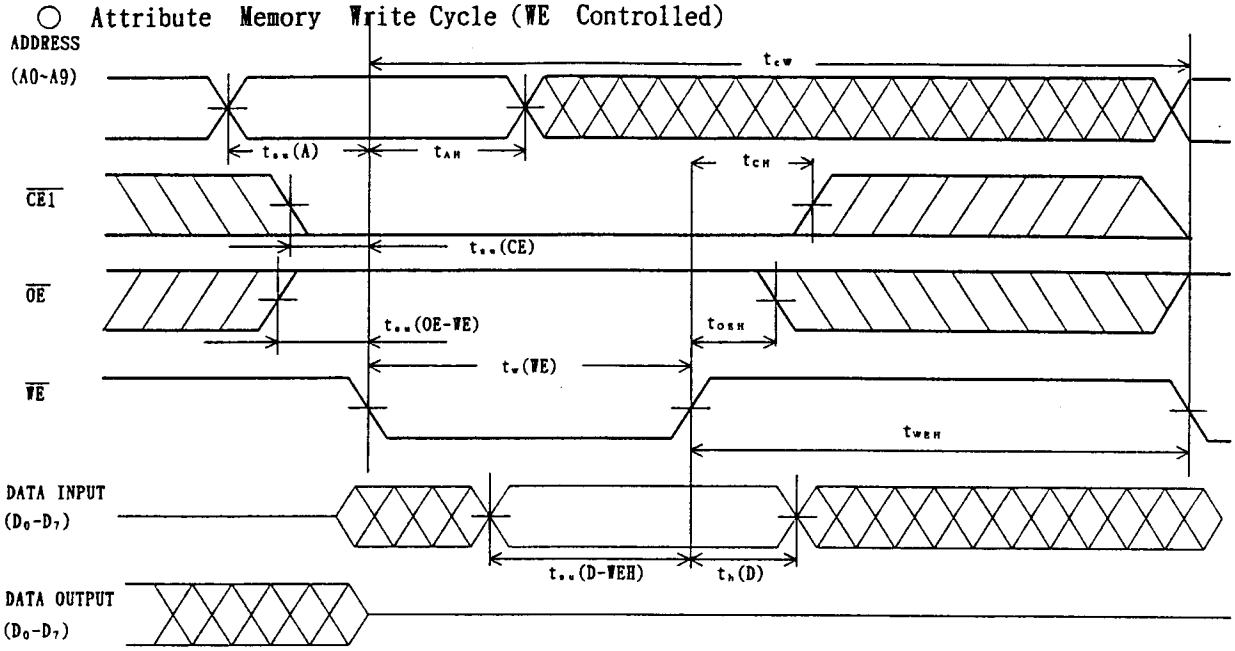
$\overline{WE}$ Controlled (V_{CC}=4.5V～5.5V, Ta=0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time	t_{WC}	t_{cw}	10	−	ms
Write Pulse Width	t_{WP}	t_{w}(WE)	180	−	ns
Address Setup Time	t_{AS}	t_{su}(A)	10	−	
Data Setup Time for $\overline{WE}$	t_{DS}	t_{su}(D-WEH)	100	−	
Crad Enable Setup Time	t_{CES}	t_{su}(CE)	0	−	
Output Enable Setup Time	t_{OES}	t_{su}(OE-WE)	45	−	
Address Hold Time	t_{AH}		260	−	
Write Hold Time	t_{CH}		0	−	
Output Enable Hold Time	t_{OEH}		70	−	
$\overline{WE}$ HIGH Hold Time	t_{WEH}		9.9	−	ms
Data Hold Time	t_{DH}	t_{h}(D)	80	−	ns

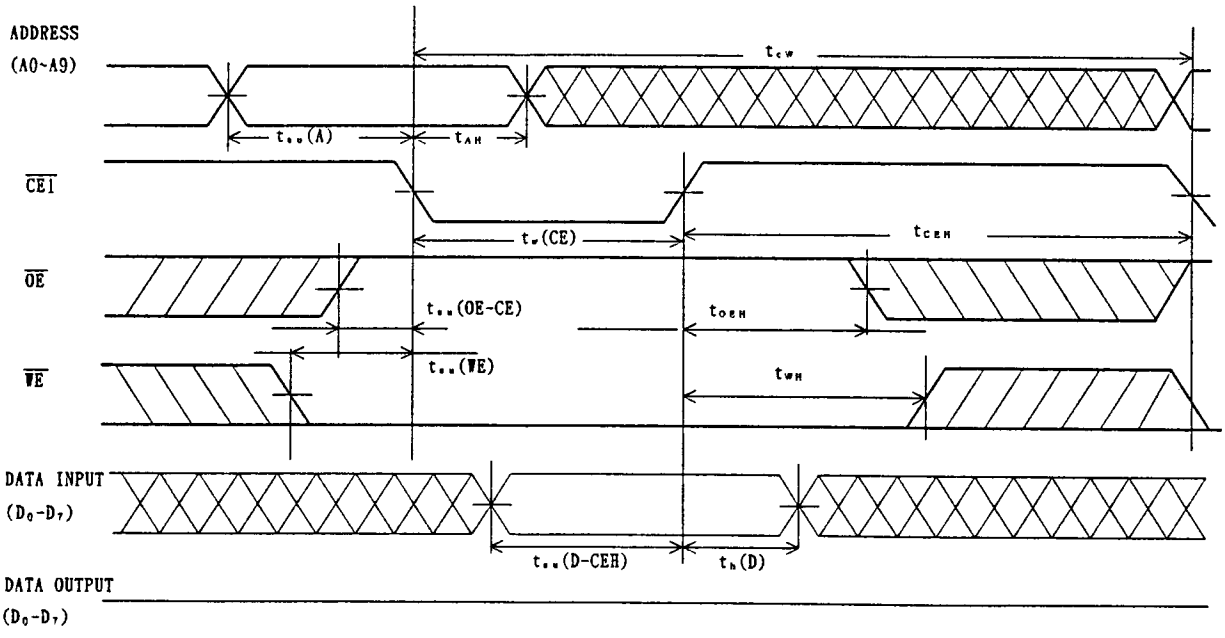
$\overline{CE}$ Controlled (V_{CC}=4.5V～5.5V, Ta=0~60℃)

PARAMETER	SYMBOL	SYMBOL(PCMCIA)	MIN	MAX	UNIT
Write Cycle Time	t_{WC}	t_{cw}	10	−	ms
Write Pulse Width	t_{WP}	t_{w}(CE)	210	−	ns
Address Setup Time	t_{AS}	t_{su}(A)	10	−	
Data Setup Time for $\overline{CE}$	t_{DS}	t_{su}(D-CEH)	100	−	
Write Enable Setup Time	t_{WES}	t_{su}(WE)	0	−	
Output Enable Setup Time	t_{OES}	t_{su}(OE-CE)	45	−	
Address Hold Time	t_{AH}		260	−	
Write Hold Time	t_{WH}		0	−	
Output Enable Hold Time	t_{OEH}		70	−	
$\overline{CE}$ HIGH Hold Time	t_{CEH}		9.9	−	ms
Data Hold Time	t_{DH}	t_{h}(D)	80	−	ns

○ Attribute Memory Write Cycle ($\overline{WE}$ Controlled)



○ Attribute Memory Write Cycle ($\overline{CE}$ Controlled)



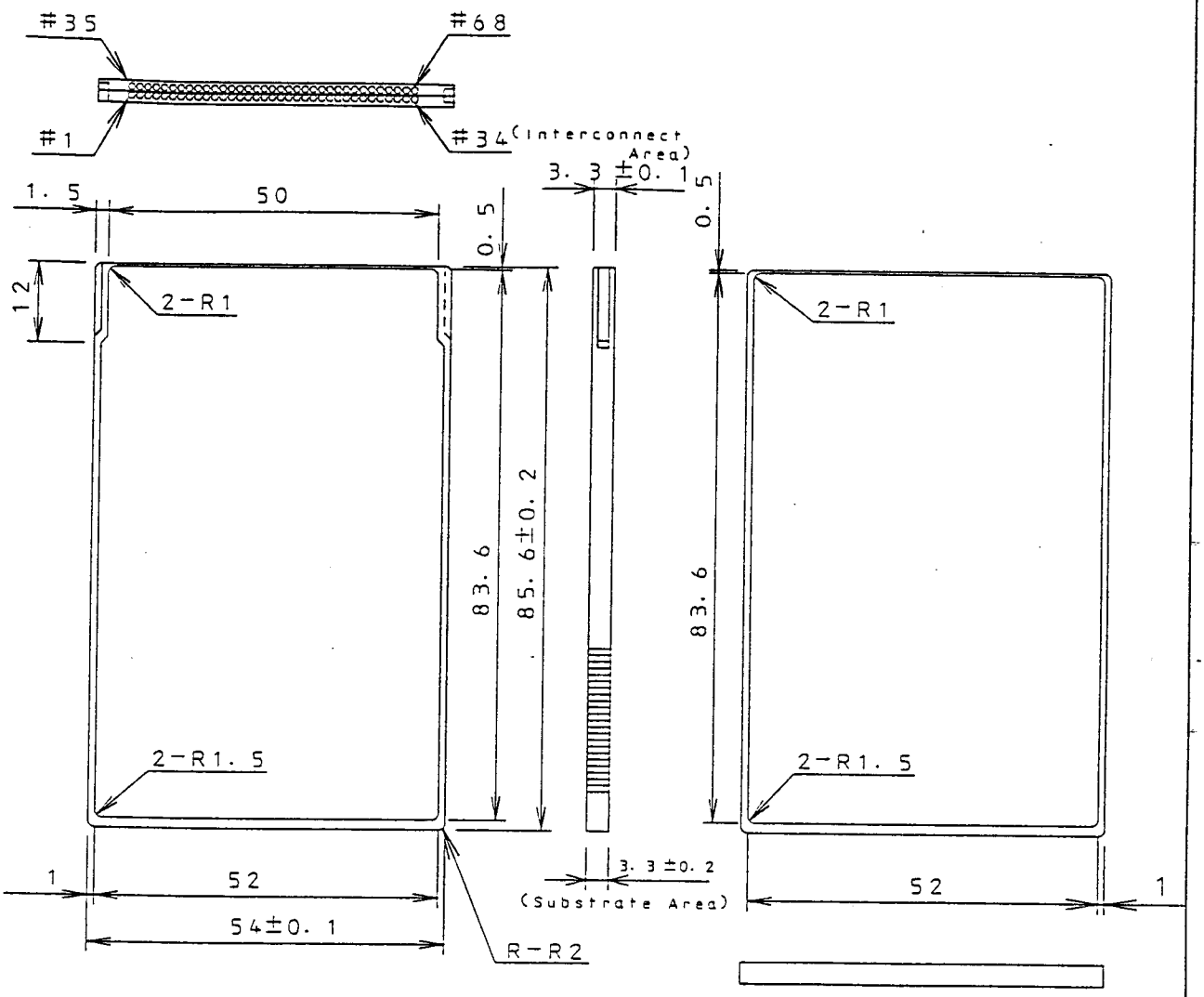
Note: To write attribute memory, $\overline{REG}$="LOW" and either $\overline{CE2}$="LOW" or else $\overline{CE2}$="HIGH" and A0="LOW".

15. Specification Changes
Specifications may be changed upon discussion and agreement between both parties.

16. Othes Precautions
- Permanent damage occures if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

SHARP

17. External Diagrams



FRONT

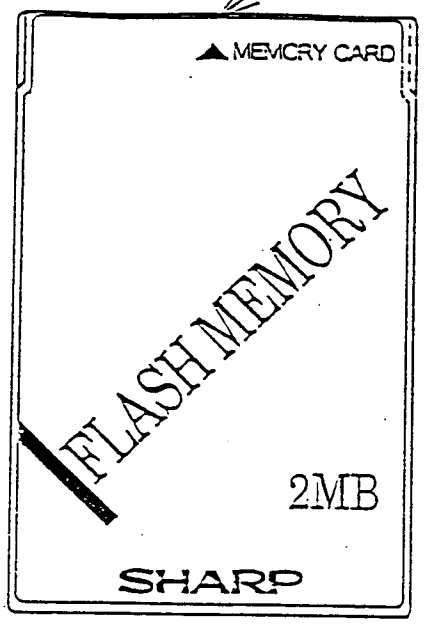
BACK

APPLICABLE MODEL		SCALE 1/1	UNIT mm	2			
				1			
				CH. DATE	REVISE	CHARGE	
THICKNESS		MATERIAL	FINISH	NAME	MEMORY CARD EXTERNAL DIAGRAM		
DATE	1994.11.16						
DESIGN / DRAW / TRACE / CHECK / APPROVE		Memory Card Business Project Team			PCMCIA Rel. 2.0 TYPE1		
		IC GROUP SHARP CORPORATION		DRAWING NO.	IMC001-A102		

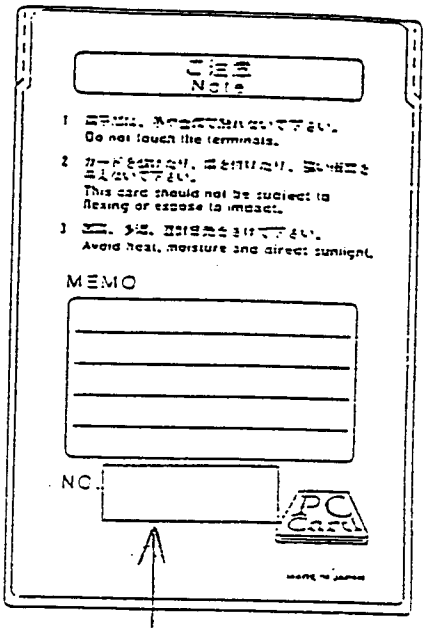
SHARP

19. EXTERNAL APPEARANCES

CONNECTOR SIDE



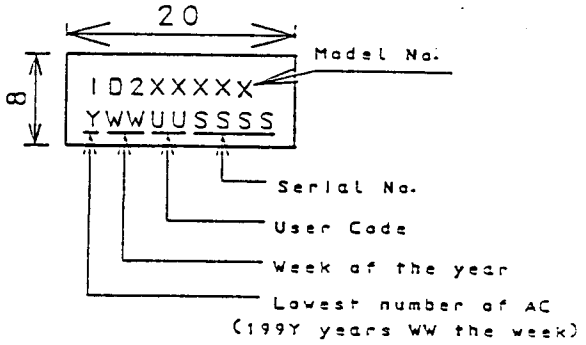
FRONT PANEL



LABELING POSITION

BACK PANEL

LABEL SIZE AND DENOTATIONS

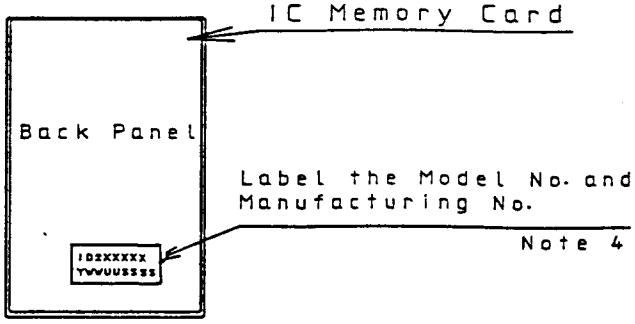


APPLICABLE MODEL		SCALE	UNIT			
			mm	CH. DATE	REVISE	CHARGE
THICKNESS	DEFFERENCE	MATERIAL	FINISH	NAME		
DATE 1995. 10. 10						
		MEMORY CARD BUSINESS PROJECT TEAM				
		INTEGRATED CIRCUITS GROUP				
		SHARP CORPORATION		DRAWING NO.		

SHARP

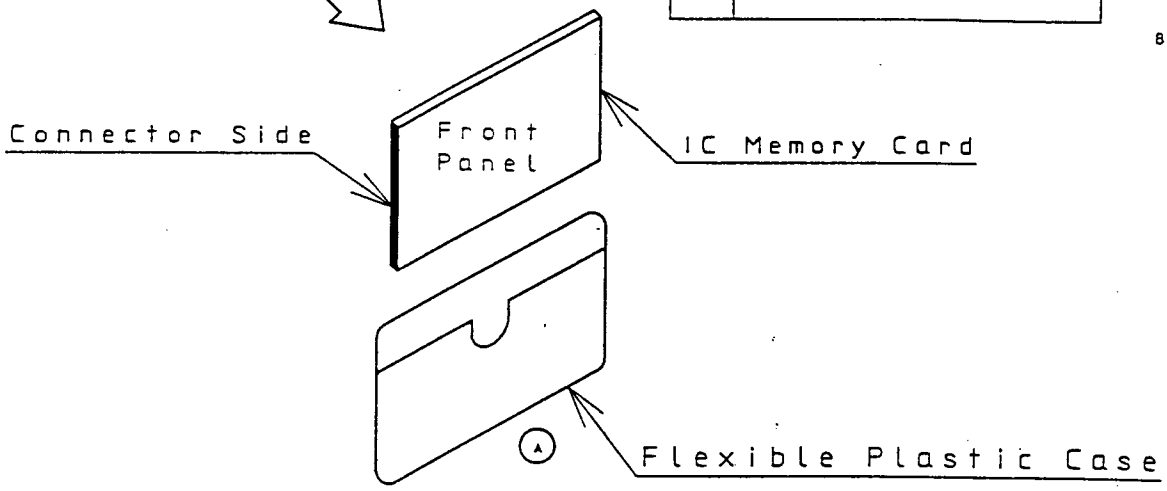
18. PACKING SPECIFICATION

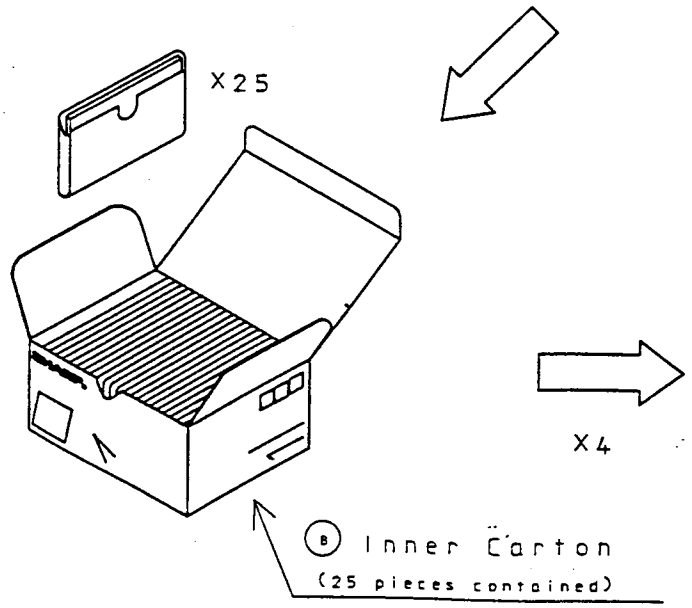
Connector Side

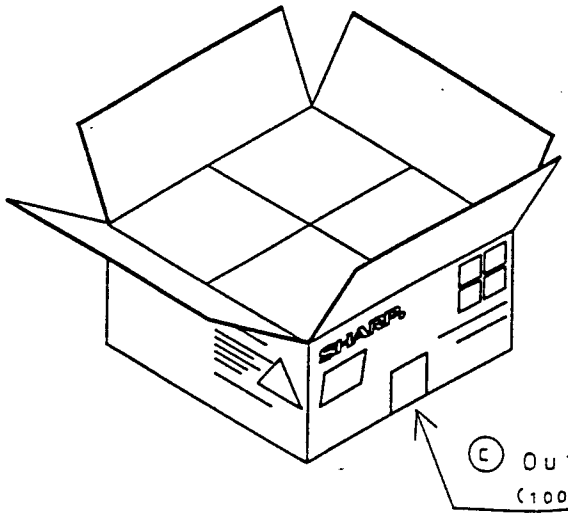


Parts List

	Parts Name
A	Flexible Plastic Case
B	Inner Carton (25 pieces contained)
C	Outer Carton (100 pieces contained)
D	Outer Case (400 pieces contained)







Packing Sp

1. Label the Model of the card.
2. Each memory car (The frontside is released. and point. so that t in the figure.)
3. The inner carto case. (Note 1.)
4. The product nam are either writ on the label wh
5. The outer carto
6. The product nam are either writ on the label wh
7. The outer carto contains 4 outer
8. The product nam are either writ label which is

Packing Specification

1. Label the Model No. and Manufuring No. on the back panel of the card.

2. Each memory card is contained in the flexible plastic case. (The frontside of the card comes to the place where the card is released, and the connector side is placed against to this point, so that the connector is not touched by finger, as shown in the figure.)

3. The inner carton contains 25 pieces of the card with the case. (Note 1.)

4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is then attached on inner carton.

5. The outer carton contains 4 inner cartons. (Note 2.)

6. The product name, lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is then attached on the outer carton.

7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)

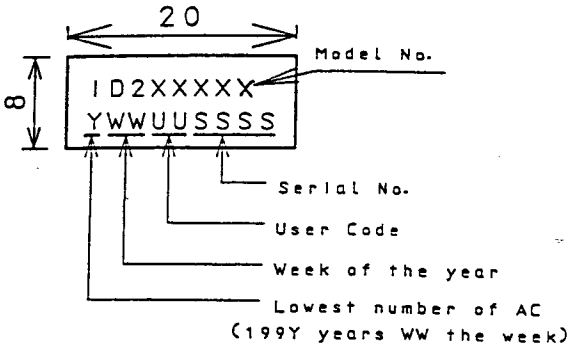
8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is then attached on the case.

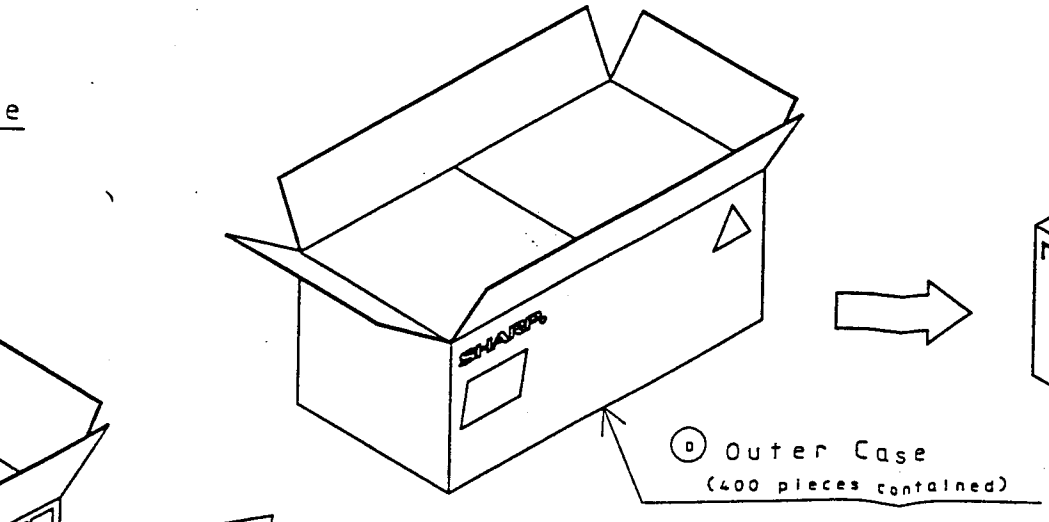
Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.

3. The other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.

4. Size of label and denotations are following. [unit: mm]





Ⓓ Outer Case
(400 pieces contained)

X4

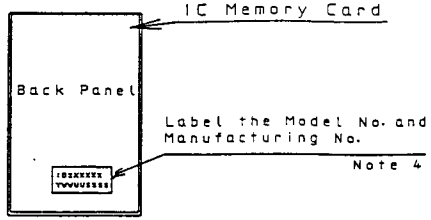
Ⓒ Outer Carton
(100 pieces contained)

APPLICABLE MODEL	ID2XXXXX	SCALE	UNIT mm	⚠2 ⚠1	CH. DATE	REVISE / CHARGE
THICKNESS	DEFFERENCE	MATERIAL	FINISH	NAME	ID2XXXXX Packing Specification	
DATE	1995. 10. 10	MEMORY CARD BUSINESS PROJECT TEAM				
K. Hashimoto / T. Sasaki / S. Shintani		INTEGRATED CIRCUITS GROUP				
		SHARP CORPORATION		DRAWING NO.	IMC025-J300	

SHARP

18. PACKING SPECIFICATION

Connector Side



Parts List

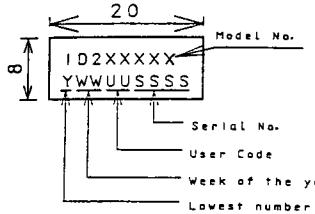
	Parts Name
A	Flexible Plastic Case
B	Inner Carton (25 pieces contained)
C	Outer Carton (100 pieces contained)
D	Outer Case (400 pieces contained)

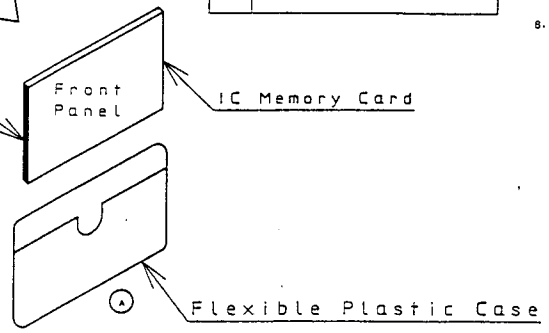
Packing Specification

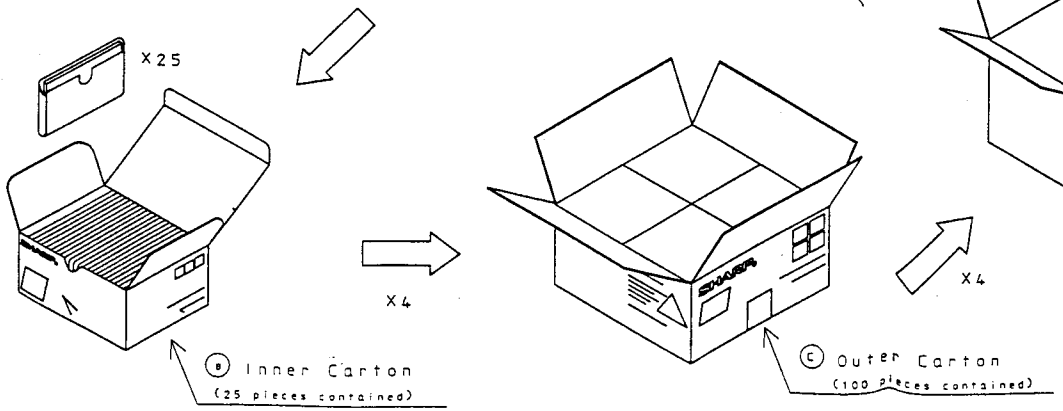
1. Label the Model No. and Manufuring No. on the back panel of the card.
2. Each memory card is contained in the flexible plastic case. (The front side of the card comes to the place where the card is released, and the connector side is placed against to this point, so that the connector is not touched by finger, as shown in the figure.)
3. The inner carton contains 25 pieces of the card with the case. (Note 1.)
4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is then attached on inner carton.
5. The outer carton contains 4 inner cartons. (Note 2.)
6. The product name, Lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is then attached on the outer carton.
7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)
8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is then attached on the case.

Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.
3. The other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.
4. Size of label and denotations are following. [unit:mm]







APPLICABLE MODEL	ID2XXXXX		SCALE	UNIT	A		
				mm	A		
THICKNESS	DEFFERENCE		MATERIAL	FINISH	CH. DATE	REVISE	CHARGE
					NAME	ID2XXXXX Packing Specification	
DATE	1995. 10. 10		MEMORY CARD BUSINESS PROJECT TEAM				
			INTEGRATED CIRCUITS GROUP				
			SHARP CORPORATION		DRAWING NO.	IMC025-J300	

FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX ID244D01 2M PC Card