PRELIMINARY DATASHEET

PROGRAMMABLE CLOCK GENERATOR IDT5P49V5901

Description

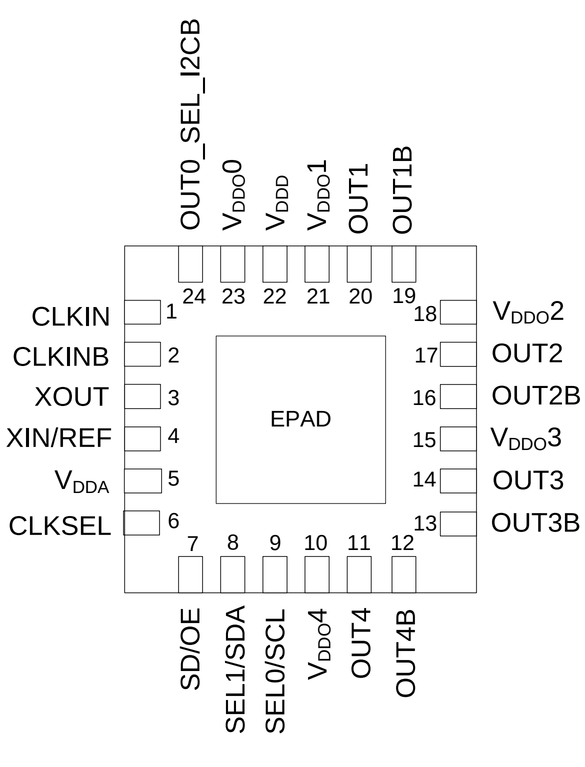
The IDT5P49V5901 is a programmable clock generator intended for high performance consumer, networking, industrial, computing, and data-communications applications. Configurations may be stored in on-chip One-Time Programmable (OTP) memory or changed using I^2C interface. This is IDTs fifth generation of programmable clock technology (VersaClock® 5).

The frequencies are generated from a single reference clock. The reference clock can come from one of the two redundant clock inputs. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation.

Two select pins allow up to 4 different configurations to be programmed and accessible using processor GPIOs or bootstrapping. The different selections may be used for different operating modes (full function, partial function, partial power-down), regional standards (US, Japan, Europe) or system production margin testing.

The device may be configured to use one of two I^2C addresses to allow multiple devices to be used in a system.

Pin Assignment

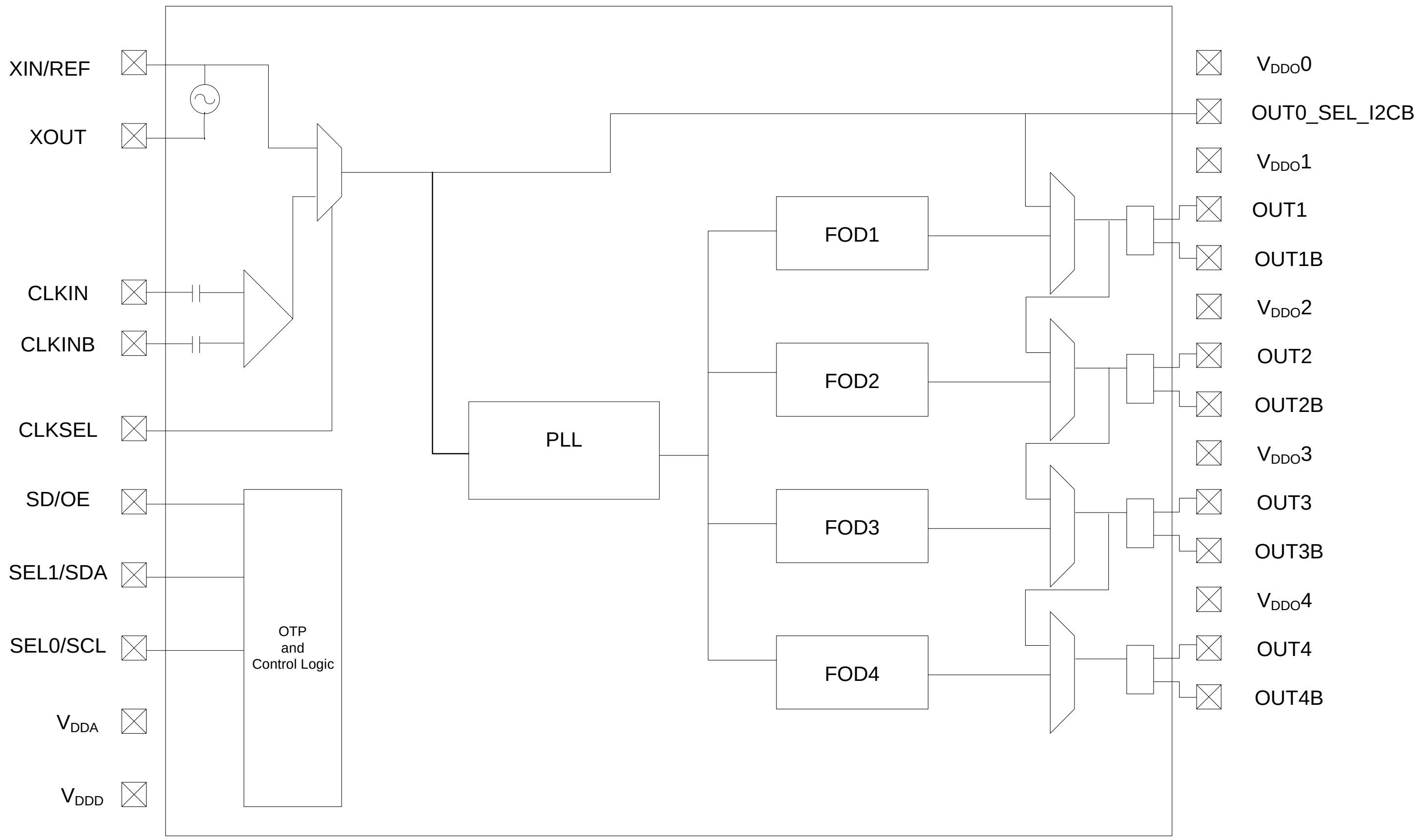


24-pin VFQFPN

Features

- Generates up to four independent output frequencies
- High performance, low phase noise PLL, <0.7 ps RMS typical phase jitter on outputs:
  - PCIe Gen1, 2, 3 compliant clock capability
  - USB 3.0 compliant clock capability
  - 1 GbE and 10 GbE
- Four fractional output dividers (FODs)
- Independent Spread Spectrum capability on each output pair
- Four banks of internal non-volatile in-system programmable or factory programmable OTP memory
- I^2C serial programming interface
- One reference LVCMOS output clock
- Four universal output pairs:
  - Each configurable as one differential output pair or two LVCMOS outputs
- I/O Standards:
  - Single-ended I/Os: 1.8V to 3.3V LVCMOS
  - Differential I/Os - LVPECL, LVDS and HCSL
- Input frequency ranges:
  - LVCMOS Reference Clock Input (XIN/REF) – 5MHz to 200MHz
  - LVDS, LVPECL, HCSL Differential Clock Input (CLKIN, CLKINB) – 5MHz to 350MHz
  - Crystal frequency range: 8MHz to 40MHz
- Output frequency ranges:
  - LVCMOS Clock Outputs – 5MHz to 200MHz
  - LVDS, LVPECL, HCSL Differential Clock Outputs – 5MHz to 350MHz
- Individually selectable output voltage (1.8V, 2.5V, 3.3V) for each output pair
- Redundant clock inputs with manual switchover
- Programmable loop bandwidth
- Programmable slew rate control
- Programmable crystal load capacitance
- Individual output enable/disable
- Power-down mode
- 1.8V, 2.5V or 3.3V core V_{DDD}, V_{DDA}
- Available in 24-pin VFQFPN 4mm x 4mm package
- -40° to +85°C industrial temperature operation

Functional Block Diagram



Applications

- Ethernet switch/router
- PCI Express 1.0/2.1/3.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Table 1: Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Internal Pull-down	Differential clock input. Weak 100kohms internal pull-down.
2	CLKINB	Input	Internal Pull-down	Complementary differential clock input. Weak 100kohms internal pull-down.
3	XOUT	Input		Crystal Oscillator interface output.
4	XIN/REF	Input		Crystal Oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is 1.2V max.Refer to the section “Overdriving the XIN/REF Interface”.
5	V_{DDA}	Power		Analog functions power supply pin.Connect to 1.8V to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
6	CLKSEL	Input	Internal Pull-down	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default) 1 = CLKIN, CLKINB CLKSEL Polarity can be changed by I2C programming as shown in Table 4.
7	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when pin is configured as OE (Default is active LOW.) Weak internal pull down resistor. When configured as SD, device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low, depending on the programming bits as shown in the SD/OE Pin Function Truth table.
8	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I^2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
9	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I^2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
10	$V_{DDO}4$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT4/OUT4B.
11	OUT4	Output		Output Clock 4. Please refer to the Output Drivers section for more details.
12	OUT4B	Output		Complementary Output Clock 4. Please refer to the Output Drivers section for more details.
13	OUT3B	Output		Complementary Output Clock 3. Please refer to the Output Drivers section for more details.
14	OUT3	Output		Output Clock 3. Please refer to the Output Drivers section for more details.
15	$V_{DDO}3$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3/OUT3B.
16	OUT2B	Output		Complementary Output Clock 2. Please refer to the Output Drivers section for more details.
17	OUT2	Output		Output Clock 2. Please refer to the Output Drivers section for more details.
18	$V_{DDO}2$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
19	OUT1B	Output		Complementary Output Clock 1. Please refer to the Output Drivers section for more details.
20	OUT1	Output		Output Clock 1. Please refer to the Output Drivers section for more details.
21	$V_{DDO}1$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.

Number	Name	Type		Description
22	V_{DDD}	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
23	$V_{DDO}0$	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0_SEL_I2CB	Input/ Output	Internal Pull-down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull up (10kohms) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I^2C interface. After power up, the pin acts as a LVCMOS reference output.
ePAD	GND	GND		Connect to ground pad.

PLL Features and Descriptions

Spread Spectrum

To help reduce electromagnetic interference (EMI), the IDT5P49V5901 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The IDT5P49V5901 implements spread spectrum using the Fractional-N output divide, to achieve controllable modulation rate and spreading magnitude. The Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread.

Table 2: Loop Filter

PLL loop bandwidth range depends on the input reference frequency (Fref) and can be set between the loop bandwidth range as shown in the table below.

Input Reference Frequency–Fref (MHz)	Loop Bandwidth Min (kHz)	Loop Bandwidth Max (kHz)
5	40	126
350	300	1000

Table 3: Configuration Table

This table shows the SEL1, SEL0 settings to select the configuration stored in OTP. Four configurations can be stored in OTP. These can be factory programmed or user programmed.

SEL1	SEL0	CONFIG
0	0	0
0	1	1
1	0	2
1	1	3

SEL0,1 pins must be changed within ~100ns of each other and then the device left alone for 1ms. Refer to OUT0_SEL_I2CB pin description.

Table 4: Input Clock Select

Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB
CLKSEL Polarity can be changed by I^2C programming as shown in Table 4.

PRIMSRC	CLKSEL	Source
0	0	XIN/REF
0	1	CLKIN, CLKINB
1	0	CLKIN, CLKINB
1	1	XIN/REF

PRIMSRC is bit 1 of Register 0x13.

Reference Clock Input Pins and Selection

The IDT5P49V5901 supports up to two clock inputs. One of the clock inputs (XIN/ REF) can be driven by either an external crystal or a reference clock. The second clock input (CLKIN, CLKINB) can only be driven from an external reference clock. The CLKSEL pin selects the input clock between either XTAL/REF or (CLKIN, CLKINB).

Either clock input can be set as the primary clock. The primary clock designation is to establish which is the main reference clock to the PLL. The non-primary clock is designated as the secondary clock in case the primary clock goes absent and a backup is needed. The PRIMSRC bit determines which clock input will be selected as primary clock. When PRIMSRC bit is "0", XIN/REF is selected as the primary clock, and when "1", (CLKIN, CLKINB) as the primary clock.

The two external reference clocks can be manually selected using the CLKSEL pin. The SM bits must be set to "0x" for manual switchover which is detailed in Manual Switchover Mode section.

Crystal Input (XIN/REF)

The crystal used should be a fundamental mode quartz crystal; overtone crystals should not be used.

When a crystal is connected across the XIN/REF and XOUT pins it is important to set the internal tuning capacitor values correctly to achieve the highest clock frequency accuracy. There are two equal valued tuning capacitors, one for XIN and one for XOUT and each capacitor provides a parallel path for its associated pin to the internal ground of the device. The values of these capacitors are composed of a fixed capacity plus a variable capacity set with the XTAL[5:0] register through the I^2C interface. Adjustment of the crystal tuning capacitors through firmware allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

XTAL[5:0] Tuning Capacitor Characteristics

Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.5	0	16

The AC voltages on the XIN and XOUT pins are out of phase, which allows the two XTAL[5:0] tuning capacitors to be translated into a single equivalent parallel load capacitor across XIN and XOUT by dividing the tuning capacity by two. Adding the fixed parallel capacity and the effective parallel tuning capacity set by XTAL results in the total parallel tuning capacity provided by the VersaClock.

XTAL load cap = 4.5pF + (XTAL[5:0]/2) (Eq. 1)

Equation 1 and the table of XTAL[5:0] tuning capacitor characteristics show that the parallel tuning capacitance can be set between 4.5pF to 12.5pF with a resolution of 0.25 pF. Consider two examples.

For a crystal CL= 8pF, where CL is the parallel capacity specified by the crystal vendor that sets the crystal frequency to the nominal value. Under the assumptions that the stray capacity between the crystal leads on the circuit board is zero and that no external tuning caps are placed on the crystal leads, then the internal parallel tuning capacity is equal to the load capacity presented to the crystal by the VersaClock. Equation 1 allows for the direct calculation that XTAL[5:0] = 14 (dec).

In the case of a CL = 18pF crystal, the maximum internal parallel tuning cap of 12.5pF will be insufficient. Two external tuning capacitors must be added to the circuit board, one on each of XIN and XOUT. For maximum turning range, set the value of the two external tuning caps so that XTAL[5:0] is set in the middle of its range, 8pF/2 = 4pF and XTAL[5:0] = 32 (dec). Using Equation 1, the internal tuning capacitor is set for 4.5pF + 4pF = 8.5pF. The remaining tuning capacity is 18pF - 8.5pF = 9.5pF. Each external tuning capacitor is then 2*9.5pF = 19pF.

The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements.

Manual Switchover Mode

When SM[1:0] is "0x", the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. The primary and secondary clock source setting is determined by the PRIMSRC bit. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

OTP Interface

The IDT5P49V5901 can also store its configuration in an internal OTP. The contents of the device's internal programming registers can be saved to the OTP by setting burn_start (W114[3]) to high and can be loaded back to the internal programming registers by setting usr_rd_start(W114[0]) to high.

To initiate a save or restore using I^2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the IDT5P49V5901 will not generate Acknowledge bits. The IDT5P49V5901 will acknowledge the instructions after it has completed execution of them. During that time, the I^2C bus should be interpreted as busy by all other users of the bus.

On power-up of the IDT5P49V5901, an automatic restore is performed to load the OTP contents into the internal programming registers. The IDT5P49V5901 will be ready to accept a programming instruction once it acknowledges its 7-bit I^2C address.

Availability of Primary and Secondary I^2C addresses to allow programming for multiple devices in a system. The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. *VersaClock 5 Programming Guide* provides detailed I^2C programming guidelines and register map.

SD/OE Pin Function

The polarity of the SD/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (W16[1]). When SP is “0” (default), the pin becomes active LOW and when SP is “1”, the pin becomes active HIGH. The SD/OE pin can be configured as either to shutdown the PLL or to enable/disable the outputs. The SH bit controls the configuration of the SD/OE pin The SH bit needs to be high for SD/OE pin to be configured as SD.

When configured as SD, device is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs are driven high/low.

Table 5: SD/OE Pin Function Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	0	0	x	x	Tri-state[2]
0	0	1	0	x	Output active
0	0	1	1	0	Output active
0	0	1	1	1	Output driven High Low
0	1	0	x	x	Tri-state[2]
0	1	1	0	x	Output active
0	1	1	1	0	Output driven High Low
0	1	1	1	1	Output active
1	0	0	x	0	Tri-state[2]
1	0	1	0	0	Output active
1	0	1	1	0	Output active
1	1	0	x	0	Tri-state[2]
1	1	1	0	0	Output active
1	1	1	1	0	Output driven High Low
1	x	x	x	1	Output driven High Low [1]

Note 1 : Global Shutdown
Note 2 : Tri-state regardless of OEn bits

Output Divides

Each output divide block has a synchronizing POR pulse to provide startup alignment between outputs divides. This allows alignment of outputs for low skew performance. This low skew would also be realized between outputs that are both integer divides from the VCO frequency. This phase alignment works when using configuration with SEL1, SEL0. For I^2C programming, I^2C reset is required.

An output divide bypass mode (divide by 1) will also be provided, to allow multiple buffered reference outputs.

Each of the four output divides are comprised of a 12 bit integer counter, and a 24 bit fractional counter. The output divide can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate a clock frequency accurate to 50 ppb.

Each of the output divides also have structures capable of independently generating spread spectrum modulation on the frequency output.

The Output Divide also has the capability to apply a spread modulation to the output frequency. Independent of output frequency, a triangle wave modulation between 30 and 63kHz may be generated.

For all outputs, there is a bypass mode, to allow the output to behave as a buffered copy of the input.

Output Skew

For outputs that share a common output divide value, there will be the ability to skew outputs by quadrature values to minimize interaction on the PCB. The skew on each output can be adjusted from 0 to 360. Contact IDT for programmable skew adjustments.

Output Drivers

The OUT1 to OUT4 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels

The operating voltage ranges of each output is determined by its independent output power pin (V_{DDO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential HCSL, LVPECL operation, and 1. 8V, 2.5V, or 3.3V are supported for LVCMOS and differential LVDS operation.

Each output may be enabled or disabled by register bits. When disabled an output will be in a logic 0 state as determined by the programming bit table shown on page 6.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the OUTx and OUTxB outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the OUTx and OUTxB pins. The OUTx and OUTxB outputs can be selected to be phase-aligned with each other or inverted relative to one another by register programming bits. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Device Hardware Configuration

The IDT5P49V5901 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with up to 4 complete device configuration.

These configurations can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The IDT5P49V5901 has an internal power-up reset (POR) circuit. The POR circuit will remain active for a maximum of 10ms after device power-up.

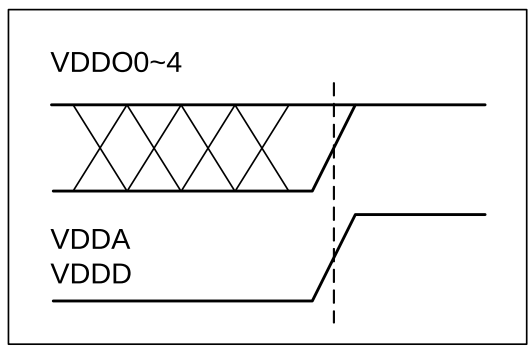
Upon internal POR circuit expiring, the device will exit reset and begin self-configuration.

The device will load internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the selected source and begin operation.

Power Up Ramp Sequence

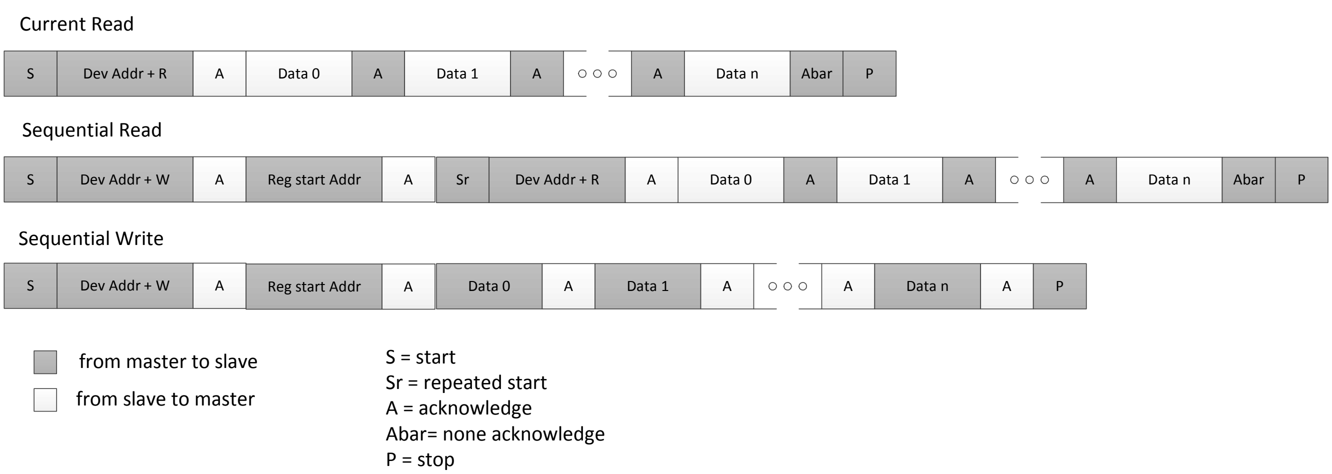
VDDA and VDDD must ramp up together. VDDO0~4 must ramp up before, or concurrently with, VDDA and VDDD. All power supply pins must be connected to a power rail even if the output is unused. All power supplies must ramp in a linear fashion and ramp monotonically.



I²C Mode Operation

The device acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.



I²C Slave Read and Write Cycle Sequencing

Table 6: I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level		$0.7xV_{DDD}$			V
V_{IL}	Input LOW Level				$0.3xV_{DDD}$	V
V_{HYS}	Hysteresis of Inputs		$0.05xV_{DDD}$			V
I_{IN}	Input Leakage Current				±1.0	μA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

Table 7: I²C Bus AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Table 8: Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P49V5901. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.465V
Inputs XIN/REF CLKIN, CLKINB Other inputs	 0V to 1.2V voltage swing 0V to 1.2V voltage swing single-ended -0.5V to V_{DDD}
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO}+ 0.5V
Outputs, I_O (SDA)	10mA
Package Thermal Impedance, θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

Table 9: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDOX}	Power supply voltage for supporting 1.8V outputs	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for supporting 2.5V outputs	2.375	2.5	2.625	V
V_{DDOX}	Power supply voltage for supporting 3.3V outputs	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVCMOS only)			15	pF
F_{IN}	External reference crystal	8		40	MHz
	External reference clock CLKIN, CLKINB	5		350	
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Note: V_{DDO}1, V_{DDO}2, V_{DDO}3, and V_{DDO}4 must be powered on either before or simultaneously with V_{DDD}, V_{DDA} and V_{DDO}0.

Table 10: Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance (T_A = +25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (CLKIN, CLKINB, CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL)		3	7	pF
Pull-down Resistor	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB		100		kΩ
R_{OUT}	LVCMOS Output Driver Impedance (V_{DDO} = 1.8V, 2.5V, 3.3V)		17		Ω
XIN/REF, XOUT	Programmable input capacitance at XIN/REF and XOUT	0		8	pF

Table 11: Crystal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Units
Mode of Oscillation		Fundamental			
Frequency		8		40	MHz
Equivalent Series Resistance (ESR)			10	100	Ω
Shunt Capacitance			2	7	pF
Load Capacitance (C_L)		8	12	18	pF
Maximum Crystal Drive Level			100		μW

Table 12: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Iddcore[3]	Core Supply Current	100 MHz on all outputs, 25 MHz REFCLK		30		mA
Iddox	Output Buffer Supply Current	LVPECL, 350 MHz, 3.3V V_{DDOX}		61		mA
		LVPECL, 350 MHz, 2.5V V_{DDOX}		52		mA
		LVDS, 350 MHz, 3.3V V_{DDOX}		18		mA
		LVDS, 350 MHz, 2.5V V_{DDOX}		17		mA
		LVDS, 350 MHz, 1.8V V_{DDOX}		16		mA
		HCSL, 250 MHz, 3.3V V_{DDOX}, 2 pF load		29		mA
		HCSL, 250 MHz, 2.5V V_{DDOX}, 2 pF load		28		mA
		LVCMOS, 50 MHz, 3.3V V_{DDOX}, [1,2]		16		mA
		LVCMOS, 50 MHz, 2.5V V_{DDOX}, [1,2]		14		mA
		LVCMOS, 50 MHz, 1.8V V_{DDOX}, [1,2]		12		mA
		LVCMOS, 200 MHz, 3.3V V_{DDOX}, [1,2]		36		mA
		LVCMOS, 200 MHz, 2.5V V_{DDOX}, [1,2]		27		mA
		LVCMOS, 200 MHz, 1.8V V_{DDOX}, [1,2]		16		mA
Iddpd	Core Power Down Current	SD asserted, I^2C Programming		5		mA

1.Single CMOS driver active.
2.Measured into a 5” 50 Ohm trace with 2 pF load.
3. Iddcore = IddA + IddD, no loads.

Table 13: Electrical Characteristics – Differential Clock Input Parameters [1,2] (Supply Voltage V_{DDA}, V_{DDD}, $V_{DDO}0$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage–CLKIN, CLKINB	Single-ended input	0.55		1.7	V
V_{IL}	Input LOW Voltage–CLKIN, CLKINB	Single-ended input	GND - 0.3		0.4	V
V_{SWING}	Input Amplitude - CLKIN, CLKINB	Peak to Peak value, single-ended	200		1200	mV
dv/dt	Input Slew Rate - CLKIN, CLKINB	Measured differentially	0.4		8	V/ns
I_{IL}	Input Leakage Low Current	V_{IN} = GND	-5		5	µA
I_{IH}	Input Leakage High Current	V_{IN} = 1.7V			20	µA
d_{TIN}	Input Duty Cycle	Measurement from differential waveform	45		55	%

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.

Table 14: DC Electrical Characteristics for 3.3V LVCMOS (V_{DDO} = 3.3V±5%, TA = -40°C to +85°C) [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -15mA	2.4		V_{DDO}	V
V_{OL}	Output LOW Voltage	I_{OL} = 15mA			0.4	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDO} = 3.465V			5	µA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	2		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	GND - 0.3		0.8	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	2		$V_{DDO}0$ + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V

1. See “Recommended Operating Conditions” table.

Table 15: DC Electrical Characteristics for 2.5V LVCMOS (V_{DDO} = 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA	0.7xV_{DDO}			V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA			0.4	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDO} = 2.625V			5	μA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	1.7		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	GND - 0.3		0.8	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	1.7		V_{DDO}0 + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V

Table 16: DC Electrical Characteristics for 1.8V LVCMOS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	IOH = -8mA	0.7 xV_{DDO}		V_{DDO}	V
V_{OL}	Output LOW Voltage	IOL = 8mA			0.25 x V_{DDO}	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDO} = 1.89V			5	μA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	0.65 * V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	GND - 0.3		0.35 * V_{DDD}	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	0.65 * V_{DDO}		V_{DDO}0 + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V

Table 17: DC Electrical Characteristics for LVDS (V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.125	1.25	1.375	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

Table 18: DC Electrical Characteristics for LVDS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	0.8	0.875	0.95	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

Table 19: DC Electrical Characteristics for LVPECL (V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output Voltage HIGH, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.19		V_{DDO} - 0.69	V
V_{OL}	Output Voltage LOW, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.94		V_{DDO} - 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.55		0.993	V

Table 20: Electrical Characteristics – DIF 0.7V Low Power HCSL Differential Outputs (V_{DDO} = 3.3V±5%, 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
dV/dt	Slew Rate	Scope averaging on	1		4	V/ns	1,2,3
V_{HIGH}	Voltage High	Statistical measurement on single-ended signal using oscilloscope math function (Scope averaging ON)	660		850	mV	1,6,7
V_{LOW}	Voltage Low		-150		150	mV	1,6
V_{MAX}	Maximum Voltage	Measurement on single-ended signal using absolute value (Scope averaging off)			1150	mV	1
V_{MIN}	Minimum Voltage		-300			mV	1
V_{SWING}	Voltage Swing	Scope averaging off	300			mV	1,2,6
V_{CROSS}	Crossing Voltage Value	Scope averaging off	250		550	mV	1,4,6
ΔV_{CROSS}	Crossing Voltage Variation	Scope averaging off			140	mV	1,5

1. Guaranteed by design and characterization. Not 100% tested in production
2. Measured from differential waveform.
3. Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
5. The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.
6. Measured from single-ended waveform.
7. Measured with scope averaging off, using statistics function. Variation is difference between min. and max.

Table 21: AC Timing Electrical Characteristics

(V_{DDO} = 3.3V+5% or 2.5V+5% or 1.8V ±5%, TA = -40°C to +85°C)
(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN} [1]	Input Frequency	Input frequency limit (XIN)	8		40	MHz
		Input frequency limit (REF)	5		200	MHz
		Input frequency limit (CLKIN, CLKINB)	5		350	MHz
f_{OUT}	Output Frequency	Single ended clock output limit (LVCMOS)	5		200	MHz
		Single ended reference clock output limit (LVCMOS)	5		150	
		Differential clock output limit (LVPECL/ LVDS/HCSL)	5		350	
f_{VCO}	VCO Frequency	VCO operating frequency range		2800		MHz
f_{PFD}	PFD Frequency	PFD operating frequency range	0.8[1]		100	MHz
f_{BW}	Loop Bandwidth	Input frequency = 25MHz	0.08		0.5	MHz
t2	Input Duty Cycle	Duty Cycle	45		55	%
t3	Output Duty Cycle	Measured at V_{DD}/2, all outputs except Reference output	45		55	%
		Measured at V_{DD}/2, Reference output (5MHz - 150MHz)	40		60	%
		Measured at V_{DD}/2, Reference output (150.1MHz - 200MHz)	35		70	%
t4 [2]	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (Output Load = 5 pF)		1.83		V/ns
	Slew Rate, SLEW[1:0] = 01	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (Output Load = 5 pF)		1.90		V/ns
	Slew Rate, SLEW[1:0] = 10	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (Output Load = 5 pF)		1.96		V/ns
	Slew Rate, SLEW[1:0] = 11	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (Output Load = 5 pF)		2.15		V/ns
t5	Rise Times	LVDS, 20% to 80%, single-ended		300		ps
	Fall Times	LVDS, 80% to 20%, single-ended		300		ps
	Rise Times	LVPECL, 20% to 80%, single-ended		400		ps
	Fall Times	LVPECL, 80% to 20%, single-ended		400		ps

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t6	Clock Jitter	Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs (1.8V to 3.3V nominal output voltage) OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		46		ps
		Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs (1.8 to 3.3V nominal output voltage) OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		74		ps
		RMS Phase Jitter (12kHz to 5MHz integration range) reference clock (OUT0), 25 MHz LVCMOS outputs (1.8 to 3.3V nominal output voltage). OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		0.5		ps
		RMS Phase Jitter (12kHz to 20MHz integration range) differential output, V_{DDO} = 3.465V, 25MHz crystal, 156.25MHz output frequency OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		0.75	1.5	ps
t7	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.		75		ps
t8 [3]	Lock Time	PLL lock time from power-up		10	20	ms
t9 [4]	Lock Time	PLL lock time from shutdown mode			2	ms

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from memory to PLL registers. It does not include memory programming/write time.
4. Actual PLL lock time depends on the loop configuration.

Table 22: PCI Express Jitter Specifications (V_{DDO} = 3.3V±5% or 2.5V±5%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	PCIe Industry Specification	Units	Notes
t_J (PCIe Gen1)	Phase Jitter Peak-to-Peak	*ƒ* = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		30		86	ps	1,4
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen2)	Phase Jitter RMS	*ƒ* = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		2.56		3.10	ps	2,4
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen2)	Phase Jitter RMS	*ƒ* = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.27		3.0	ps	2,4
t_{REFCLK_RMS} (PCIe Gen3)	Phase Jitter RMS	*ƒ* = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.8		1.0	ps	3,4

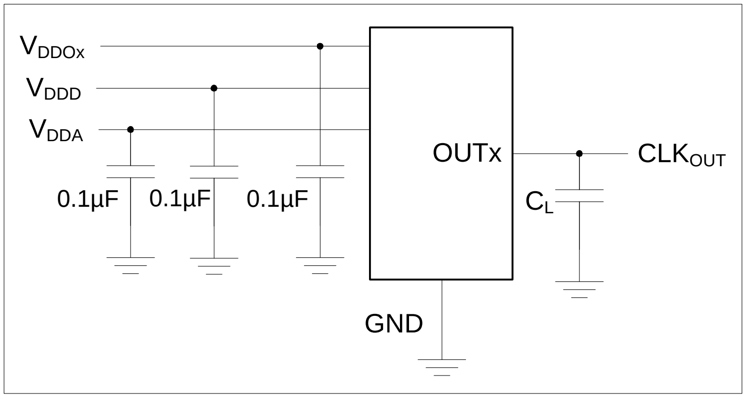
Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

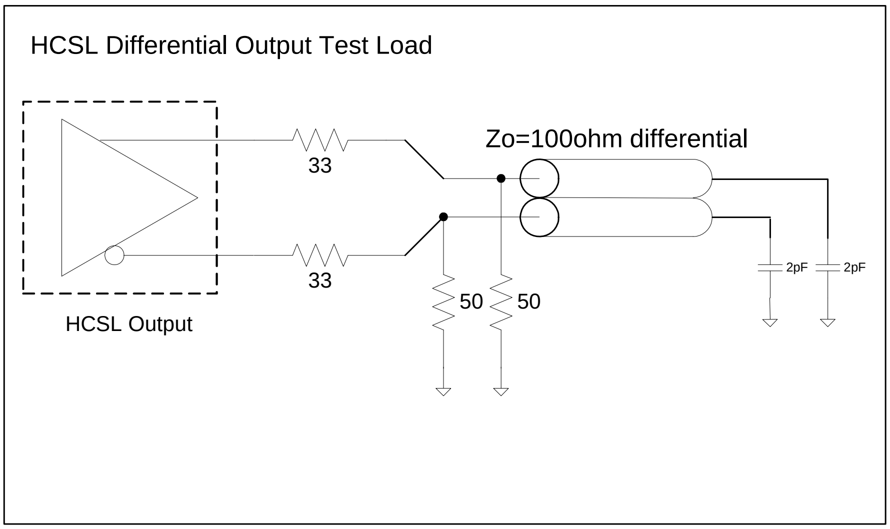
1. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1.
2. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
3. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov, 2010 specification, and is subject to change pending the final release version of the specification.
4. This parameter is guaranteed by characterization. Not tested in production.

Table 23: Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Output Frequency Range	5		300	MHz
f_{MOD}	Mod Frequency	Modulation Frequency	30 to 63			kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (programmable) - Center Spread	±0.25% to ±2.5%			$\%f_{OUT}$
		Amount of Spread Value (programmable) - Down Spread	-0.5% to -5%			

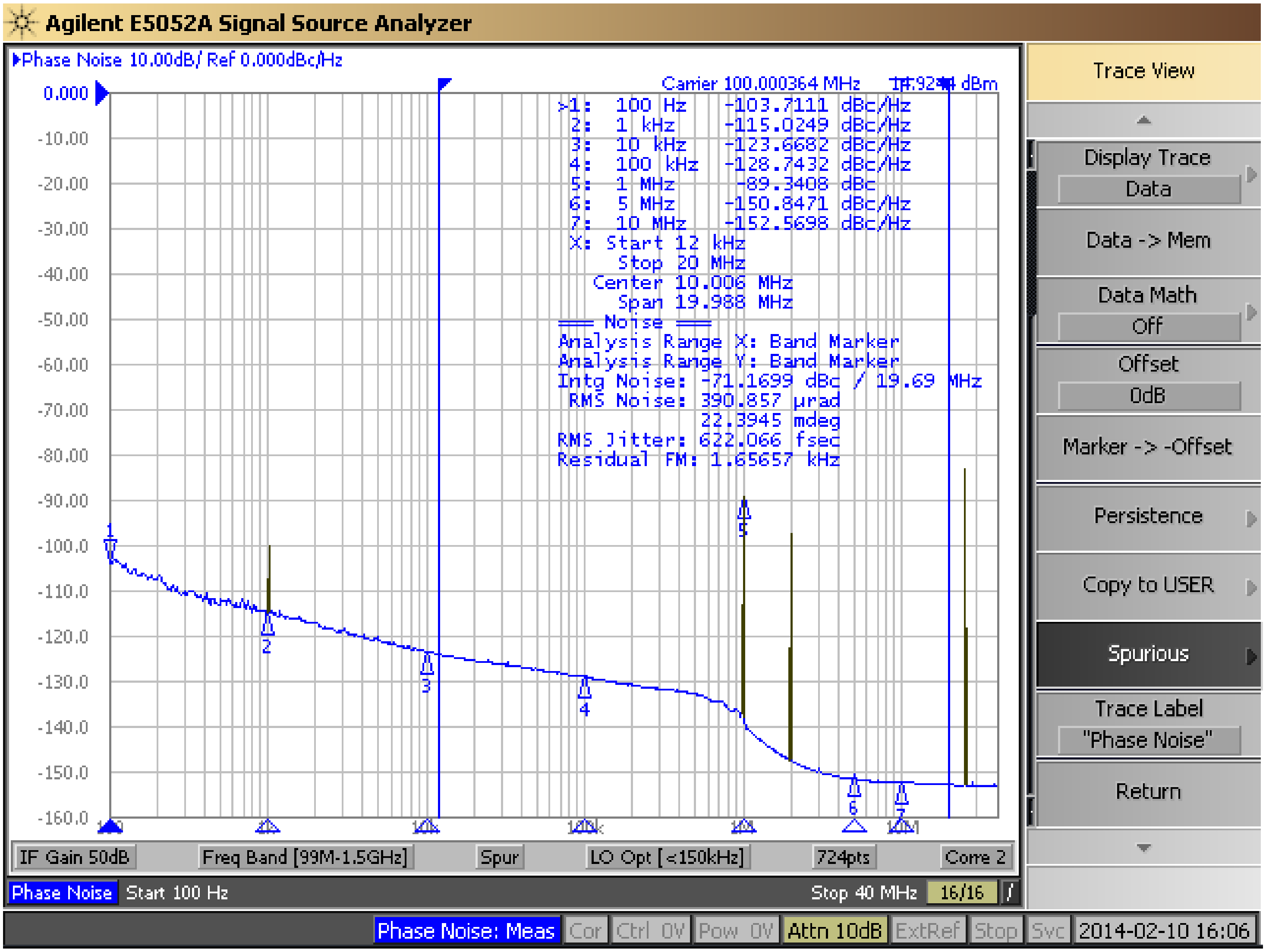
Test Circuits and Loads





Test Circuits and Loads for Outputs

Typical Phase Noise at 100MHz (3.3V, 25°C)



NOTE: All outputs operational at 100MHz, Phase Noise Plot with Spurs On.

IDT5P49V5901 Application Schematic

The following figure shows an example of IDT5P49V5901 application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. In this example, the device is operated at V_{DDD}, V_{DDA} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. A 12pF parallel resonant 8MHz to 40MHz crystal is used in this example. Different crystal frequencies may be used. The C1 = C2 = 5pF are recommended for frequency accuracy. If different crystal types are used, please consult IDT for recommendations. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

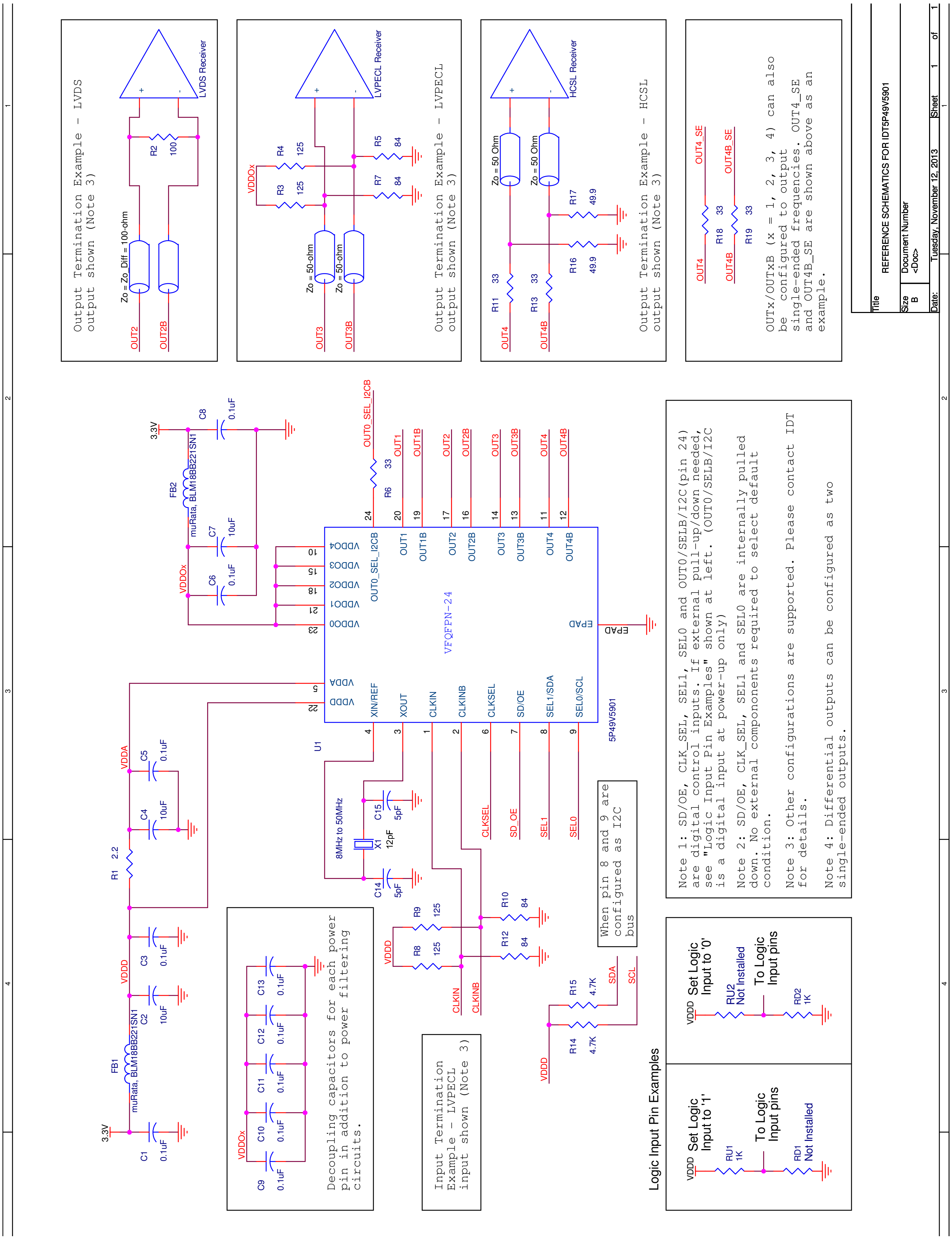
As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. IDT5P49V5901 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

IDT5P49V5901 Reference Schematic

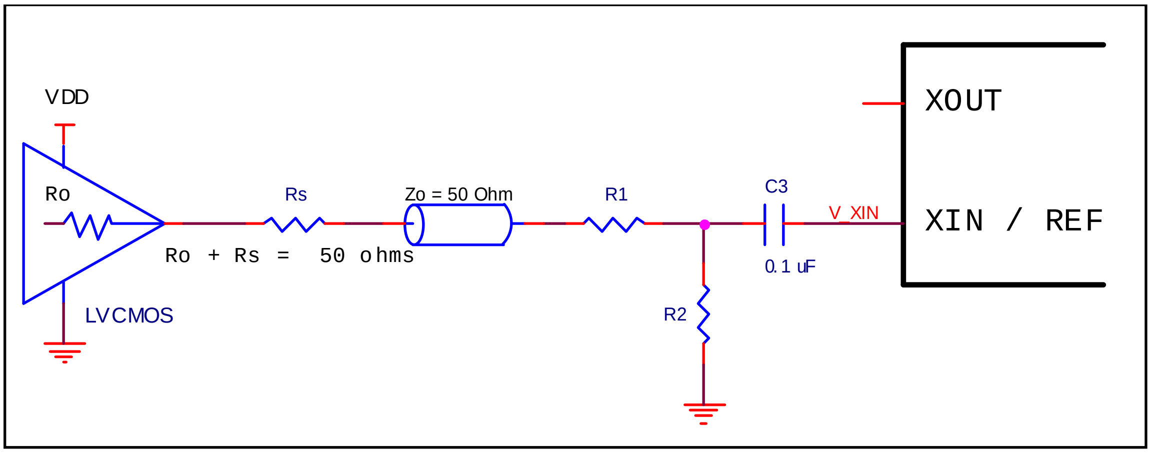


Overdriving the XIN/REF Interface

LVCMOS Driver

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V and the slew rate should not be less than 0.2V/ns. Figure General Diagram for LVCMOS Driver to XTAL Input Interface shows an example of the interface diagram for a LVCMOS driver.

This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that the clock level at XIN is less than the maximum value of 1.2V.



General Diagram for LVCMOS Driver to XTAL Input Interface

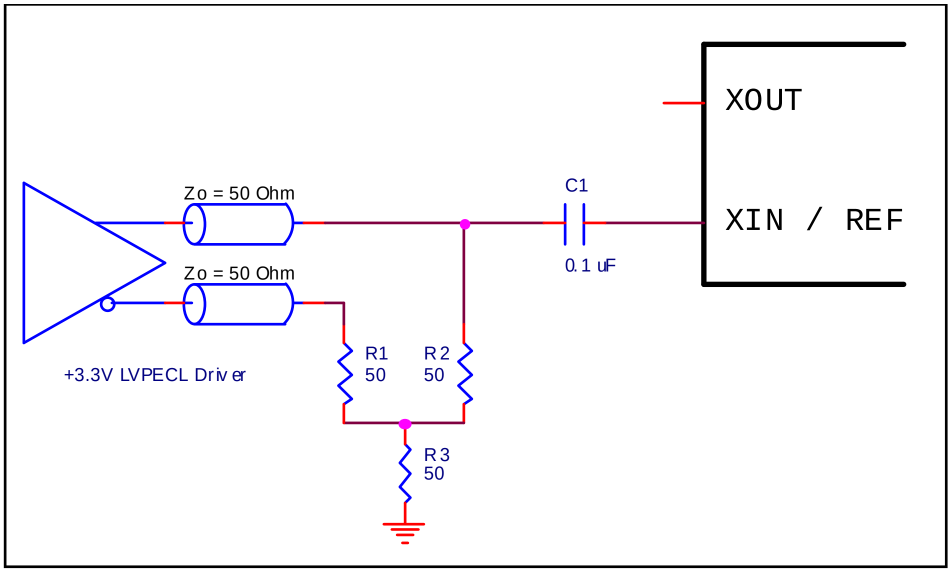
Table 24 *Nominal Voltage Divider Values vs LVCMOS VDD for XIN* shows resistor values that ensure the maximum drive level for the XIN/REF port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock VDDA and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the voltage divider attenuation as long as the minimum drive level is maintained over all tolerances. To assist this assessment, the total load on the driver is included in the table.

Table 24: Nominal Voltage Divider Values vs LVCMOS VDD for XIN

LVCMOS Driver VDD	Ro+Rs	R1	R2	V_XIN (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

LVPECL Driver

Figure General Diagram for LVPECL Driver to XTAL Input Interface shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

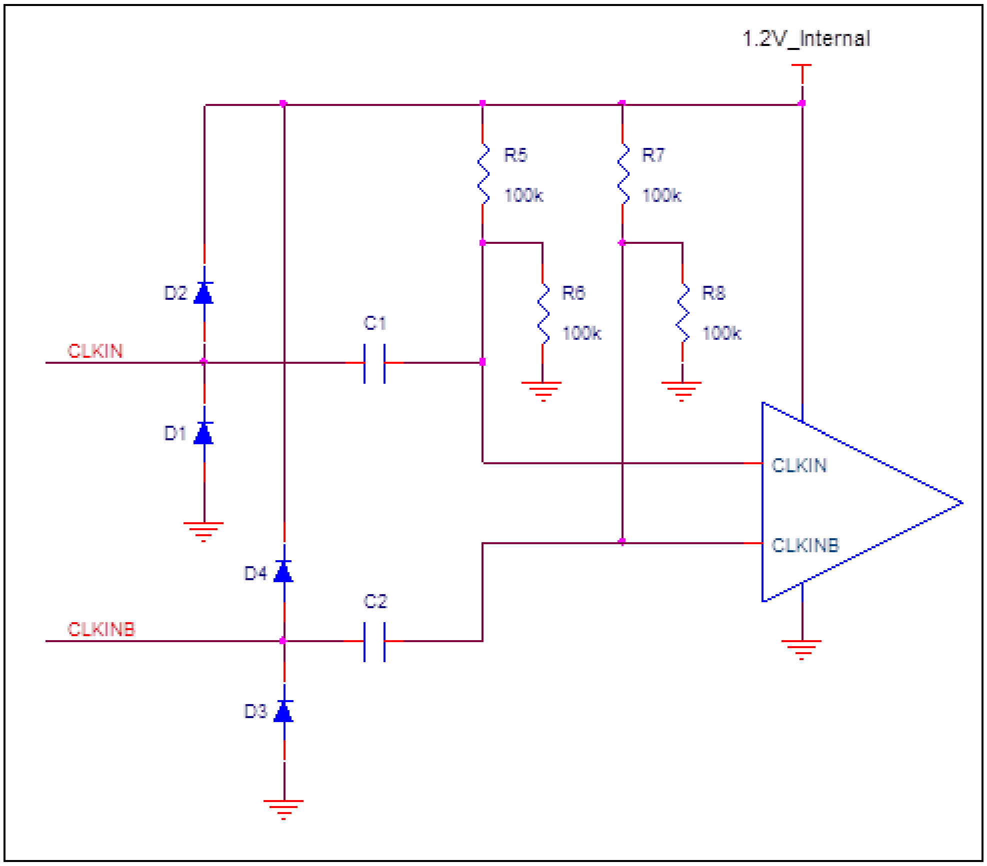


General Diagram for +3.3V LVPECL Driver to XTAL Input Interface

CLKIN Equivalent Schematic

Figure *CLKIN Equivalent Schematic* below shows the basis of the requirements on VIH max, VIL min and the 1200 mV p-p single ended Vswing maximum.

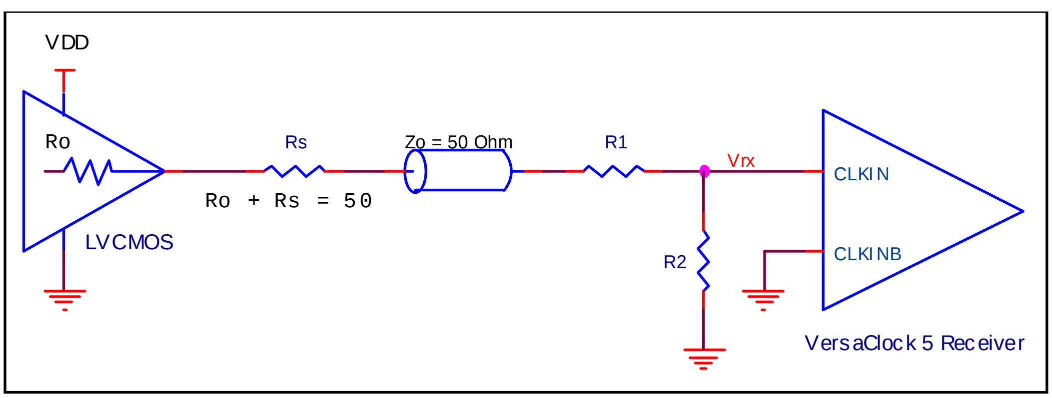
- The CLKIN and CLKINB Vih max spec comes from the cathode voltage on the input ESD diodes D2 and D4, which are referenced to the internal 1.2V supply. CLKIN or CLKINB voltages greater than 1.2V + 0.5V =1.7V will be clamped by these diodes. CLKIN and CLKINB input voltages less than -0.3V will be clamped by diodes D1 and D3.
- The 1.2V p-p maximum Vswing input requirement is determined by the internally regulated 1.2V supply for the actual clock receiver. This is the basis of the Vswing spec in Table 13.



CLKIN Equivalent Schematic

Wiring the Differential Input to Accept Single-Ended Levels

Figure *Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels* shows how a differential input can be wired to accept single ended levels. This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that Vrx p-p at CLKIN is less than the maximum value of 1.2V.



Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

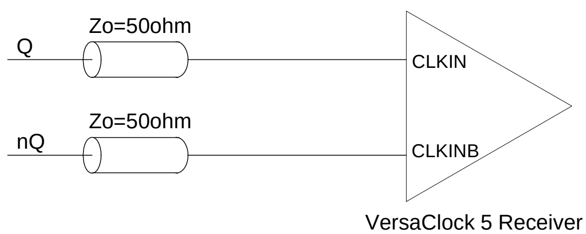
Table 25 *Nominal Voltage Divider Values vs Driver VDD* shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock Vddo_0 and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the R1-R2 divider. To assist this assessment, the total load on the driver is included in the table.

Table 25: Nominal Voltage Divider Values vs Driver VDD

LVCMOS Driver VDD	Ro+Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

HCSL Differential Clock Input Interface

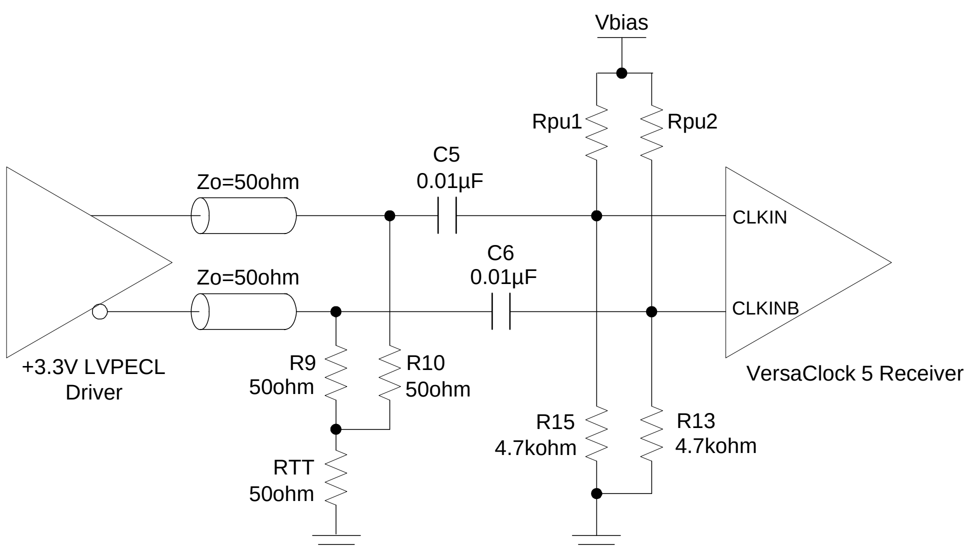
CLKIN/CLKINB will accept DC coupled HCSL signals.



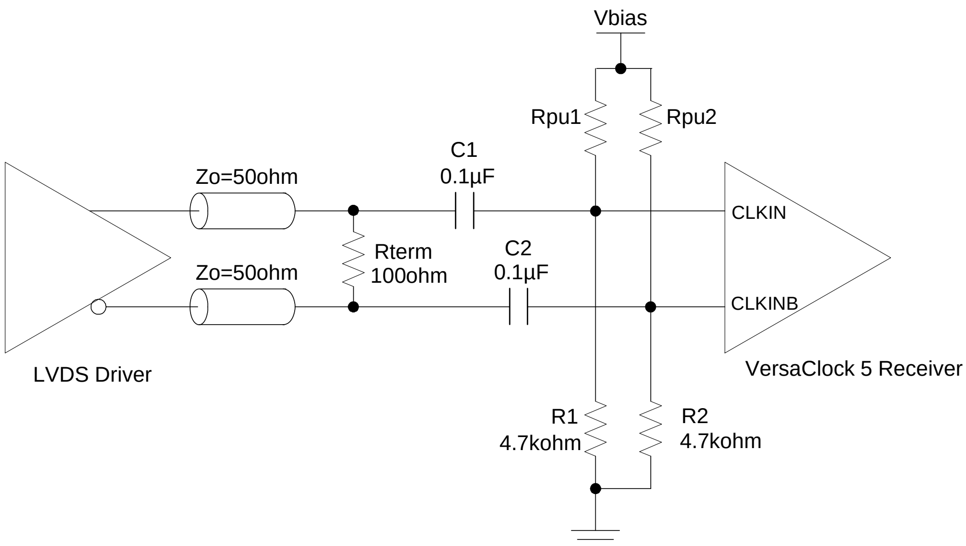
CLKIN, CLKINB Input Driven by an HCSL Driver

3.3V Differential LVPECL Clock Input Interface

The logic levels of 3.3V LVPECL and LVDS can exceed VIH max for the CLKIN/B pins. Therefore the LVPECL levels must be AC coupled to the VersaClock differential input and the DC bias restored with external voltage dividers. A single table of bias resistor values is provided below for both for 3.3V LVPECL and LVDS. Vbias can be VDDD, V_{DDOX} or any other available voltage at the VersaClock receiver that is most conveniently accessible in layout.



CLKIN, CLKINB Input Driven by a 3.3V LVPECL Driver



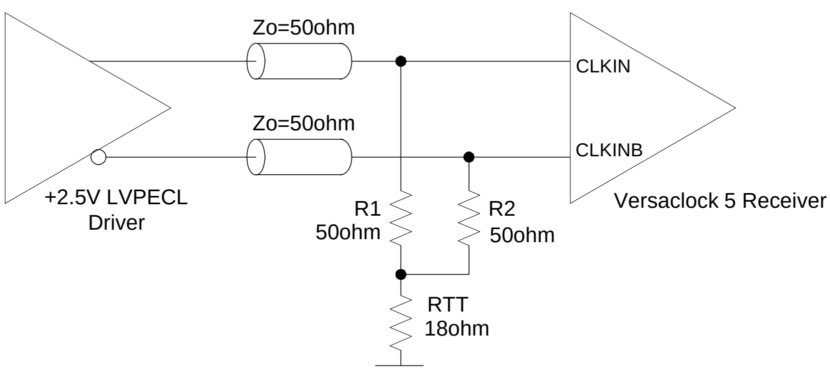
CLKIN, CLKINB Input Driven by an LVDS Driver

Table 26: Bias Resistors for 3.3V LVPECL and LVDS Drive to CLKIN/B

Vbias (V)	Rpu1/2 (kohm)	CLKIN/B Bias Voltage (V)
3.3	22	0.58
2.5	15	0.60
1.8	10	0.58

2.5V Differential LVPECL Clock Input Interface

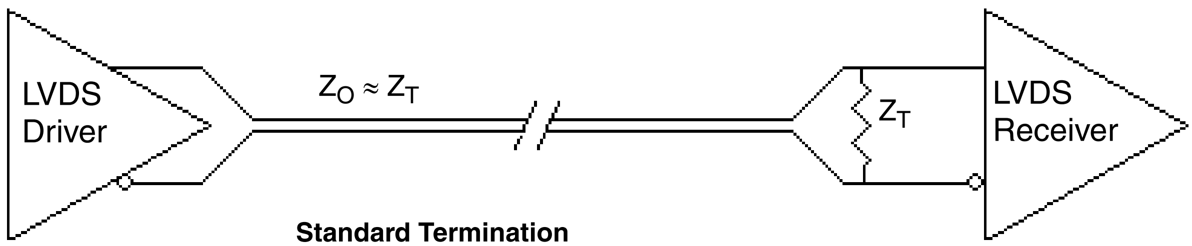
The maximum DC 2.5V LVPECL voltage meets the VIH max CLKIN requirement. Therefore 2.5V LVPECL can be connected directly to the CLKIN terminals without AC coupling



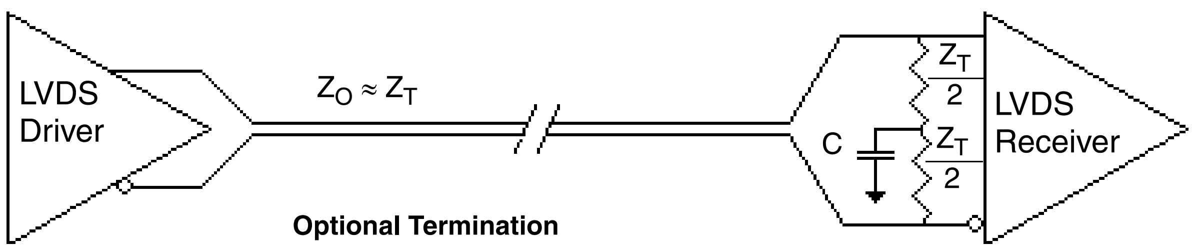
CLKIN, CLKINB Input Driven by a 2.5V LVPECL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω. and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω. differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the IDT LVDS output. If using a non-standard termination, it is recommended to contact IDT and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100 ohm shunt load. If AC coupling is required, the coupling caps must be placed between the 100 ohm shunt termination and the receiver. In this manner the termination of the LVDS output remains DC coupled



Standard Termination

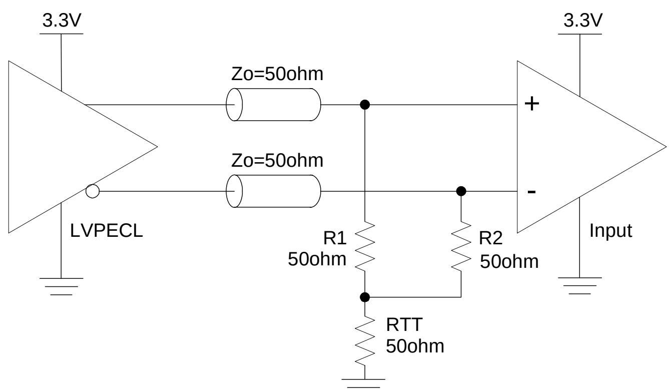


Optional Termination

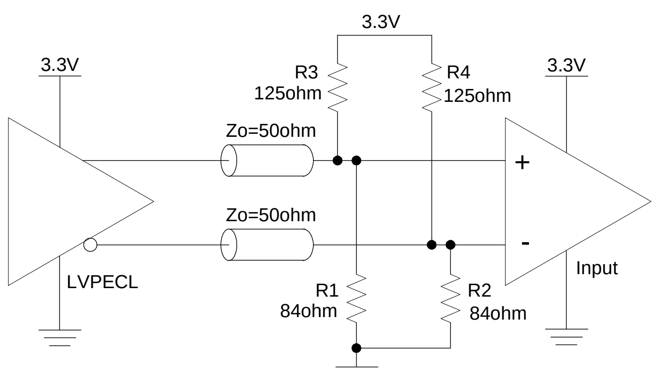
Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The figure below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



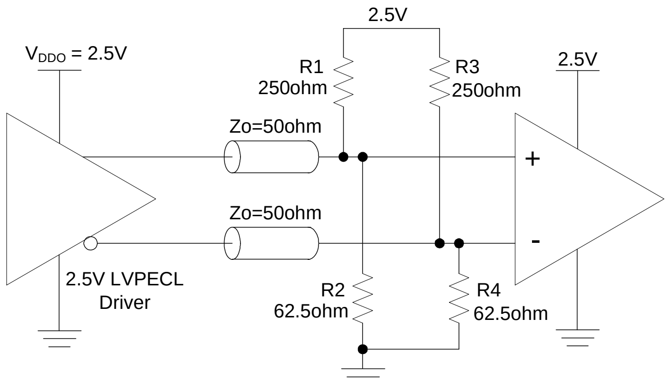
3.3V LVPECL Output Termination (1)



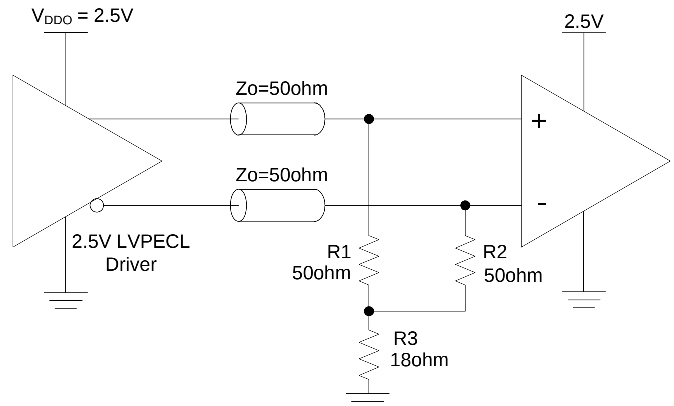
3.3V LVPECL Output Termination (2)

Termination for 2.5V LVPECL Outputs

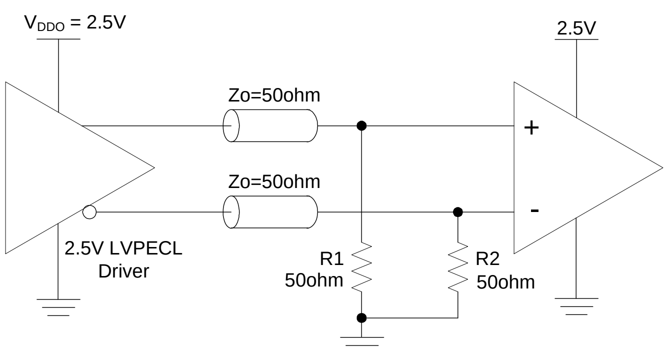
Figures *2.5V LVPECL Driver Termination Example (1) and (2)* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure *2.5V LVPECL Driver Termination Example (3)* can be eliminated and the termination is shown in example (2).



2.5V LVPECL Driver Termination Example (1)



2.5V LVPECL Driver Termination Example (3)



2.5V LVPECL Driver Termination Example (2)

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used Common Clock Architecture in which a copy of the reference clock is provided to both ends of the PCI Express Link.

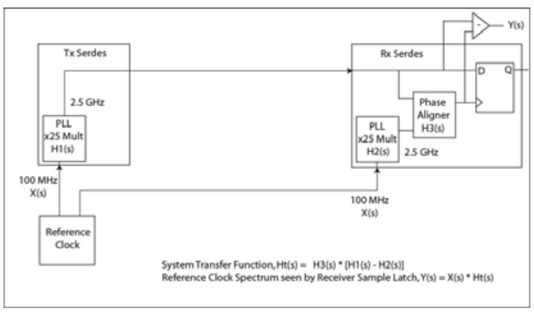
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

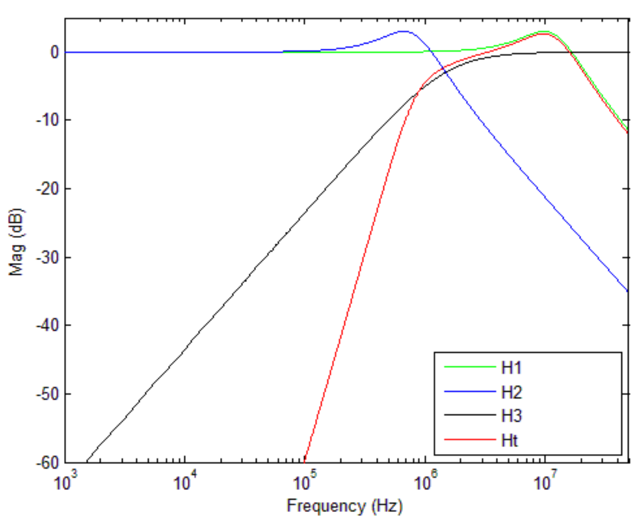
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



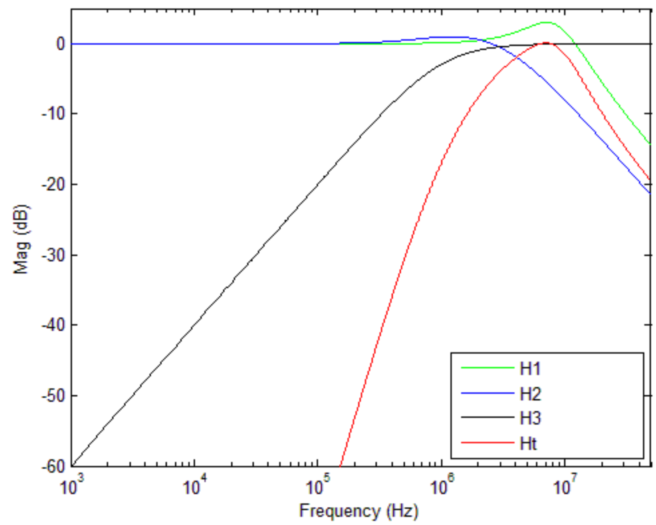
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

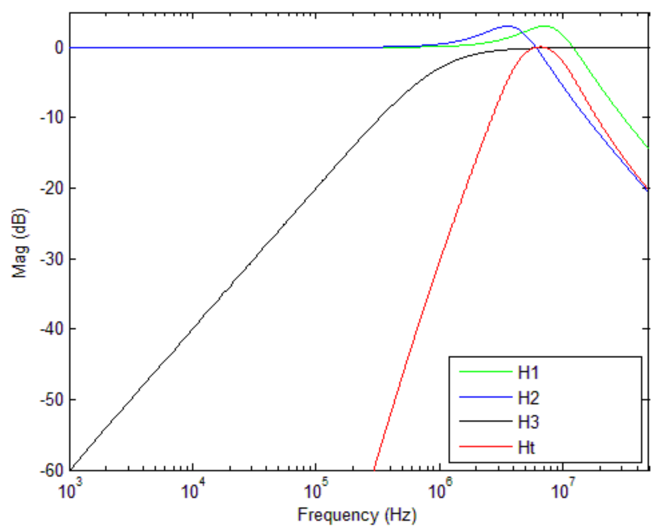


PCIe Gen1 Magnitude of Transfer Function

For PCI Express Gen2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

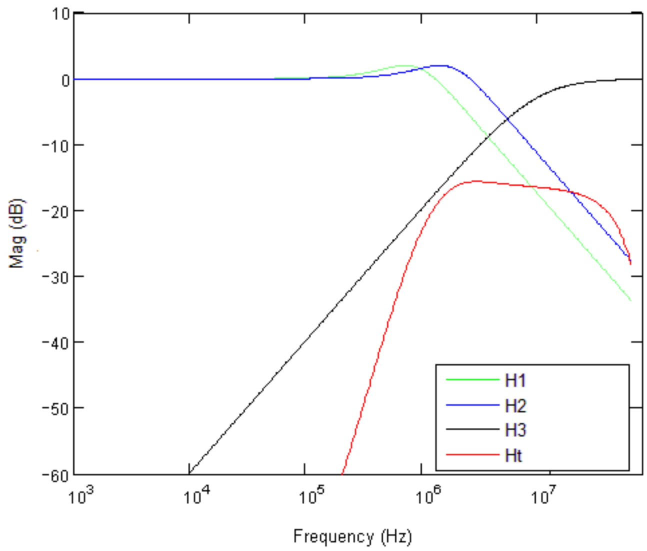


PCIe Gen2A Magnitude of Transfer Function



PCIe Gen2B Magnitude of Transfer Function

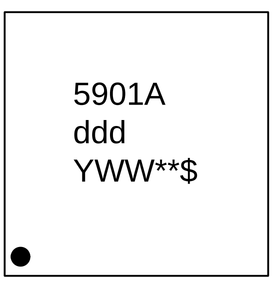
For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen3 Magnitude of Transfer Function

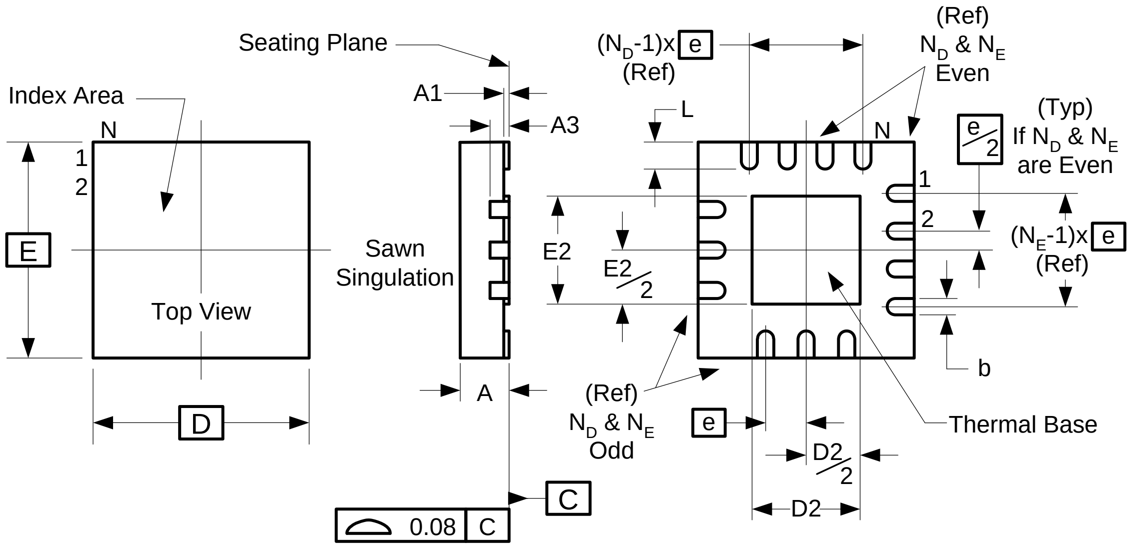
For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note PCI Express Reference Clock Requirements.

Marking Diagram



1. Line 1 is the truncated part number.
2. “ddd” denotes dash code.
3. “YWW” is the last digit of the year and week that the part was assembled.
4. “**” denotes lot number.
5. “$” denotes mark code.

Package Outline and Package Dimensions (24-pin 4mm x 4mm VFQFPN)



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	24	
N_D	6	
N_E	6	
D x E BASIC	4.00 x 4.00	
D2	2.3	2.55
E2	2.3	2.55
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P49V5901AdddNLGI	see page 32	Trays	24-pin VFQFPN	-40° to +85°C
5P49V5901AdddNLGI8		Tape and Reel	24-pin VFQFPN	-40° to +85°C

Note: for the specific "ddd" order codes, refer to the *VersaClock 5 Ordering Product Information Guide*.

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/10/14	B. Chandhoke	Initial release.

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