



3.3V CMOS ONE-TO-FOUR ADDRESS/CLOCK DRIVER

IDT74FCT163344A/C

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range, or $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components
- Available in SSOP and TSSOP packages

DESCRIPTION:

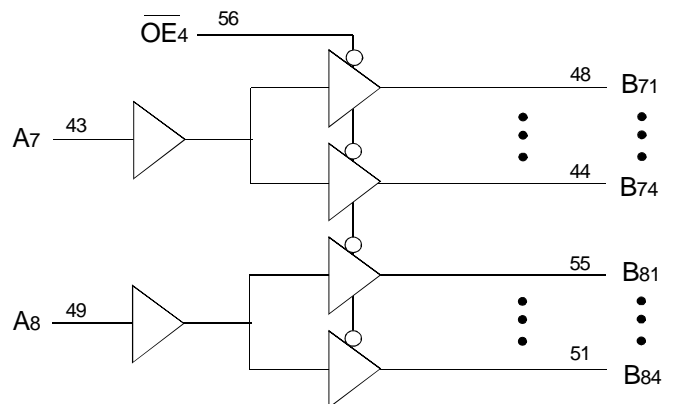
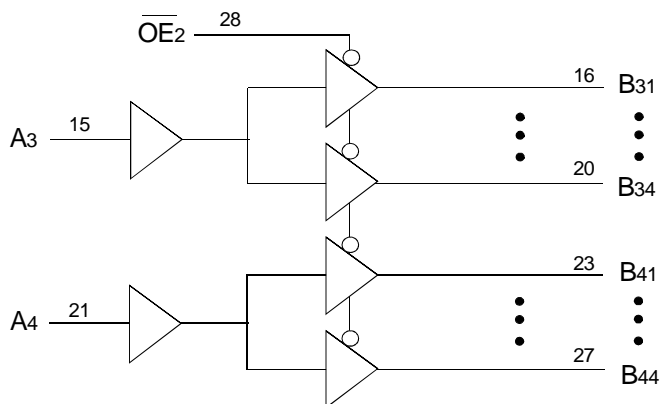
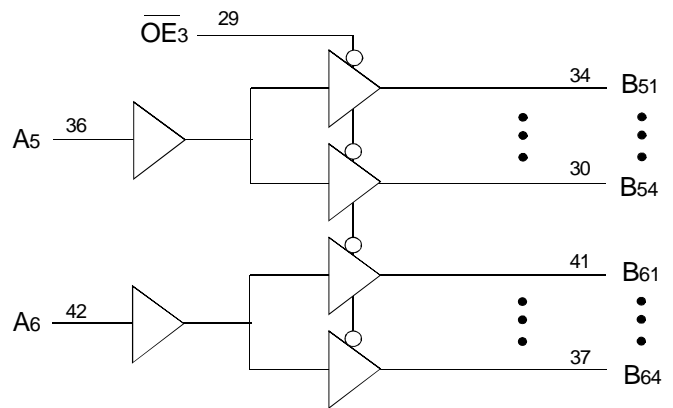
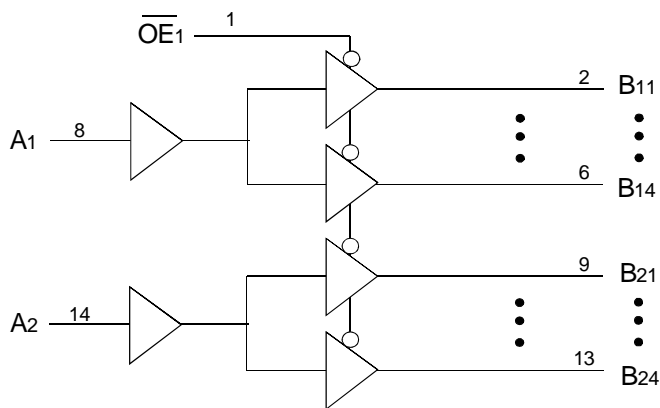
The FCT163344 is a 1:4 address/clock driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

The FCT163344 has series current limiting resistors. These offer low ground bounce, minimal undershoot and controlled output fall times, reducing the need for external series terminating resistors.

A large number of power and ground pins ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

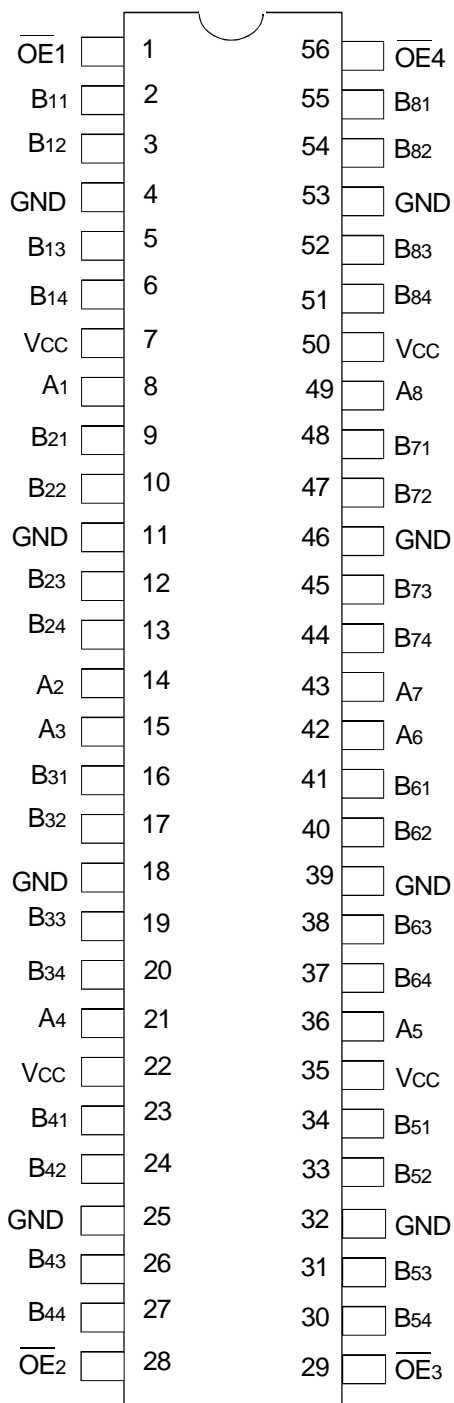
The inputs of the FCT163344 can be driven from either 3.3V or 5V device. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to 7 | V |
| V _{TERM} ⁽⁴⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -60 to +60 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 3.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 3.5 | 7 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|------------------|---|
| $\overline{OE}x$ | 3-State Output Enable Inputs (Active LOW) |
| Ax | Inputs |
| Bxx | 3-State Outputs |

FUNCTION TABLE⁽¹⁾

| Inputs | | Outputs |
|------------------|----|---------|
| $\overline{OE}x$ | Ax | Bxx |
| L | L | L |
| L | H | H |
| H | X | Z |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Unit | |
|-------------------------------------|--|--|--------------------------|---------------------|--------------|---------------|--------------------|
| V_{IH} | Input HIGH Level (Input pins) | Guaranteed Logic HIGH Level | 2 | — | 5.5 | V | |
| | Input HIGH Level (I/O pins) | | 2 | — | $V_{CC}+0.5$ | | |
| V_{IL} | Input LOW Level (Input and I/O pins) | Guaranteed Logic LOW Level | -0.5 | — | 0.8 | V | |
| I_{IH} | Input HIGH Current (Input pins) | $V_{CC} = \text{Max.}$ | $V_I = 5.5\text{V}$ | — | — | ± 1 | |
| | Input HIGH Current (I/O pins) | | | | | | $V_I = V_{CC}$ |
| I_{IL} | Input LOW Current (Input pins) | | $V_I = \text{GND}$ | — | — | ± 1 | |
| | Input LOW Current (I/O pins) | | | | | | $V_I = \text{GND}$ |
| I_{OZH} | High Impedance Output Current (3-State Output pins) | $V_{CC} = \text{Max.}$ | $V_O = V_{CC}$ | — | — | ± 1 | |
| I_{OZL} | | | $V_O = \text{GND}$ | — | — | ± 1 | |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | — | -0.7 | -1.2 | V | |
| I_{ODH} | Output HIGH Current | $V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$ | -36 | -60 | -110 | mA | |
| I_{ODL} | Output LOW Current | $V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$ | 50 | 90 | 200 | mA | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$ | $I_{OH} = -0.1\text{mA}$ | $V_{CC}-0.2$ | — | — | V |
| | | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -3\text{mA}$ | 2.4 | 3 | — | |
| | | $V_{CC} = 3\text{V}$ | $I_{OH} = -8\text{mA}$ | 2.4 ⁽⁵⁾ | 3 | — | |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$ | $I_{OL} = 0.1\text{mA}$ | — | — | 0.2 | V |
| | | | $I_{OL} = 16\text{mA}$ | — | 0.2 | 0.4 | |
| | | | $I_{OL} = 24\text{mA}$ | — | 0.3 | 0.55 | |
| | | $V_{CC} = 3\text{V}$ | $I_{OL} = 24\text{mA}$ | — | 0.3 | 0.5 | |
| I_{OS} | Short Circuit Current ⁽⁴⁾ | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | — | — | — | — | |
| | | | | | | | — |
| I_{CCL} I_{CCH} I_{CCZ} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC} | — | 0.1 | 10 | μA | |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC}-0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|---|---|---|------|---------------------|--------------------|-----------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$ | | — | 2 | 30 | μA |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 230 | 320 | $\mu A/$ MHz |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 2.3 | 3.2 | mA |
| | | | $V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$ | — | 2.3 | 3.2 | |
| | | $V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE}x = \text{GND}$ Eight Input Bits Toggling 32 Output Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 4.6 | 6.4 ⁽⁵⁾ | |
| | | | $V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$ | — | 4.6 | 6.5 ⁽⁵⁾ | |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

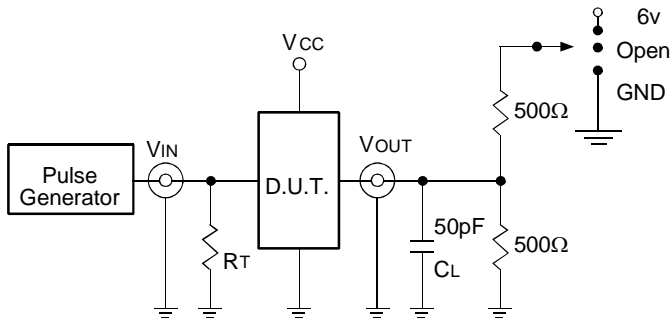
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

| Symbol | Parameter | Condition ⁽²⁾ | FCT163344A | | FCT163344C | | Unit |
|--------------|--|--------------------------|---------------------|------|---------------------|------|------|
| | | | Min. ⁽³⁾ | Max. | Min. ⁽³⁾ | Max. | |
| tPLH tPHL | Propagation Delay Ax to Bxx | CL = 50pF RL = 500Ω | 1.5 | 4.8 | 1.5 | 4.3 | ns |
| tPZH tPZL | Output Enable Time OEx to Bxx | | 1.5 | 6.2 | 1.5 | 5.8 | ns |
| tPHZ tPLZ | Output Disable Time OEx to Bxx | | 1.5 | 5.6 | 1.5 | 5.2 | ns |
| tSK(b) | Skew between outputs of the same bank and same package (same transition) ^(4,5) | | — | 0.5 | — | 0.35 | ns |
| tSK(o) | Skew between outputs of all banks of the same package (A1 - A8 tied together) ^(4,5) | | — | 0.5 | — | 0.5 | ns |

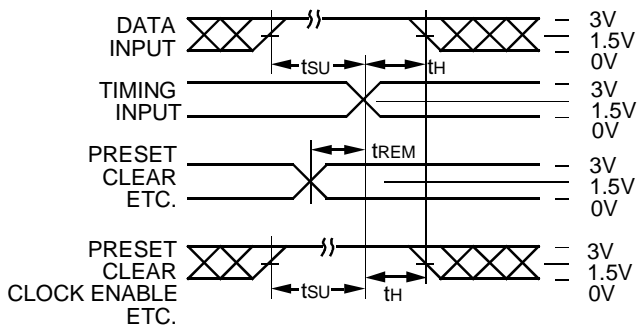
NOTES:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, Normal Range. For Vcc = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
5. This parameter is guaranteed but not tested. Skew is not guaranteed when Vcc < 0.3V.

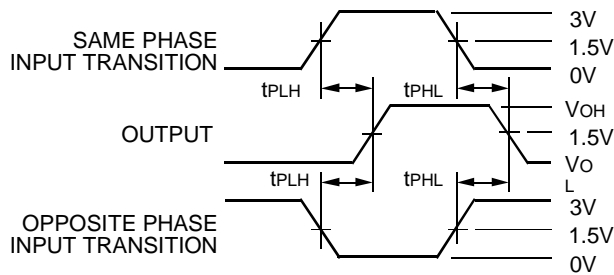
TEST CIRCUITS AND WAVEFORMS



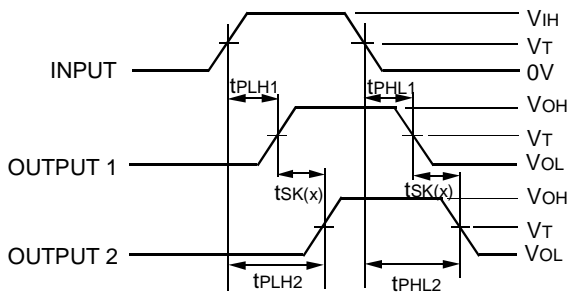
Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay



$$tsk(x) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Output Skew - $tsk(x)$

NOTES:

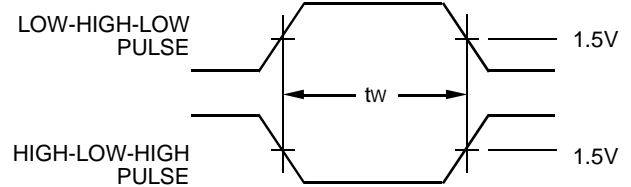
- For $tsk(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
- For $tsk(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

SWITCH POSITION

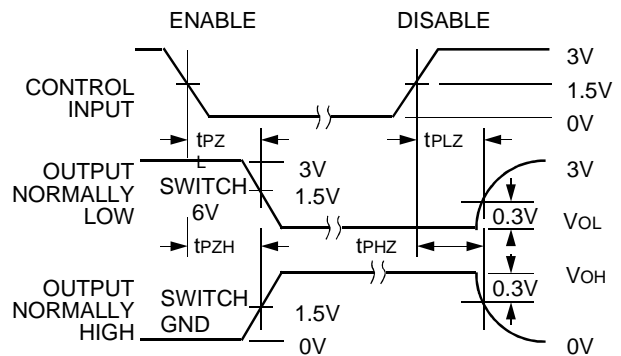
| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | 6V |
| Disable High Enable High | GND |
| All Other Tests | Open |

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

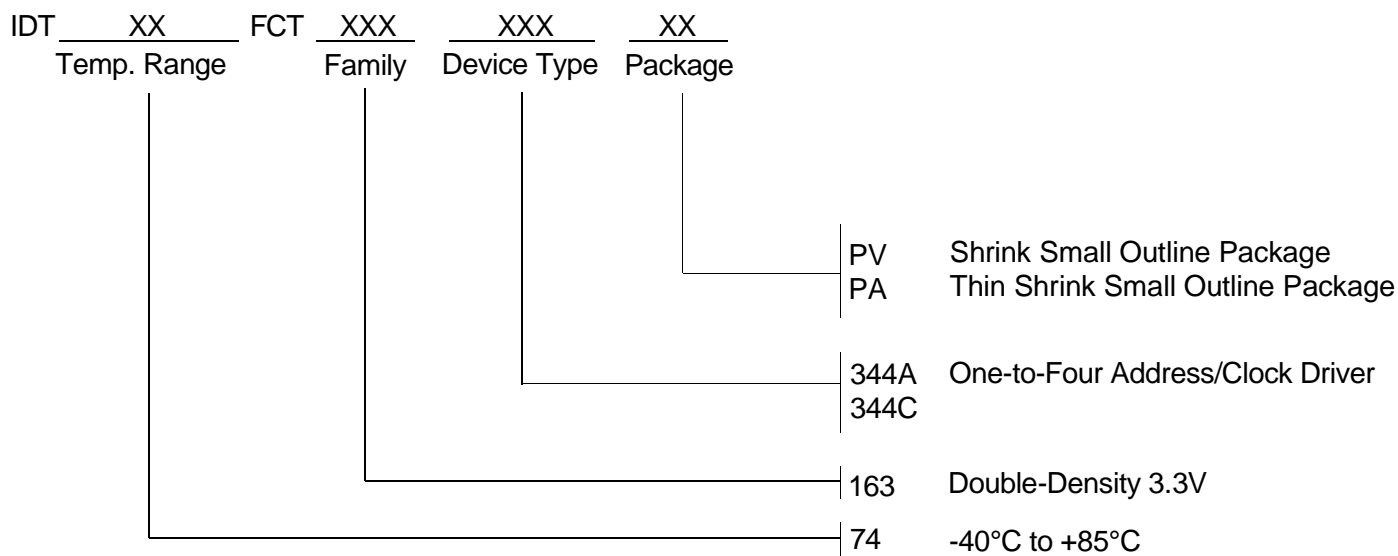


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
- if V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

4/22/2002 Removed blank speed grade



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