



Integrated Device Technology, Inc.

# 3.3V LOW SKEW PLL-BASED CMOS CLOCK DRIVER

## IDT74FCT3932-100 IDT74FCT32932-100 ADVANCE INFORMATION

### FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew
- 16 programmable frequency configurations
- 17 3-state outputs:  $\pm 24$  mA FCT3932  
 $\pm 8$  mA FCT32932
- Output configuration:  
  BANK1: 4 outputs  
  BANK2: 8 outputs  
  BANK3: 5 outputs
- Dedicated feedback output (Q\_FB)
- Maximum output frequency: 100MHz
- VCC = 3.3V  $\pm 0.3$ V
- Inputs can be driven from 3.3V or 5V components
- Available in 48 SSOP, TSSOP packages
- Suited to SDRAM applications

### DESCRIPTION:

The FCT3932 uses phase-lock loop technology to lock the frequency and phase of the feedback to the input reference clock. It provides a large number of low skew outputs that are configurable in 16 different modes using the CNTRL 1-4 inputs. A dedicated output, Q\_FB, is provided to supply the PLL feedback and it should be connected to the FEEDBACK input. Q\_FB is located adjacent to FEEDBACK to minimize the delay in the feedback path. In order to offset any delay in the output path from the FCT3932 output to a receiving device,

feedback path delay should be made to match this output path delay.

The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The FCT3932 requires no external loop filter components.

The FCT3932 provides 17 outputs grouped in 3 banks with individual 3-state control and an additional dedicated feedback output with no disable. Connecting Q\_FB to FEEDBACK ensures uninterrupted PLL operation when all outputs are disabled.

Individual bank 3-state allows users to disable unused outputs in order to limit power dissipation or minimize switching noise. It also allows users to shut down outputs in low power modes while maintaining phase lock.

The FCT3932 provides a LOCK pin that goes high when the device is phase-locked.

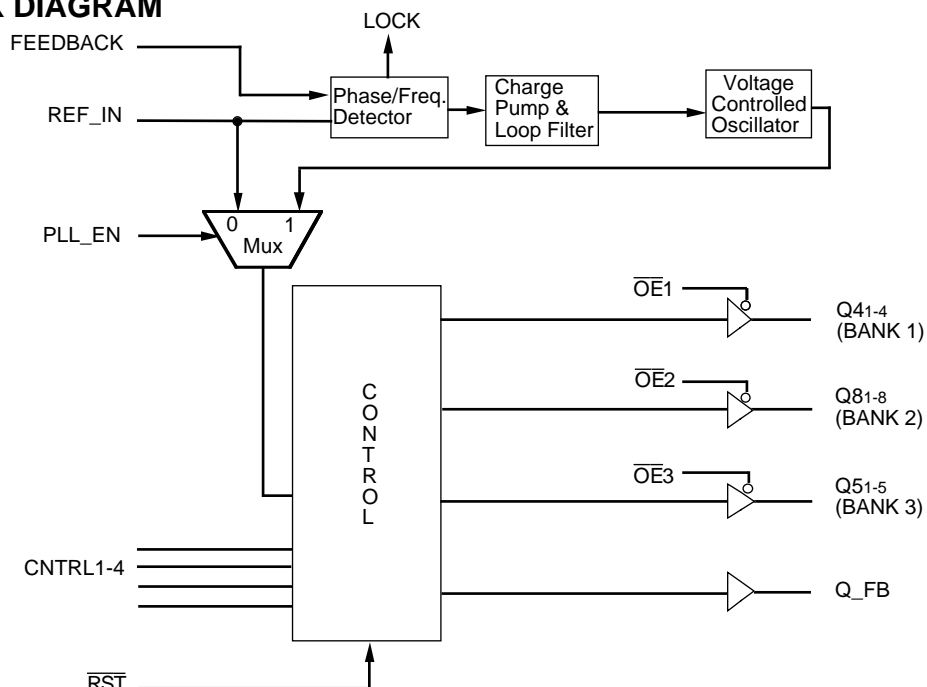
The user can bypass the PLL for testability purposes by deasserting PLL\_EN. In this "test" mode, the input frequency is not limited to the specified range.

The FCT3932 provides an asynchronous reset input,  $\overline{RST}$ , which resets all outputs. This initializes all internal registers so that outputs start up in a known state.

### APPLICATIONS:

SDRAM DIMM Clock, Caches, high speed microprocessors, motherboard clock distribution to DIMMs.

### FUNCTIONAL BLOCK DIAGRAM



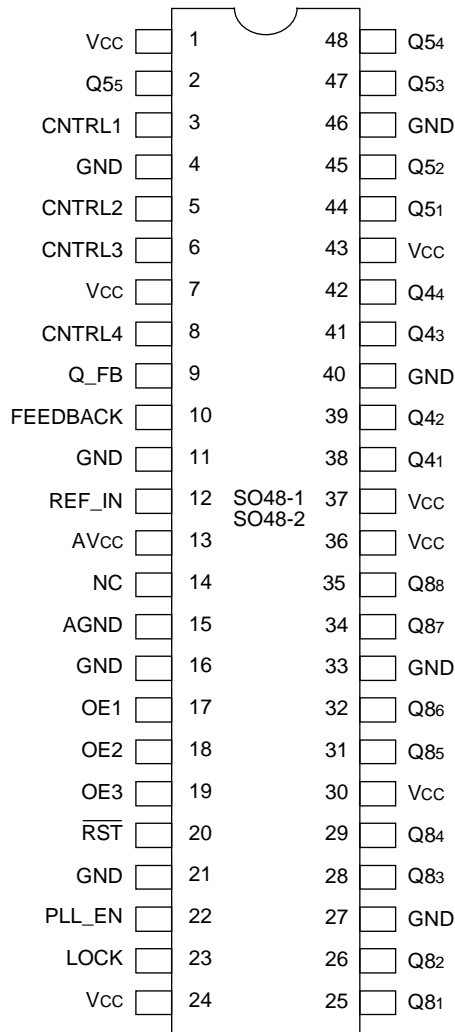
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COMMERCIAL TEMPERATURE RANGE

NOVEMBER 1996

## PIN CONFIGURATIONS



SSOP  
 TSSOP  
 TOP VIEW

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\*NC = No connect

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(4)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> + 0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +60	mA

### NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- Input terminals.
- Output and I/O terminals.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	3.2	5.0	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	3.7	8.0	pF

### NOTE:

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- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Name	I/O	Description
REF_IN	I	Reference clock input.
FEEDBACK	I	Feedback input to phase detector.
Q41-4	O	BANK1 clock outputs.
Q81-8	O	BANK2 clock outputs.
Q51-5	O	BANK3 clock outputs.
$\overline{OE}$ 1-3	I	Output enable controls for BANKS 1, 2 and 3 (Active LOW).
CNTRL1-4	I	Control lines to select output configuration (see table).
Q_FB	O	Dedicated PLL feedback output.
$\overline{RST}$	I	Asynchronous reset (Active LOW).
PLL_EN	I	Disables phase-lock for low frequency testing (Refer to functional block diagram).
LOCK	O	PLL "LOCK" indicator (HIGH when PLL is locked).

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## OUTPUT FREQUENCY CONFIGURATION AND INPUT FREQUENCY RANGE TABLE

MODE	CNTRL	Q_FEEDBACK	Q_BANK1 (4 outputs)	Q_BANK2 (8 outputs)	Q_BANK3 (5 outputs)	Fin Range
	4 3 2 1					
0	0 0 0 0	F (divide-by-1)	$\overline{F}$	F	F	50-100MHz
1	0 0 0 1	F (divide-by-1)	$\overline{F}$	F	F/2	50-100MHz
2	0 0 1 0	F (divide-by-1)	F	F	F	50-100MHz
3	0 0 1 1	F (divide-by-1)	F	F/2	F/2	50-100MHz
4	0 1 0 0	F (divide-by-1)	F	F/3	F	50-100MHz
5	0 1 0 1	F (divide-by-3)	3F	3F	F	16.7-33.3MHz
6	0 1 1 0	F (divide-by-3)	3F	F	3F	16.7-33.3MHz
7	0 1 1 1	F (divide-by-3)	3F	3F	3F	16.7-33.3MHz
8	1 0 0 0	F (divide-by-2)	2F	2F	2F	25-50MHz
9	1 0 0 1	F (divide-by-2)	2F	F	2F	25-50MHz
10	1 0 1 0	F (divide-by-2)	2F	F	F	25-50MHz
11	1 0 1 1	F (divide-by-2)	2F	F	F/2	25-50MHz
12	1 1 0 0	F (divide-by-2)	2F	F/2	F	25-50MHz
13	1 1 0 1	F (divide-by-4)	4F	2F	4F	12.5-25MHz
14	1 1 1 0	F (divide-by-4)	4F	2F	2F	12.5-25MHz
15	1 1 1 1	F (divide-by-4)	4F	2F	F	12.5-25MHz

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## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V <sub>CC</sub> +0.5	
V <sub>IL</sub>	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I <sub>IH</sub>	Input HIGH Current (Input pins)	V <sub>CC</sub> = Max.	V <sub>I</sub> = 5.5V	—	—	±1	μA
I <sub>IL</sub>	Input LOW Current (Input pins)		V <sub>I</sub> = GND	—	—	±1	
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = Max.	V <sub>O</sub> = V <sub>CC</sub>	—	—	±1	μA
I <sub>OZL</sub>			V <sub>O</sub> = GND	—	—	±1	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
I <sub>ODH</sub>	Output HIGH Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>		-36	-75		mA
I <sub>ODL</sub>	Output LOW Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>		50	75		mA
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>		—	—	6	mA

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### TYPE 1 DRIVER - FCT3932

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.2	—	—	V
		V <sub>CC</sub> = 3.0V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -8mA	2.2 <sup>(4)</sup>	2.4	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 0.1mA	—	—	0.2	V
			I <sub>OL</sub> = 16mA	—	0.2	0.4	
			I <sub>OL</sub> = 24mA	—	0.3	0.5	

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### TYPE 2 DRIVER - FCT32932

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.2	—	—	V
		V <sub>CC</sub> = 3.0V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -8mA	2.4 <sup>(4)</sup>	3.0	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 0.05mA	—	—	0.2	V
			I <sub>OL</sub> = 4mA	—	0.2	0.4	
			I <sub>OL</sub> = 8mA	—	0.3	0.5	

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#### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- V<sub>OH</sub> = V<sub>CC</sub> - 0.6V at rated current.

## INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit	
tRISE/FALL	Rise/Fall Times REF_IN input (0.8V to 2.0V)	—	3.0	ns	
Frequency	Input Frequency REF_IN input	Modes 0, 1, 2, 3, 4	50	100	MHz
		Modes 5, 6, 7	16.7	33.3	
		Modes 8, 9, 10, 11, 12	25	50	
		Modes 13, 14, 15	12.5	25	
Duty Cycle	Input Duty Cycle, REF_IN input	25	75	%	

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## OUTPUT FREQUENCY SPECIFICATIONS

Mode	Parameter	Min.	Max.	Unit	
0, 1, 2, 3, 4	Operating frequency	F, $\bar{F}$ Outputs	50	100	MHz
		F/2 Outputs	25	50	
		F/3 Outputs	16.7	33.3	
5, 6, 7	Operating frequency	3F Outputs	50	100	MHz
		F Outputs	16.7	33.3	
8, 9, 10, 11, 12	Operating frequency	2F Outputs	50	100	MHz
		F Outputs	25	50	
		F/2 Outputs	12.5	25	
13, 14, 15	Operating frequency	4F Outputs	50	100	MHz
		2F Outputs	25	50	
		F Outputs	12.5	25	

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## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub> - 0.6V <sup>(3)</sup>	—	2.0	30	$\mu$ A
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. All Outputs Open 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> F = 50MHz V <sub>IN</sub> = GND MODE 10	—	72		$\mu$ A/ MHz/ bit
I <sub>C</sub>	Total Power Supply Current <sup>(5,6)</sup>	V <sub>CC</sub> = Max. PLL_EN = 1, LOCK = 1, MODE 10 REF_IN frequency = 50MHz. All outputs open		—	62		mA

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD}(f) + I_{LOAD}$   
 I<sub>CC</sub> = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CC3</sub>)  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f = SYNC input frequency  
 I<sub>LOAD</sub> = Dynamic Current due to load.

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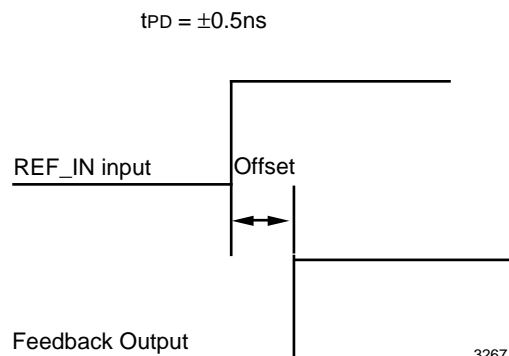
### SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(7)</sup>

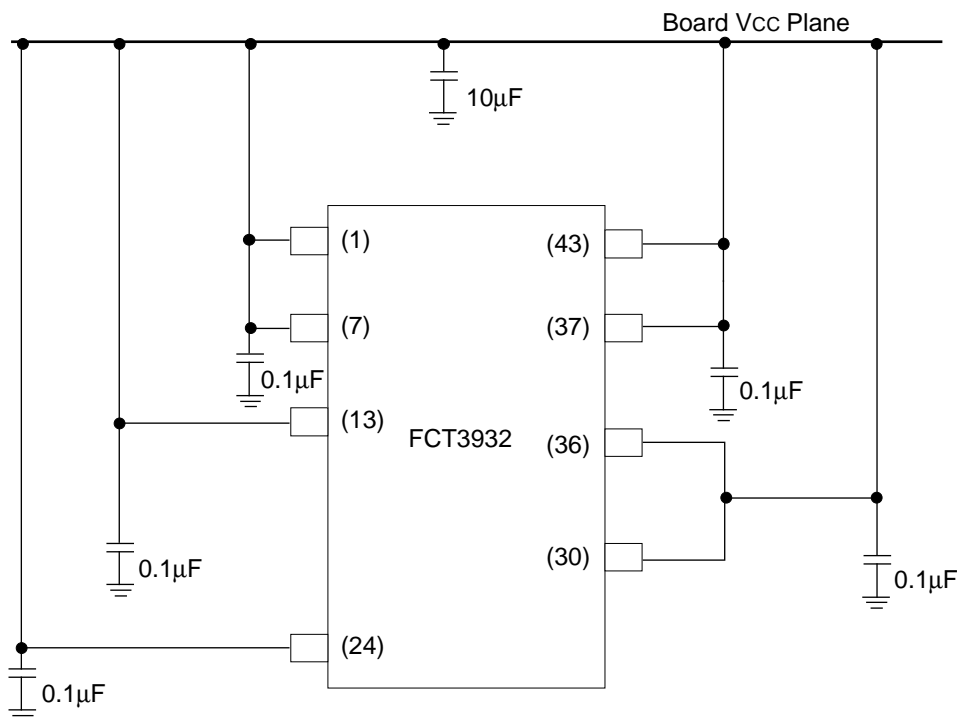
Symbol	Parameter	Condition <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Unit	
t <sub>PD</sub> <sup>(3)</sup> REF_IN-Q_FB	Propagation Delay (REF_IN input to Q outputs)	No Load	-0.5	+0.5	ns	
t <sub>RISE/FALL</sub> All Outputs	Rise/Fall Time (between 0.8 and 2.0V)	FCT3932 FCT32932	CL = 20pF for FCT3932 CL = 10pF for FCT32932	0.5 0.5	1.5 2.0	ns
t <sub>PW</sub> <sup>(3)</sup>	Output Duty Cycle		45	55	%	
t <sub>SKEWr</sub> <sup>(3,4)</sup>	Output to Output Skew (All outputs at same frequency rising edge)		—	500	ps	
t <sub>SKEWf</sub> <sup>(3,4)</sup>	Output to Output Skew (All outputs at same frequency falling edge)		—	500	ps	
t <sub>SKEWall</sub> <sup>(3,4)</sup>	Output to Output Skew (All outputs, rising edge any frequency)		—	1.0	ns	
t <sub>LOCK</sub> <sup>(5)</sup>	Time required to acquire Phase-Lock from time REF_IN input signal is received		1	10	ms	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEx}$ (LOW-to-HIGH) to Q		3.0	8.0	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEx}$ (HIGH-to-LOW) to Q		3.0	8.0	ns	

**GENERAL AC SPECIFICATION NOTES:**

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1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. With V<sub>cc</sub> fully powered-on and Q\_FB properly connected to the FEEDBACK pin.
6. The t<sub>PD</sub> spec gives the limits of the phase offset between the REF\_IN input and the Q\_FB output.
7. The AC specifications are only guaranteed with the decoupling scheme shown in figure 2.





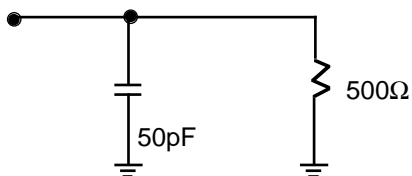
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Figure 2. Recommended Decoupling for the FCT3932/FCT32932

**NOTES:**

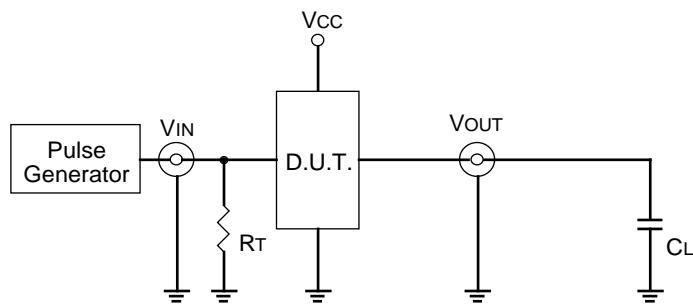
1. Figure 2 shows a decoupling scheme which will be effective in most FCT3932 applications. The following guidelines should be followed for stable, jitter-free operation:
  - a. All decoupling capacitors should be connected as close to the package as possible. (Preferably at the device pins).
  - b. The 10µF and 0.1µF bypass capacitors provide protection from power supply and ground plane transients.

**STANDARD LOAD (USED WHEN SPECIFIED)**

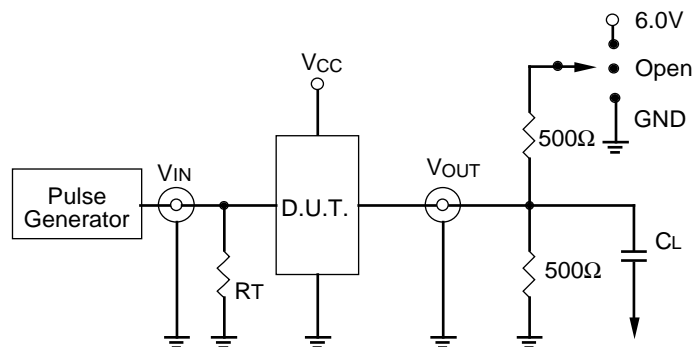


## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUIT



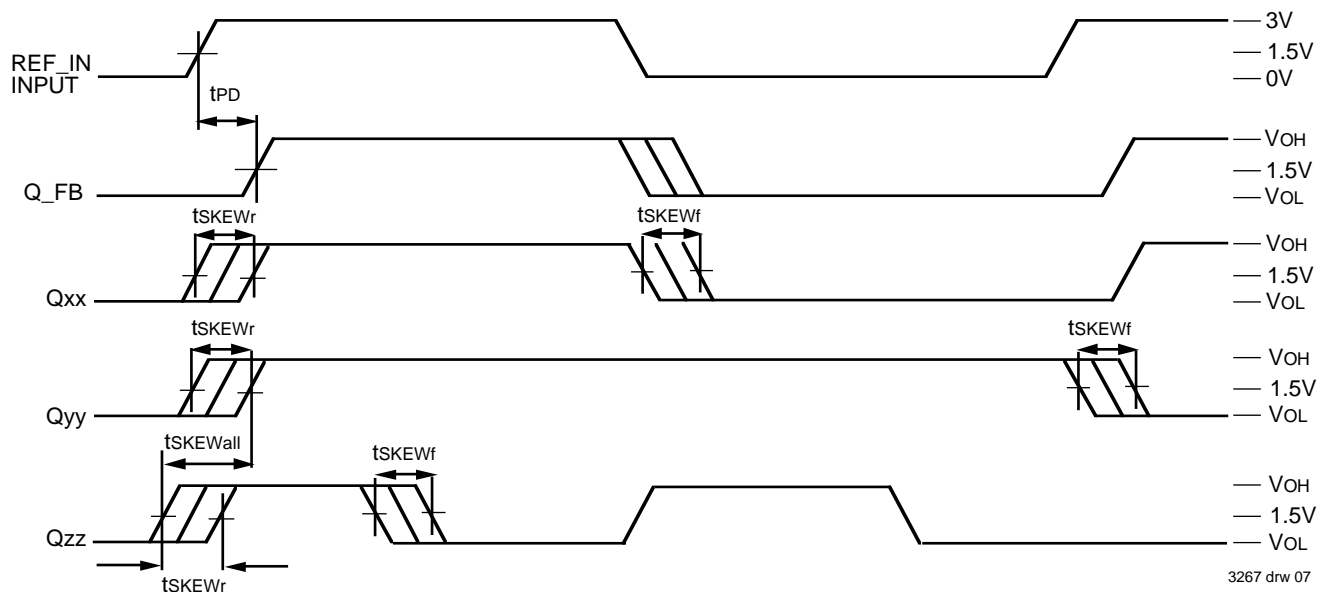
### ENABLE/DISABLE TEST CIRCUIT



### PROPAGATION DELAY, OUTPUT SKEW

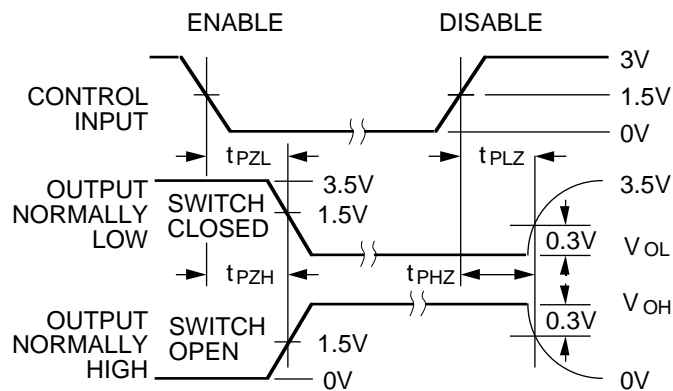
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### ENABLE AND DISABLE TIMES



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#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses:  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

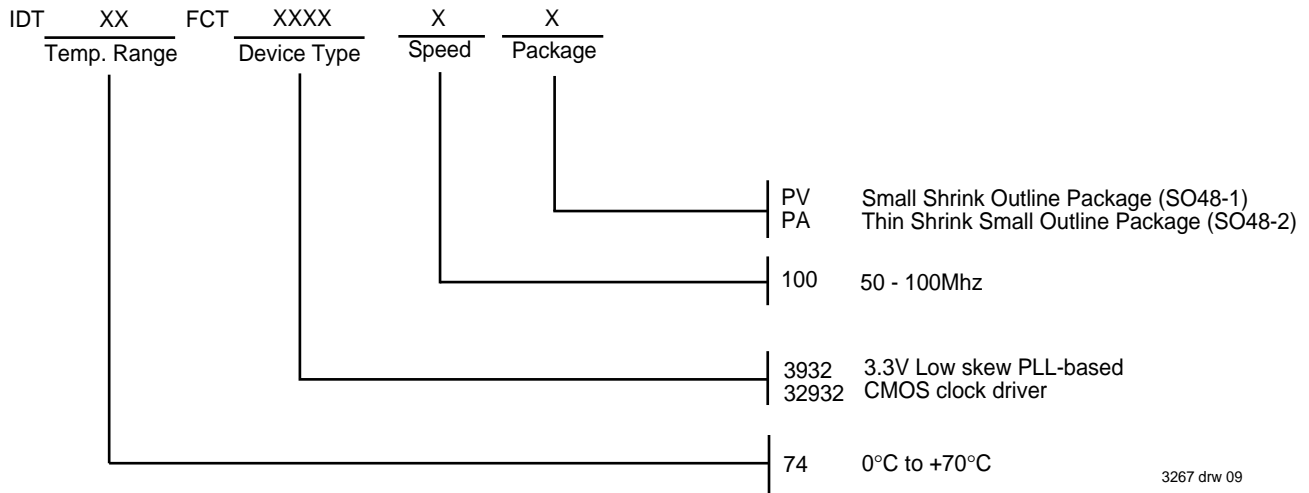
#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

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## ORDERING INFORMATION



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