FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
  FST163xxx – 4Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP
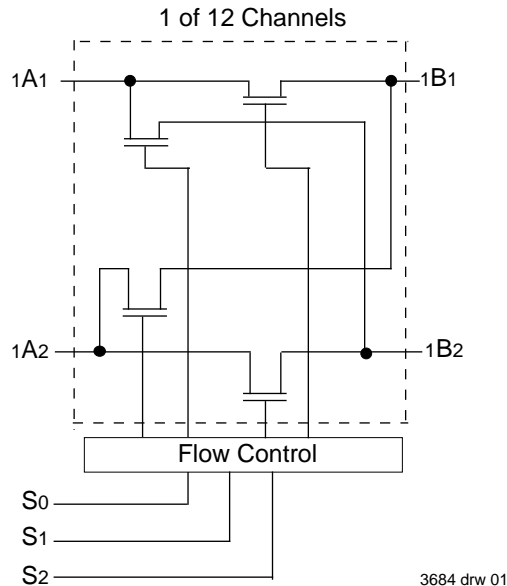
DESCRIPTION:

The FST163213 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When ther gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163213 provides four 12-bit TTL-compatible ports that support 2 way bus exchange. The S_{0-2} pins control the bus exchange and switch enable functions.

FUNCTIONAL BLOCK DIAGRAM

1 of 12 Channels

3684 drw 01

PIN DESCRIPTION

Pin Names	I/O	Description
A_1, A_2 B_1, B_2	I/O	Buses A_1, A_2, B_1, B_2
S_{0-2}	I	Control Pins for Mux and Switch Enable Functions

3684 tbl 01

COMMERCIAL TEMPERATURE RANGE   **FEBRUARY 1997**

DSC-3684/-

PIN CONFIGURATION

S_0	1		56	S_1
$1A_1$	2		55	S_2
$1A_2$	3		54	$1B_1$
$2A_1$	4		53	$1B_2$
$2A_2$	5		52	$2B_1$
$3A_1$	6		51	$2B_2$
$3A_2$	7		50	$3B_1$
GND	8		49	GND
$4A_1$	9		48	$3B_2$
$4A_2$	10		47	$4B_1$
$5A_1$	11		46	$4B_2$
$5A_2$	12		45	$5B_1$
$6A_1$	13		44	$5B_2$
$6A_2$	14	SO56-1 SO56-2 SO56-3	43	$6B_1$
$7A_1$	15		42	$6B_2$
$7A_2$	16		41	$7B_1$
V_{CC}	17		40	$7B_2$
$8A_1$	18		39	$8B_1$
GND	19		38	GND
$8A_2$	20		37	$8B_2$
$9A_1$	21		36	$9B_1$
$9A_2$	22		35	$9B_2$
$10A_1$	23		34	$10B_1$
$10A_2$	24		33	$10B_2$
$11A_1$	25		32	$11B_1$
$11A_2$	26		31	$11B_2$
$12A_1$	27		30	$12B_1$
$12A_2$	28		29	$12B_2$

3684 drw 02

**SSOP/
TSSOP/TVSOP
TOP VIEW**

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

3684 lnk 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condiitions for extended periods may affect reliability.
2. V_{CC}, Control and Switch terminals.

CAPACITANCE[1]

Symbol	Parameter	Conditions[2]	Typ.	Unit
C_{IN}	Control Input Capacitance		4	pF
$C_{I/O}$	Switch Input/Output Capacitance	Switch Off		pF

3684 lnk 03

NOTES:
1. Capacitance is characterized but not tested
2. $T_A = 25°C$, $f = 1MHz$, $V_{IN} = 0V$, $V_{OUT} = 0V$

FUNCTION TABLE

S_2	S_1	S_0	A_1	A_2	Function
L	L	L	Z	Z	Disconnect
L	L	H	B_1	Z	A_1 to B_1
L	H	L	B_2	Z	A_1 to B_2
L	H	H	Z	B_1	A_2 to B_1
H	L	L	Z	B_2	A_2 to B_2
H	L	H	A_2 & B_2	Z	A_1 to A_2 and B_2
H	H	L	B_1	B_2	A_1 to B_1, A_2 to B_2
H	H	H	B_2	B_1	A_1 to B_2, A_2 to B_1

3684 tbl 04

2

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance[4]	V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 64mA		—	4	7	Ω
		V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 30mA		—	4	7	Ω
		V_{CC} = Min. V_{IN} = 2.4V I_{ON} = 15mA		—	10	15	Ω
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	µA

3684 tbl 05

NOTES:
1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be testes at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pins Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	—	7.2	9.6	mA
		(24 Switches Toggling) f_i = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	7.7	11.1	

3684 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} \, D_H N_T + I_{CCD} \, (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

| Symbol	Description	Condition[1]	Min.[2]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	ns
t_{BX}	Switch Multiplex Delay S to A, B		1.5	—	6.5	ns
t_{PZH} t_{PZL}	Switch Turn on Delay S to A, B		1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay S to A, B[3]		1.5	—	7	ns
$|Q_{CI}|$	Charge Injection, Typical[5,7]		—	1.5	—	pC
$|Q_{DCI}|$	Charge Injection, Typical[6,7]		—	0.5	—	

3684 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Measured at switch turn off through bus multiplexer, (e.g.- A1 to B1 = >A1 to B2), load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A1 to B1 switch is compensated by the turn on of the A1 to B2 switch.
7. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS
TEST CIRCUITS FOR ALL OUTPUTS

V_{CC}

7.0V

500Ω

Pulse Generator — V_{IN} — D.U.T. — V_{OUT}

R_T

50pF

C_L

500Ω
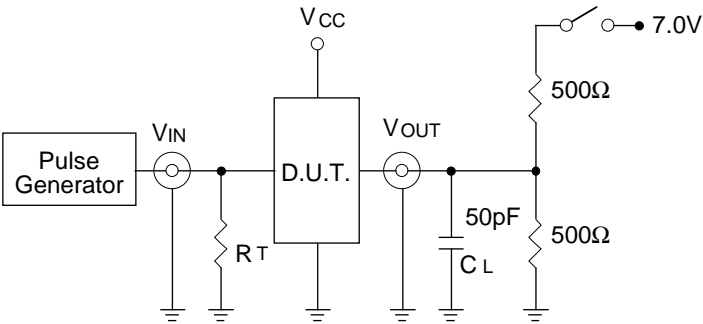
3684 drw 03

SWITCH POSITION
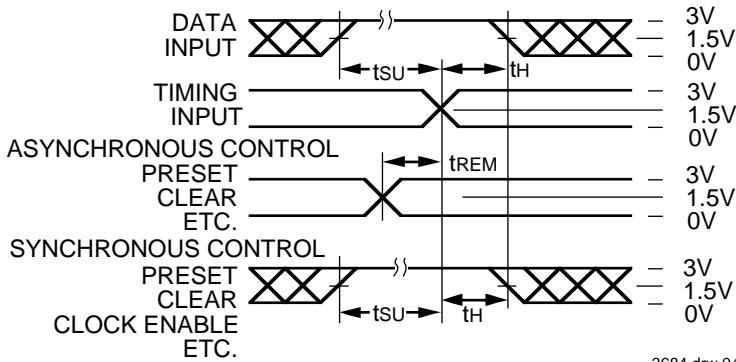
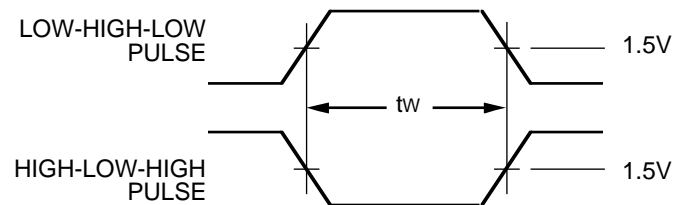| Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3684 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
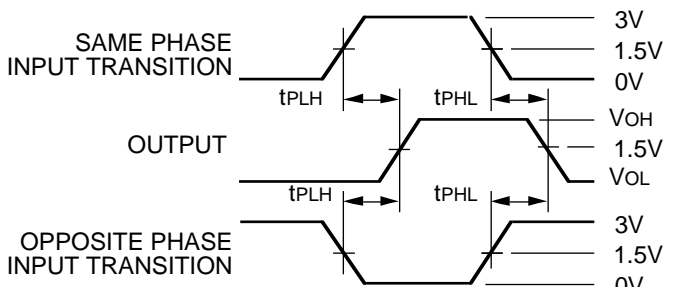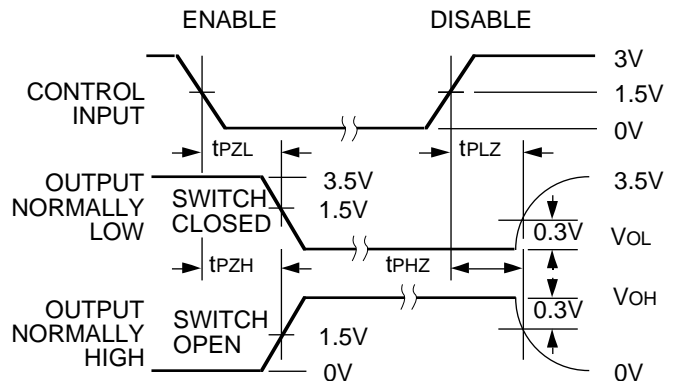
SET-UP, HOLD AND RELEASE TIMES

DATA INPUT — 3V / 1.5V / 0V

t_{SU} — t_H

TIMING INPUT — 3V / 1.5V / 0V

ASYNCHRONOUS CONTROL PRESET CLEAR ETC. — t_{REM} — 3V / 1.5V / 0V

SYNCHRONOUS CONTROL PRESET CLEAR CLOCK ENABLE ETC. — t_{SU} — t_H — 3V / 1.5V / 0V

3684 drw 04

PULSE WIDTH

LOW-HIGH-LOW PULSE — 1.5V

t_W

HIGH-LOW-HIGH PULSE — 1.5V

3684 drw 05

PROPAGATION DELAY

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V

t_{PLH} — t_{PHL}

OUTPUT — V_{OH} / 1.5V / V_{OL}

t_{PLH} — t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

3684 drw 06

ENABLE AND DISABLE TIMES

ENABLE   DISABLE

CONTROL INPUT — 3V / 1.5V / 0V

t_{PZL} — t_{PLZ}

OUTPUT NORMALLY LOW — SWITCH CLOSED — 3.5V / 1.5V

t_{PZH} — t_{PHZ} — 3.5V / 0.3V / V_{OL}

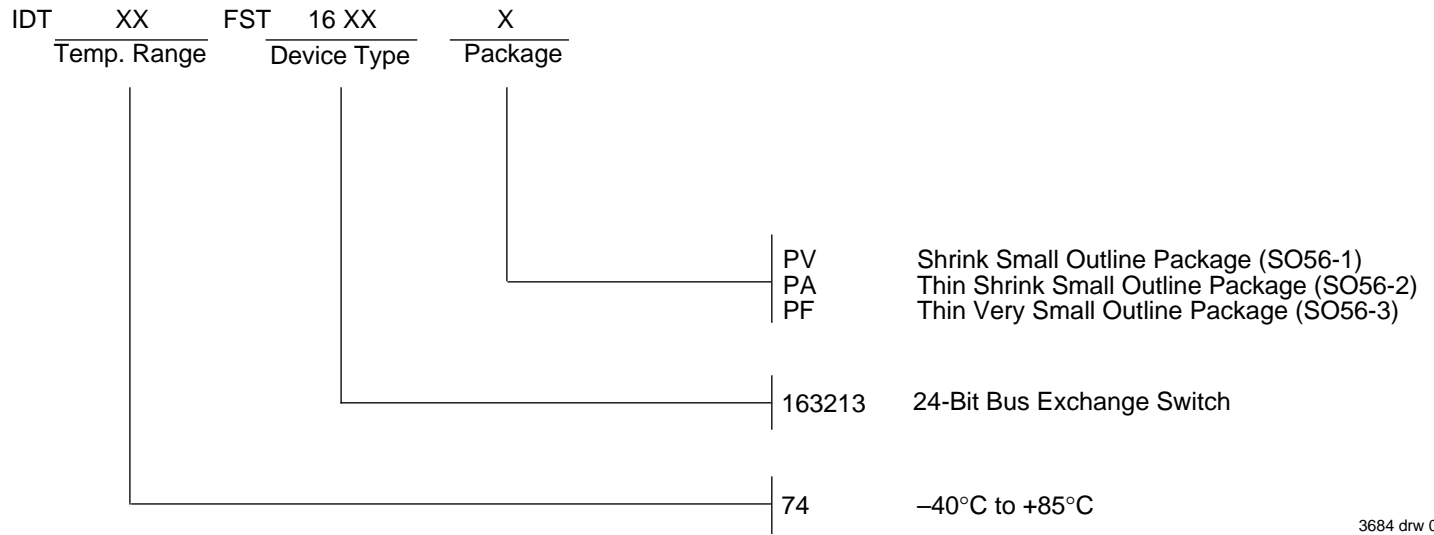OUTPUT NORMALLY HIGH — SWITCH OPEN — 1.5V / 0V — 0.3V / V_{OH} / 0V

3684 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION

```
IDT     XX     FST   16 XX        X
      Temp. Range      Device Type    Package
```

PV	Shrink Small Outline Package (SO56-1)
PA	Thin Shrink Small Outline Package (SO56-2)
PF	Thin Very Small Outline Package (SO56-3)

163213	24-Bit Bus Exchange Switch

74	–40°C to +85°C

3684 drw 08