



Integrated Device Technology, Inc.

# 512K x 8 CMOS STATIC RAM MODULE

**IDT7MB4048**

## FEATURES:

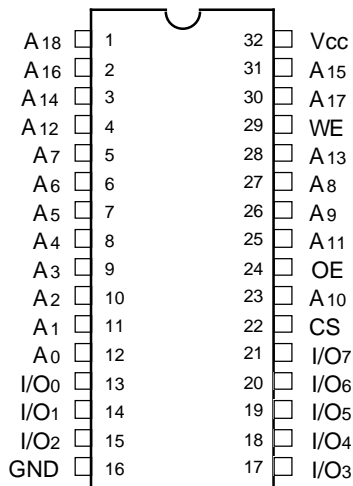
- High-density 4-megabit (512K x 8) Static RAM module
- Fast access time: 25ns (max.)  
Surface mounted plastic packages on a 32-pin, 600 mil FR-4 DIP substrate
- Single 5V ( $\pm 10\%$ ) power supply
- Inputs/outputs directly TTL-compatible

## DESCRIPTION:

The IDT7MB4048 is a 4-megabit (512K x 8) Static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using four 1 megabit SRAMs and a decoder. The IDT7MB4048 is available with access times as fast as 25ns. The IDT7MB4048 is packaged in a 32-pin FR-4 DIP resulting in the JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7MB4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

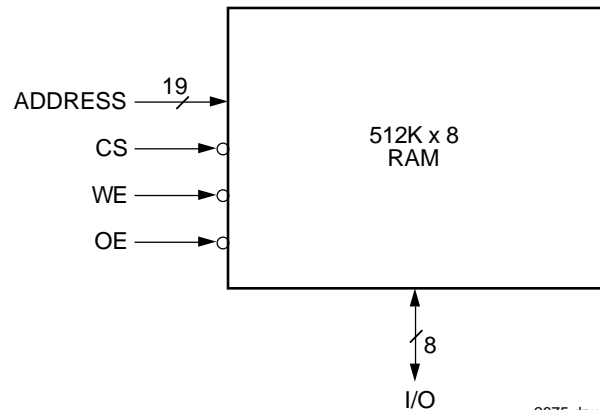
## PIN CONFIGURATION



2675 drw 01

**DIP  
TOP VIEW**

## FUNCTIONAL BLOCK DIAGRAM



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## PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

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The IDT logo is a registered trademark of Integrated Device Technology Inc.

**COMMERCIAL TEMPERATURE RANGE**

**DECEMBER 1995**

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DSC-2675/6

### TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

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### CAPACITANCE<sup>(1)</sup> (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance ( $\overline{CS}$ )	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

**NOTE:**

- This parameter is guaranteed by design, but not tested.

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### RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

- VIL = -2.0V for pulse width less than 10ns.

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### DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4048SxxP		Unit
			Min.	Max.	
IL	Input Leakage	VCC = Max., VIN = GND to VCC	—	8	μA
ILO	Output Leakage	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	8	μA
VOL	Output Low Voltage	VCC = Min., IOL = 8mA	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL; f = fMAX, Outputs Open	—	480	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Outputs Open	—	250	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2	—	170	mA

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### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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### RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

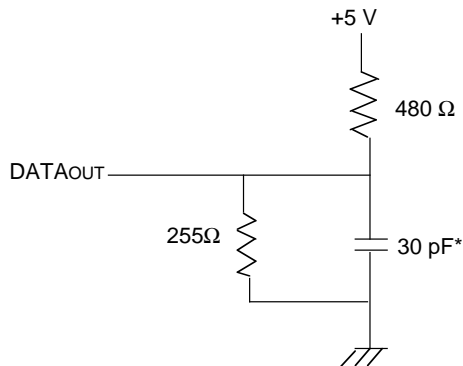
Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

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## AC TEST CONDITIONS

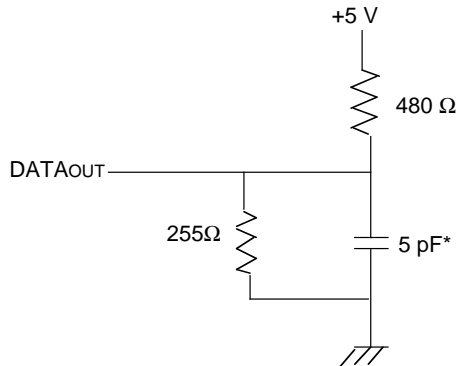
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

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Figure 1. Output Load



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Figure 2. Output Load  
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

## AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C)

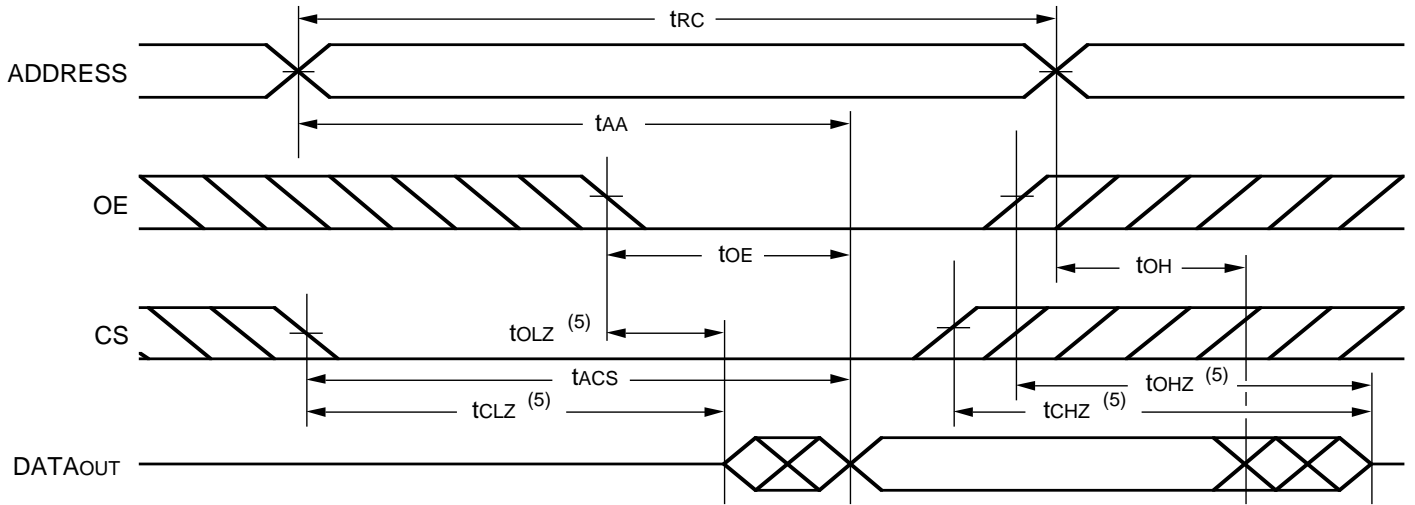
Symbol	Parameter	7MB4048						Unit
		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
tRC	Read Cycle Time	25	—	30	—	35	—	ns
tAA	Address Access Time	—	25	—	30	—	35	ns
tACS	Chip Select Access Time	—	25	—	30	—	35	ns
tOE	Output Enable to Output Valid	—	12	—	15	—	15	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in High-Z	—	12	—	12	—	15	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tCLZ <sup>(1)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
tCHZ <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	14	—	16	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	25	—	30	—	35	ns
<b>Write Cycle</b>								
tWC	Write Cycle Time	25	—	30	—	35	—	ns
tWP	Write Pulse Width	17	—	20	—	25	—	ns
tAS <sup>(2)</sup>	Address Set-up Time	3	—	0	—	0	—	ns
tAW	Address Valid to End-of-Write	20	—	25	—	30	—	ns
tCW	Chip Select to End-of-Write	20	—	25	—	30	—	ns
tDW	Data to Write Time Overlap	15	—	17	—	20	—	ns
tDH <sup>(2)</sup>	Data Hold Time	0	—	0	—	0	—	ns
tWR <sup>(2)</sup>	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ <sup>(1)</sup>	Write Enable to Output in High-Z	—	15	—	15	—	15	ns
tOW <sup>(1)</sup>	Output Active from End-of-Write	2	—	5	—	5	—	ns

### NOTES

1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for  $\overline{\text{CS}}$  controlled write cycles. tDH, tWR= 3ns for  $\overline{\text{CS}}$  controlled write cycles.

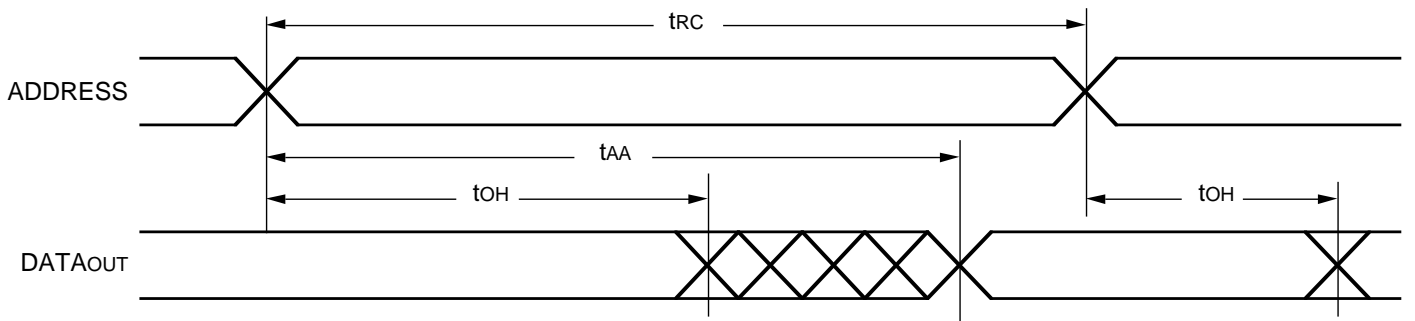
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**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



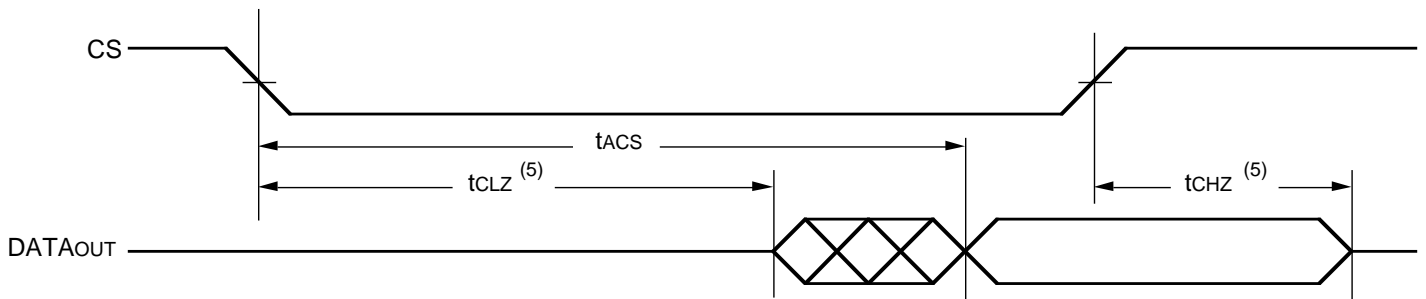
2675 drw 06

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



2675 drw 07

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**

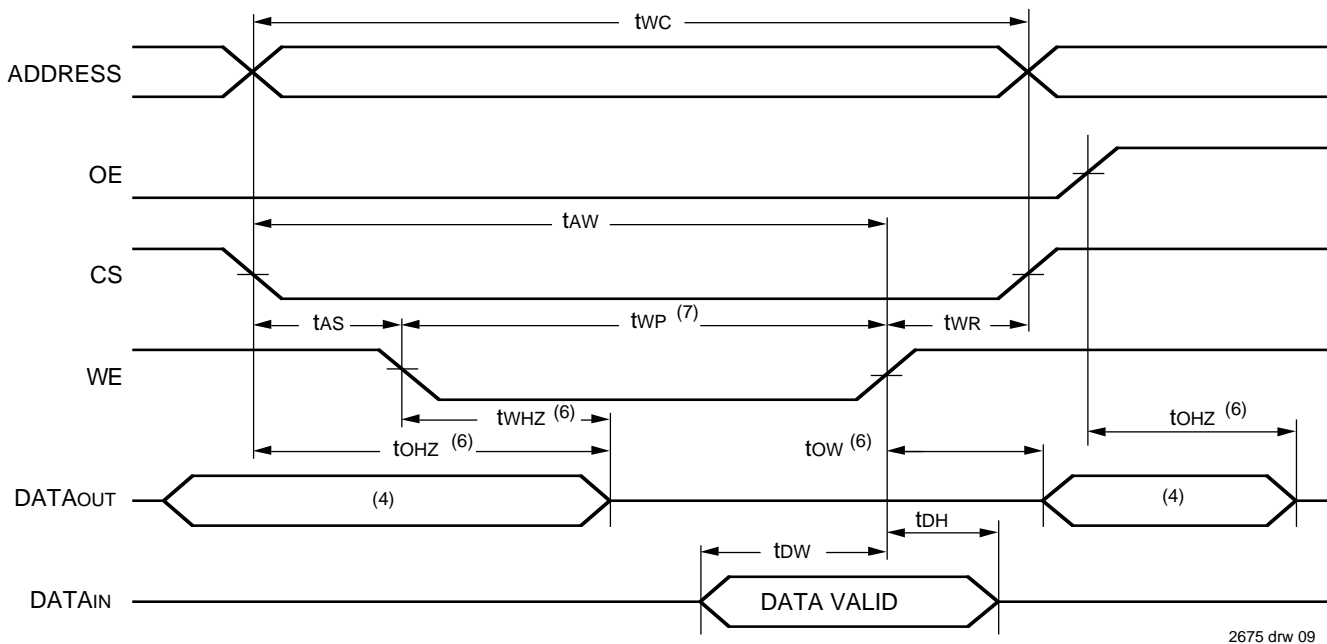


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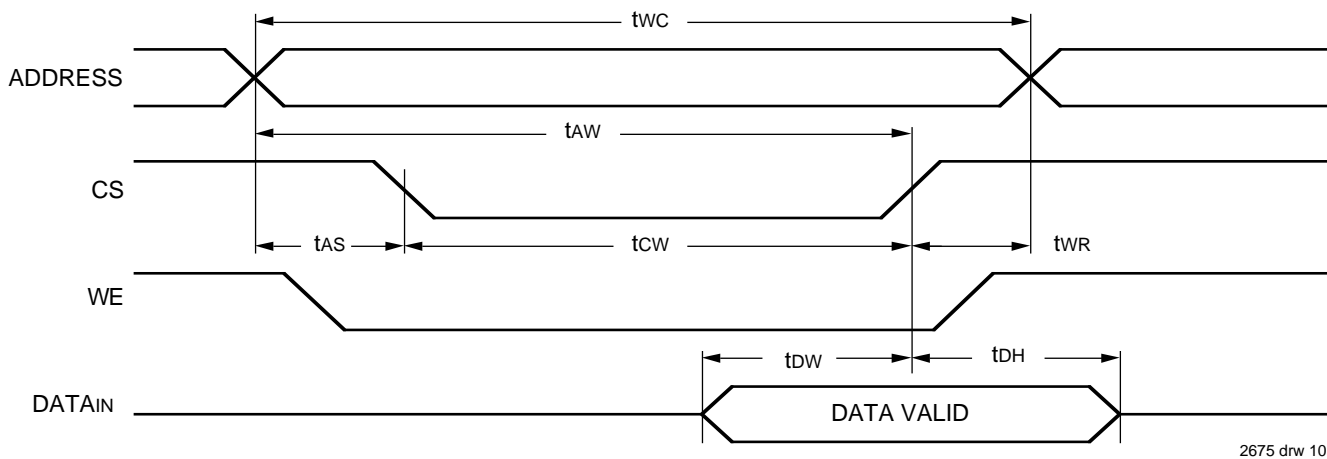
**NOTES:**

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 200mV$  from steady state. This parameter is guaranteed by design, but not tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)**(1, 2, 3, 7)



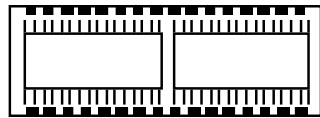
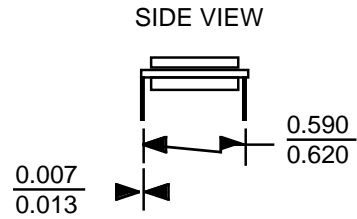
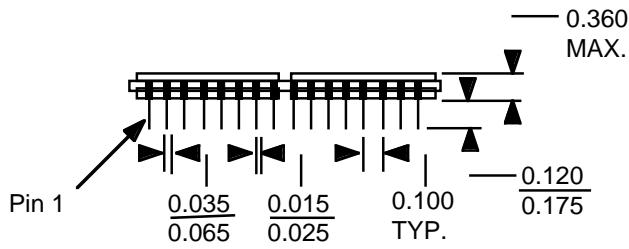
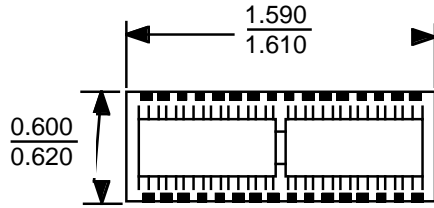
**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)**(1, 2, 3, 5)



**NOTES:**

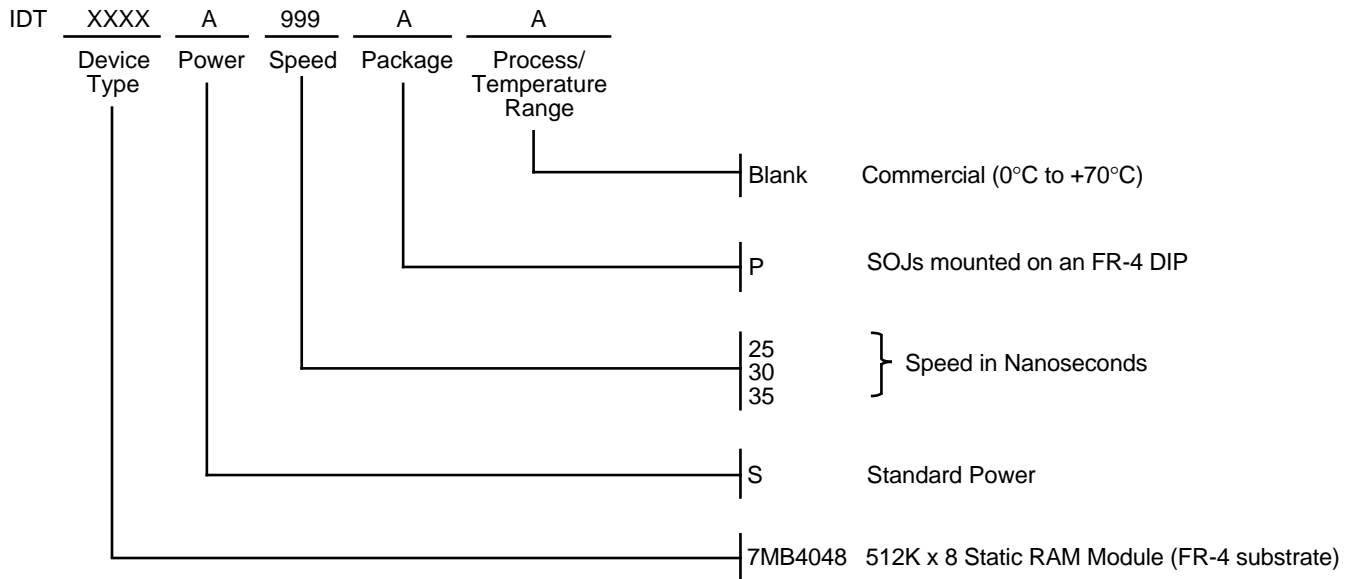
1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{DW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

**PACKAGE DIMENSIONS**



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**ORDERING INFORMATION<sup>(1)</sup>**



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