SM561

Spread Spectrum Clock Generator

Features

- **54- to 166-MHz operating frequency range**
- **Wide (9) range of spread selections**
- **Accepts clock and crystal inputs**
- **Low power dissipation**
- **3.3V = 165 mw. (Fin = 120 MHz)**
- **Frequency spread disable function**
- **Center spread modulation**
- **Low cycle-to-cycle jitter**
- **Eight-pin SOIC package**

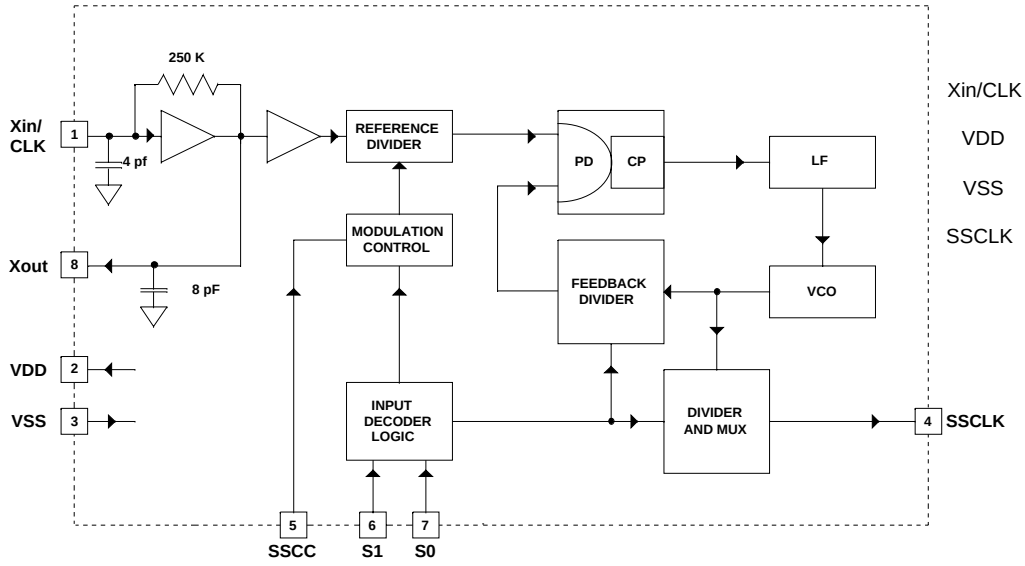
Applications

- High-resolution VGA controllers
- LCD panels and monitors
- Workstations and servers

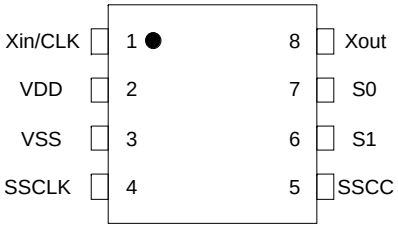
Benefits

- Peak electromagnetic interference (EMI) reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

Block Diagram



Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	Xin/CLK	I	**Clock or Crystal connection input**. Refer to *Table 1* for input frequency range selection.
2	VDD	P	**Positive power supply**.
3	GND	P	**Power supply ground**.
4	SSCLK	O	**Modulated clock output**.
5	SSCC	I	**Spread Spectrum Clock Control (Enable/Disable) function**. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	**Tri-level Logic input control pin used to select Frequency and Bandwidth**. Frequency/Bandwidth selection and Tri-level Logic programming. See *Figure 1* on page 3.
7	S0	I	**Tri-level Logic input control pin used to select Frequency and Bandwidth**. Frequency/Bandwidth selection and Tri-level Logic programming. See *Figure 1* on page 3.
8	Xout	O	**Oscillator output pin connected to crystal**. Leave this pin unconnected If an external clock drives Xin/CLK.

General Description

The Cypress SM561 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing EMI found in today's high-speed digital electronic systems.

The SM561 uses a Cypress proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of Clock (SSCLK) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading the system performance.

The SM561 is a very simple and versatile device to use. The frequency and spread% range is selected by programming S0 and S1 digital inputs. These inputs use three (3) logic states including High (H), Low (L), and Middle (M) to select one of the nine available Frequency Modulation and Spread% ranges. Refer to *Table* for programming details.

The SM561 is intended for use with applications with a reference frequency in the range of 54 to 166 MHz.

A wide range of digitally selectable spread percentages is made possible by using Tri-level (High, Low, and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread Spectrum Clock Control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The SM561 is available in an eight-pin SOIC package with a 0°C-to-70°C operating temperature range.

Refer to the SM560 data sheet for operation at frequencies from 25 to 108 MHz.

Table 1. Frequency and Spread% Selection (Center Spread)

54-108 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M (%)	S1=M S0=0 (%)	S1=1 S0=0 (%)	S1=0 S0=0 (%)	S1=0 S0=M (%)
54 - 60	3.6	3.1	2.6	2.1	1.8
60 - 70	3.5	3.0	2.5	2.0	1.7
70 - 80	3.3	2.8	2.4	1.9	1.6
80 - 100	3.0	2.5	2.1	1.7	1.4
100 - 108	2.6	2.3	1.9	1.5	1.3

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

108 - 166 MHz (High Range)

Input Frequency (MHz)	S1=1 S0=M (%)	S1=0 S0=1 (%)	S1=1 S0=1 (%)	S1=M S0=1 (%)
180 - 120	2.3	1.7	1.1	0.9
120 -130	2.3	1.7	1.1	0.9
130 - 140	2.3	1.7	1.1	0.9
140 - 150	2.2	1.6	1.1	0.9
150 - 166	2.1	1.5	1.0	0.8

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

Tri-level Logic

With binary logic, four states can be programmed with two control lines where as Tri-level Logic can program nine logic states using two control lines. Tri-level Logic in the SM561 is implemented by defining a third logic state in addition to the standard logic “1” and “0”. Pins 6 and 7 of the SM561 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (Low), “M” (Middle), and “1” (One). Each of these states have a defined voltage range that is interpreted by the SM561 as a “0”, “M,” or “1” logic state. Refer to *Table 1* for voltage ranges for each logic state. By using two equal value resistors (typically 20K) the “M” state can be easily programmed. Pins 6 or 7 can be tied directly to ground or V_{DD} for Logic “0” or “1,” respectively.

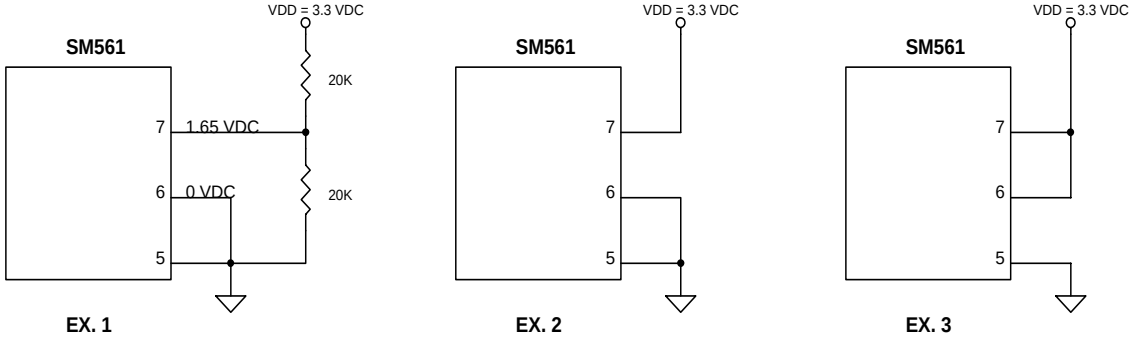


Figure 1.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}): ..... –0.5V to +6.0V
DC Input Voltage: ..... –0.5V to V_{DD} + 0.5V
Junction Temperature ..... –40°C to +140°C
Operating Temperature: ..... 0°C to 70°C
Storage Temperature ..... –65°C to +150°C
Static Discharge Voltage(ESD) 2,000V–Min

DC Electrical Characteristics (V_{DD} = 3.3V, Temp. = 25°C and C_L (pin 4) = 15 pF, unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VDD	Power Supply Range	± 10%	2.97	3.3	3.63	V
VINH	Input High Voltage	S0 and S1 only	$0.85V_{DD}$	V_{DD}	V_{DD}	V
VINM	Input Middle Voltage	S0 and S1 only	$0.40V_{DD}$	$0.50V_{DD}$	$0.60V_{DD}$	V
VINL	Input Low Voltage	S0 and S1 only	0.0	0.0	$0.15V_{DD}$	V
VOH1	Output High Voltage	I_{OH} = 6 ma	2.4			V
VOH2	Output High Voltage	I_{OH} = 20 ma	2.0			V
VOL1	Output Low Voltage	I_{OH} = 6 ma			0.4	V
VOL2	Output Low Voltage	I_{OH} = 20 ma			1.2	V
Cin1	Input Capacitance	Xin/CLK (pin 1)	3	4	5	pF
Cin2	Input Capacitance	Xout (pin 8)	6	8	10	pF
Cin2	Input Capacitance	S0, S1, SSCC (pins 7, 6, 5)	3	4	5	pF
IDD1	Power Supply Current	FIN = 65 MHz		35	45	mA
IDD2	Power Supply Current	FIN = 166 MHz		50	55	mA

Electrical Timing Characteristics (V_{DD} = 3.3V, T = 25°C and C_L=15 pF, unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ICLKFR	Input Clock Frequency Range	V_{DD} = 3.30V	54		166	MHz
Trise	Clock Rise Time (pin 4)	SSCLK1 @ 0.4 – 2.4V	1.2	1.4	1.6	ns
Tfall	Clock Fall Time (pin 4)	SSCLK1 @ 0.4 – 2.4V	1.2	1.4	1.6	ns
DTYin	Input Clock Duty Cycle	XIN/CLK (pin 1)	20	50	80	%
DTYout	Output Clock Duty Cycle	SSCLK1 (pin 4)	45	50	55	%
JCC1	Cycle-to-Cycle Jitter	Fin = 140 MHz	–	125	175	ps
JCC2	Cycle-to-Cycle Jitter	Fin = 140 MHz	–	150	200	ps

Note:
1. **Single Power Supply:** The Voltage on any input or I/O pin cannot exceed the power pin during power up.

SSCG Theory of Operation

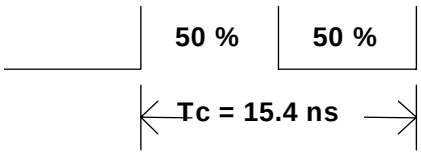
The SM561 is a PLL-type clock generator using a proprietary Cypress design. By precisely controlling the bandwidth of the output clock, the SM561 becomes a Low EMI clock generator. The theory and detailed operation of the SM561 will be discussed in the following sections.

EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of this 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e., third, fifth, seventh, etc. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI have been to use shielding, filtering, multilayer PCBs, etc. The SM561 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM561 takes a narrow band digital reference clock in the range of 54–166 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 65-MHz clock with a 50% duty cycle. From a 65-MHz clock we know the following, as illustrated here.



Clock Frequency = fc = 65 MHz
Clock Period = Tc =1/65 MHz = 15.4 ns

If this clock is applied to the Xin/CLK pin of the SM561, the output clock at pin 4 (SSCLK) will be sweeping back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate to total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition from F1 to F2, the amount of time and sweep waveform play a very important role in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. *Figure 1* also shows the modulation profile of a 65-MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. *Figure 2* is a scan of the same SSCG clock using a spectrum analyzer. In this scan you can see a 6.48-dB reduction in the peak RF energy when using the SSCG clock.

Modulation Rate

Spectrum Spread Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmr. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.

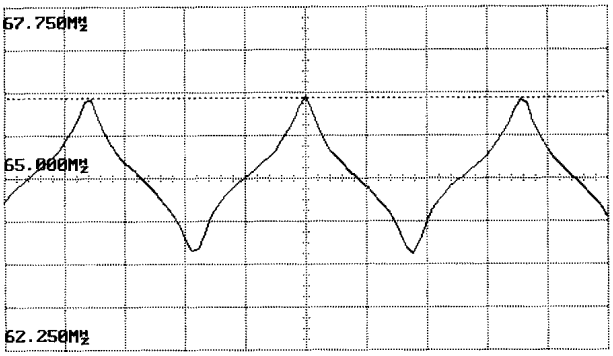
The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. The SM560 and SM561 have a fixed divider count, as listed below.

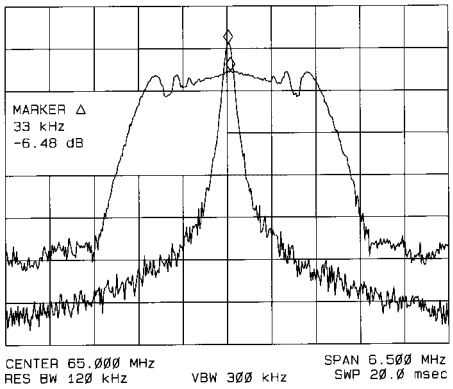
Device	Cdiv	
SM561	2332	(All Ranges)

Example:

Device = SM561
Fin = 65 MHz
Range = S1 = 1, S0 = 0
Then;

Modulation Rate = Fmod = 65 MHz/2332 = 27.9 kHz.





Modulation Profile **Spectrum Analyzer**

Figure 2. SSCG Clock, SM561, Fin = 65 MHz

SM560 Application Schematic

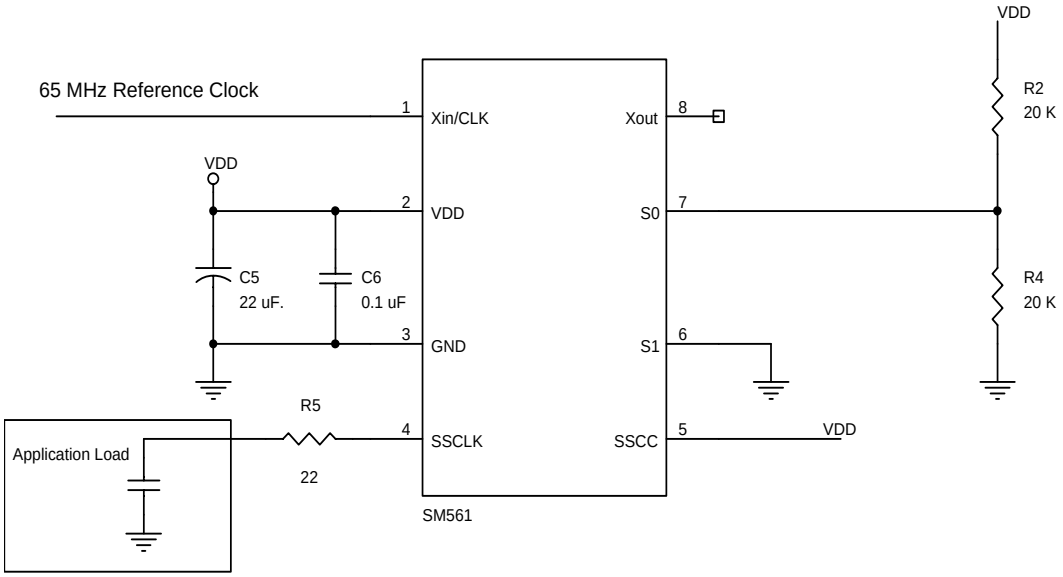


Figure 3. Application Schematic

The schematic in *Figure 3* demonstrates how SM561 is configured in a typical application. This application uses a 65-MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (Xout) is left unconnected.

Figure 3 also demonstrates how to properly use the Tri-level Logic employed in the SM561. Note that resistors R2 and R4 create a voltage divider that places VDD/2 on pin 7 to satisfy the voltage requirement for an “M” state.

With this configuration, the SM561 will produce an SSCG clock that is at a center frequency of 65 MHz. Referring to *Table 1*, range “0, M” at 65 MHz will generate a modulation profile that has a 1.7% peak to peak spread.

Ordering Information [2]

Part Number	Package Type	Product Flow
IMISM561BZ	8-pin SOIC	Commercial, 0° to 70°C
IMISM561BZT	8-pin SOIC–Tape and Reel	Commercial, 0° to 70°C

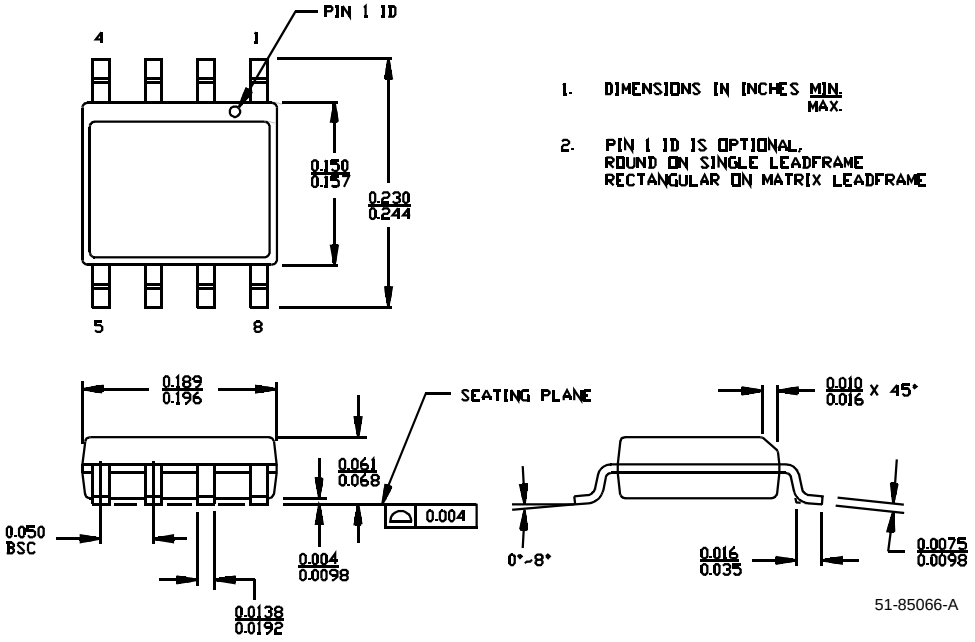
Package Drawing and Dimensions

Marking: Example: IMI
SM561BS
Date Code, Lot#

SM561 B S

- Package S = SOIC
- Revision
- IMI Device Number

8-lead (150-Mil) SOIC S8



Note:
2. The ordering part number differs from the marking on the actual device.

Document History Page

Document Title:SM561 Spread Spectrum Clock Generator Document Number: 38-07021				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106949	06/05/01	IKA	Convert from IMI to Cypress
*A	113521	05/08/02	DMG	Package suffix changed
*B	119446	10/17/02	RGL	Corrected the values in the Absolute Maximum Ratings to match the device.
*C	122676	12/14/02	RBI	Add power up requirements to operating conditions information.