

# IMP705/6/7/8, 813L

#### POWER MANAGEMENT

## Low-Power µP Supervisor Circuits

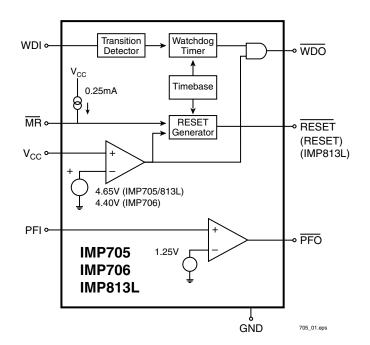
- Watchdog timer
- Brownout detection
- Power supply monitor

The IMP705/706/707/708 and IMP813L CMOS supervisor circuits monitor power-supply and battery voltage level, and  $\mu P/\mu C$  operation. Compared to pin-compatible devices offered by Maxim Integrated Products, IMP devices feature 60 percent lower maximum supply current.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions. A reset is generated when the supply drops below 4.65V (IMP705/707/813L) or 4.40V (IMP706/708). For 3V power supply applications, refer to the IMP705P/R/S/T data sheet. In addition, the IMP705/706/813L feature a 1.6 second watchdog timer. The IMP707/708 have both active-HIGH and active-LOW reset outputs but no watchdog function. The IMP813L has the same pin-out and functions as the IMP705 but has an active-HIGH reset output. A versatile power-fail circuit has a 1.25V threshold, useful in checking battery levels and non-5V supplies. All devices have a manual reset  $(\overline{\rm MR})$  input. The watchdog timer output will trigger a reset if connected to  $\overline{\rm MR}$ .

All devices are available in 8-pin DIP, SO and MicroSO packages.

## **Block Diagrams**

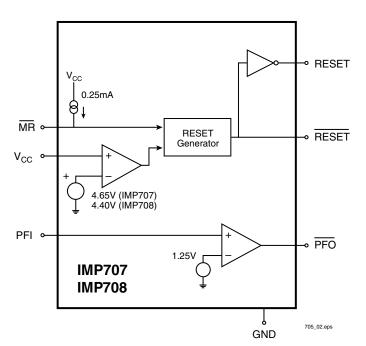


#### **Key Features**

- Improved replacements for the Maxim MAX705/6/7/8, MAX813L
  - 140µA maximum supply current
  - 60% improvement
- ◆ Precision power supply monitor
  - 4.65V threshold (IMP705/707/813L)
  - 4.40V threshold (IMP706/8)
- Debounced manual reset input
- **♦** Voltage monitor
  - 1.25V threshold
  - Battery monitor/Auxiliary supply monitor
- ♦ Watchdog timer (IMP705/706/813L)
- ♦ 200ms reset pulse width
- ◆ Active HIGH reset output (IMP707/708/813L)
- ♦ MicroSO package

#### **Applications**

- Computers and embedded controllers
- ◆ Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment





## **Pin Configuration**

#### **MicroSO** DIP/SO RESET (RESET) 1 8 WDI MR 1 8 RESET MR 1 8 WDO RESET 1 8 NC 7 RESET (RESET) WDO 2 7 PFO V<sub>CC</sub> 2 IMP707 7 RESET V<sub>CC</sub> 2 IMP705 RESET 2 IMP707 7 PFO IMP708 IMP706 IMP708 IMP706 GND 3 6 NC GND 3 6 WDI MR 3 6 PFI MR 3 6 PFI (IMP813L) (IMP813L) 5 PFO PFI 4 5 PFO V<sub>CC</sub> 4 5 GND PFI 4 V<sub>CC</sub> 4 5 GND

## **Ordering Information**

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package					
IMP705 Active LOW Reset, Watchdog Output and Manual RESET								
IMP705CPA	4.65	0°C to +70°C	8-Plastic DIP					
IMP705CSA	4.65	0°C to +70°C	8-SO					
IMP705CUA	4.65	0°C to +70°C	8-MicroSO					
IMP705C/D	4.65	25°C	Dice					
IMP705EPA	4.65	-40°C to +85°C	8-Plastic DIP					
IMP705ESA	4.65	-40°C to +85°C	8-SO					
IMP706ESA	4.40	-40°C to +85°C	8-SO					
IMP706 Active LOW Reset, W	atchdog Output and Manua	al RESET						
IMP706CPA	4.40	0°C to +70°C	8-Plastic DIP					
IMP706CSA	4.40	0°C to +70°C	8-SO					
IMP706CUA	4.40	0°C to +70°C	8-MicroSO					
IMP706C/D	4.40	25°C	Dice					
IMP706EPA	4.40	-40°C to +85°C	8-Plastic DIP					
IMP706ESA	4.40	-40°C to +85°C	8-SO					
IMP707 Active LOW & HIGH Reset with Manual RESET								
IMP707CPA	4.65	0°C to +70°C	8-Plastic DIP					
IMP707CSA	4.65	0°C to +70°C	8-SO					
IMP707CUA	4.65	0°C to +70°C	8-MicroSO					
IMP707C/D	4.65	25°C	Dice					
IMP707EPA	4.65	-40°C to +85°C	8-Plastic DIP					
IMP707ESA	4.65	-40°C to +85°C	8-SO					
IMP708 Active LOW & HIGH	Reset with Manual RESET							
IMP708CPA	4.40	0°C to +70°C	8-Plastic DIP					
IMP708CSA	4.40	0°C to +70°C	8-SO					
IMP708CUA	4.40	0°C to +70°C	8-MicroSO					
IMP708C/D	4.40	25°C	Dice					
IMP708EPA	4.40	-40°C to +85°C	8-Plastic DIP					
IMP708ESA	4.40	−40°C to +85°C	8-SO					
IMP813L Active HIGH Reset,	Watchdog Output and Man	ual RESET						
IMP813LCPA	4.65	0°C to +70°C	8-Plastic DIP					
IMP813LCSA	4.65	0°C to +70°C	8-SO					
IMP813LCUA	4.65	0°C to +70°C	8-MicroSO					
IMP813LC/D	4.65	25°C	Dice					
IMP813LEPA	4.65	-40°C to +85°C	8-Plastic DIP					
IMP813LESA	4.65	-40°C to +85°C	8-SO					



## **Absolute Maximum Ratings**

rin terminal voltage with Respect to Groun	Voltage with Respect to Grou	Res	with	Voltage	ıal	<b>Termin</b>	Pin
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V <sub>CC</sub>	. −0.3V to 6.0V
All other inputs <sup>1</sup>	$-0.3V$ to $(V_{CC} + 0.3V)$
Input Current at V <sub>CC</sub> and GND	. 20mA
Output Current: All outputs	. 20mA
Rate of Rise at V <sub>CC</sub>	. 100V/μs
Plastic DIP Power Dissipation	. 700 mW
(Derate 9 mW/°C above 70°C)	
SO Power Dissipation	. 470 mW
(Derate 5.9 mW/°C above 70°C)	
MicroSO Power Dissipation	. 330mW
(Derate 4.1 mW/°C above 70°C)	

#### **Operating Temperature Range**

IMP705E/706E/707E/708E/813LE	−40°C to 85°C
IMP706C/707C/708C/813LC	0°C to 70°C
Storage Temperature Range	-65°C to 160°C
Lead Temperature Soldering(10 sec)	300°C

Note: 1. The input voltage limits on PFI and  $\overline{MR}$  can be exceeded if the input current is less than 10mA.

These are stress ratings only and functional operation is not implied.

#### **Electrical Characteristics**

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Unless otherwise noted,  $V_{CC} = 4.75 \text{V}$  to 5.5V for the IMP705/707/813L.  $V_{CC} = 4.5 \text{V}$  to 5.5V for the IMP706/708 and over the operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage Range V <sub>CC</sub> IMP705/6/7/8C		IMP705/6/7/8C	1.2		5.5	V
		IMP813L	1.1		5.5	
		IMP705/6/7/8E, IMP813IE	1.2		5.5	
Supply Current	I <sub>CC</sub>	IMP705C/706C/813LC		75	140	μА
		IMP705E, IMP706E, IMP813LE		75	140	
		IMP707C, IMP708C		50	140	
		IMP707E, IMP708E		50	140	
RESET Threshold	V <sub>RT</sub>	IMP705, IMP707, IMP813L, Note 2	4.50	4.65	4.75	V
		IMP706, IMP708, Note 2	4.25	4.40	4.50	
RESET Threshold Hysteresis		Note 2		40		mV
RESET Pulse Width	t <sub>RS</sub>	Note 2	140	200	280	ms
MR Pulse Width	t <sub>MR</sub>		0.15			μs
MR to RESET Out Delay	t <sub>MD</sub>	Note 2			0.25	μs
MR Input Threshold	V <sub>IH</sub>		2.0			V
	V <sub>IL</sub>				8.0	
MR Pull-up Current		MR = 0V	100	250	600	μΑ
RESET Output Voltage		I <sub>SOURCE</sub> = 800μA	V <sub>CC</sub> - 1.5V			V
		$I_{SINK} = 3.2mA$			0.4	
		IMP705/6/7/8, $V_{CC} = 1.2V$ , $I_{SINK} = 100\mu A$			0.3	
RESET Output Voltage		IMP707/708/813L, $I_{SOURCE} = 800\mu A$	V <sub>CC</sub> - 1.5V			V
		IMP707/708, I <sub>SINK</sub> = 1.2mA			0.4	
		IMP813L, I <sub>SINK</sub> = 3.2mA			0.4	
		IMP813L, $V_{CC} = 1.2V$ , $I_{SOURCE} = 4\mu A$	0.9			
Watchdog Timeout Period	t <sub>WD</sub>	IMP705/706/813L	1.00	1.60	2.25	s
WDI Pulse Width	t <sub>WP</sub>	$V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}$	50			ns
WDI Input Threshold	V <sub>IH</sub>	IMP705/706/813L, V <sub>CC</sub> = 5V	3.5			V
	$V_{IL}$				0.8	
WDI Input Current		IMP705/706/813L, WDI = V <sub>CC</sub>		50	150	μΑ
		IMP705/706/813L, WDI = 0V	-150	-50		
WDO Output Voltage		IMP705/706/813L, $I_{SOURCE} = 800\mu A$	V <sub>CC</sub> - 1.5V			V
		IMP705/706/813L, I <sub>SINK</sub> = 1.2mA			0.4	
PFI Input Threshold		$V_{CC} = 5V$	1.2	1.25	1.3	V
PFI Input Current			-25	0.01	25	nA
PFO Output Voltage		I <sub>SOURCE</sub> = 800μA	V <sub>CC</sub> - 1.5V			V
		$I_{SINK} = 3.2mA$			0.4	

*Notes:* 2. RESET (IMP705/6/7/8), RESET (IMP707/8, IMP813L)



## **Pin Descriptions**

		Pin N	umber				
IMP70			07/708	IMP8			
DIP/SO	MicroSO	DIP/SO	MicroSO	DIP/SO	MicroSO	Name	Function
1	3	1	3	1	3	MR	Manual RESET input. The active LOW input triggers a reset pulse. A 250μA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	2	4	2	4	V <sub>CC</sub>	+5V power supply input.
3	5	3	5	3	5	GND	Ground reference for all signals.
4	6	4	6	4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, PFO goes low. Connect PFI to ground or V <sub>CC</sub> when not used.
5	7	5	7	5	7	PFO	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	_	_	6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting WDO LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge.
_	_	6	_	_	_	NC	Not connected.
7	1	7	1	_	_	RESET	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays low whenever $V_{CC}$ is below the reset threshold (IMP705: 4.65V, IMP705J: 4.00V, IMP706: 4.40V). $\overline{RESET}$ remains LOW for 200ms after $V_{CC}$ rises above the RESET threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$ .
8	2	_	_	8	2	WDO	Watchdog output. WDO pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when V <sub>CC</sub> is below the reset threshold, WDO remains low. Unlike RESET, WDO does not have a minimum pulse width and as soon as V <sub>CC</sub> exceeds the reset threshold, WDO goes HIGH with no delay.
	_	8	2	7	1	RESET	Active-HIGH reset output. RESET is the inverse of RESET. The IMP813L has only a RESET output.

## Feature Summary

	IMP705	IMP706	IMP707	IMP708	IMP813L
Power-fail detector					
Brownout detection					
Manual RESET input					
Power-up/down RESET					
Watchdog timer					
Active-HIGH RESET output					
Active-LOW RESET output					
RESET threshold	4.65V/4.00V	4.40V	4.65V	4.40V	4.65V



#### **Detail Descriptions**

#### **RESET/RESET Operation**

The RESET/RESET signals are designed to start a  $\mu P/\mu C$  in a known state or return the system to a known state.

The IMP707/708 have two RESET outputs, one active-HIGH RESET and one active-LOW RESET output. The IMP813L has only an active-HIGH output. RESET is simply the complement of  $\overline{\text{RESET}}$ .

RESET is guaranteed to be LOW with  $V_{CC}$  above 1.2V. During a power-up sequence,  $\overline{RESET}$  remains low until the supply rises above the threshold level, either 4.65V, 4.40V or 4.00V.  $\overline{RESET}$  goes high approximately 200ms after crossing the threshold.

During power-down,  $\overline{RESET}$  goes LOW as  $V_{CC}$  falls below the threshold level and is guaranteed to be under 0.4V with  $V_{CC}$  above 1.2V.

In a brownout situation where  $V_{CC}$  falls below the threshold level,  $\overline{RESET}$  pulses low. If a brownout occurs during an already-initiated reset, the pulse will continue for a minimum of 140ms.

#### **Auxiliary Comparator**

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output  $(\overline{PFO})$  and noninverting input  $(\overline{PFI})$ . This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the  $\overline{PFO}$  output to transit LOW. Normally  $\overline{PFO}$  interrupts the processor so the system can be shut down in a controlled manner.

#### Manual Reset (MR)

The active-LOW manual reset input is pulled high by a  $250\mu A$  pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output  $(\overline{WDO})$  and  $\overline{MR}$ , a watchdog timeout forces  $\overline{RESET}$  to be generated. The IMP813L should be used when an active-HIGH RESET is required.

#### **Watchdog Timer**

The watchdog timer available on the IMP705/706/813L monitors  $\mu P/\mu C$  activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output,  $\overline{WDO}$ , into a LOW state.  $\overline{WDO}$  will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

 $\overline{WDO}$  will also become LOW and remain so, whenever the supply voltage,  $V_{CC}$ , falls below the device threshold level.  $\overline{WDO}$  goes HIGH as soon as  $V_{CC}$  transitions above the threshold. There is no minimum pulse width for  $\overline{WDO}$  as there is for the RESET outputs. If WDI is floated,  $\overline{WDO}$  essentially acts as a low-power output indicator.

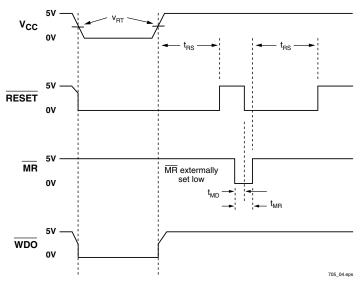


Figure 1. WDI Three-state operation

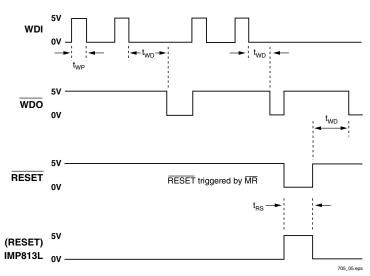


Figure 2. Watchdog Timing



#### **Application Information**

#### Ensuring That $\overline{RESET}$ is Valid Down to $V_{CC} = 0V$

When  $V_{CC}$  falls below 1.1V, the IMP705-708  $\overline{RESET}$  output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force  $\overline{RESET}$  to the wrong state, a pull-down resistor should be connected to the  $\overline{RESET}$  pin, thus draining such charges to ground and holding RESET low. The resistor value is not critical. A  $100k\Omega$  resistor will pull  $\overline{RESET}$  to ground without loading it.

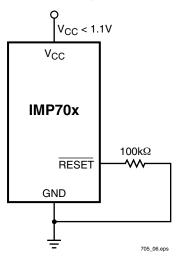


Figure 3. Ensuring That  $\overline{RESET}$  is Valid Down to  $V_{CC} = 0V$ 

#### **Bi-directional Reset Pin Interfacing**

The IMP705/6/7/8 can interface with  $\mu P/\mu C$  bi-directional reset pins by connecting a 4.7k $\Omega$  resistor in series with the RESET output and the  $\mu P/\mu C$  bi-directional RESET pin.

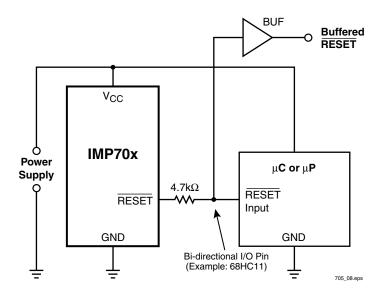


Figure 3. Bi-directional Reset Pin Interfacing



#### Monitoring Voltages Other Than V<sub>CC</sub>

The IMP705-708 can monitor voltages other than  $V_{CC}$  using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input, PFI, the  $\overline{PFO}$  (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and  $\overline{PFO}$  pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a RESET in addition to the  $\overline{PFO}$  flag, this may be achieved by connecting the  $\overline{PFO}$  output to  $\overline{MR}$ .

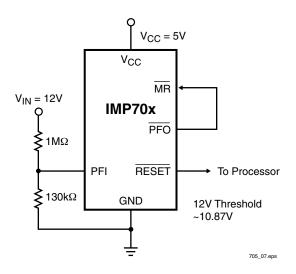


Figure 4. Monitoring Voltages Other Than  $V_{CC}$ 

### **Application Information**

#### Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK,  $\overline{PFO}$  will be LOW, and when the negative rail is failing (not negative enough),  $\overline{PFO}$  goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The  $\overline{RESET}$  output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the  $V_{CC}$  line, the PFI threshold tolerance, and the resistors.

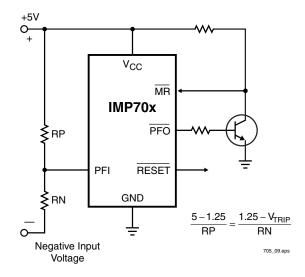
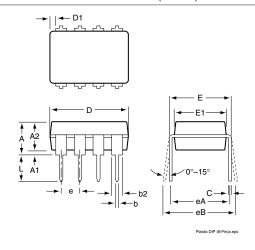


Figure 5. Monitoring a Negative Voltage

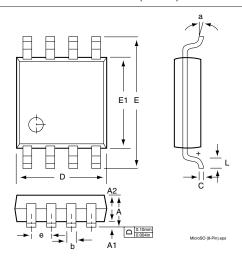


## **Package Dimensions**

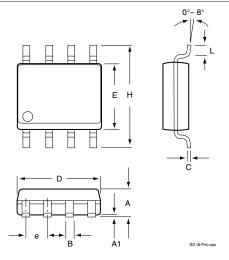
Plastic DIP (8-Pin)\*



MicroSO (8-Pin)\*\*



SO (8-Pin)\*\*\*



	Inc	hes	Millimeters					
	Min	Max	Min	Max				
Plastic DIP (8-Pin)								
Α		0.210		5.33				
A1	0.015		0.38					
A2	0.115	0.195	2.92	4.95				
b	0.014	0.022	0.36	0.56				
b2	0.045	0.070	1.14	1.78				
b3	0.030	0.045	0.80	1.14				
D	0.355	0.400	9.02	10.16				
D1	0.005		0.13					
Е	0.300	0.325	7.62	8.26				
E1	0.240	0.280	6.10	7.11				
е	0.100		2.5	54				
eА	0.300		7.0	62				
еВ		0.430		10.92				
еC		0.060						
L	0.115	0.150	2.92	3.81				
		MicroSO	) (8-Pin)					
Α		0.0433		1.10				
A1	0.0020	0.0059	0.050	0.15				
A2	0.0295	0.0374	0.75	0.95				
b	0.0098	0.0157	0.25	0.40				
С	0.0051	0.0091	0.13	0.23				
D	0.1142	0.1220	2.90	3.10				
е	0.025	6 BSC	0.65 BSC					
Е	0.193	BSC	4.90 BSC					
E1	0.1142	0.1220	2.90	3.10				
L	0.0157	0.0276	0.40	0.70				
а	0°	6°	0°	6°				
		SO (8	3-Pin)					
Α	0.053	0.069	1.35	1.75				
A1	0.004	0.010	0.10	0.25				
В	0.013	0.020	0.33	0.51				
С	0.007	0.010	0.19	0.25				
е	0.0	050	1.2	27				
Е	0.150	0.157	3.80	4.00				
Н	0.228	0.244	5.80	6.20				
L	0.016	0.050	0.40	1.27				
D	0.189	0.197	4.80	5.00				

<sup>\*</sup> JEDEC Drawing MS-001BA \*\* JEDEC Drawing MO-187AA \*\*\* JEDEC Drawing MS-012AA





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