IN16C01
16-BIT RISC MICROCONTROLLER

1. Introduction

The IN16C01 is a CMOS single-chip 16-bit microcontroller.
The IN16C01 is a general purpose microcomputer and can be used in control systems, data acquisition systems and DSP systems. Low-power and fully static operation allow to use the microcontroller in self-contained systems with limited power consumption.
On the base of its capabilities the IN16C01 could be compared with the next general-purpose microcontrollers: Intel's 80C196 and 80C186, Motorola's 68300 and 68HC16, Siemens' SAB 80C16x. The IN16C01 has an array multiplier and dedicated hardware for DSP operations support, which allows to compare the microcontroller with the next DSP: Texas Instruments' TMS320C25, Motorola's DSP561xx, Analog Devices' ADSP21xx.
The IN16C01 implements the modular architecture when there is a common internal bus to which all other units are connected. The architecture allows to 'tailor' the microcontroller to an appropriate customer's application. The basic set of the microcontroller units includes:

- Microprocessor
- RAM
- ROM
- Timers
- UART
- Synchronous Serial Interface (SSI)
- Bi-directional Parallel Ports

The microcontroller is assumed to be extended with ADC, EEPROM, PWM unit, I^2C interface and other units in future.

2. Architectural Overview

A simplified functional block diagram of the IN16C01 microcontroller is shown in fig.2.1.

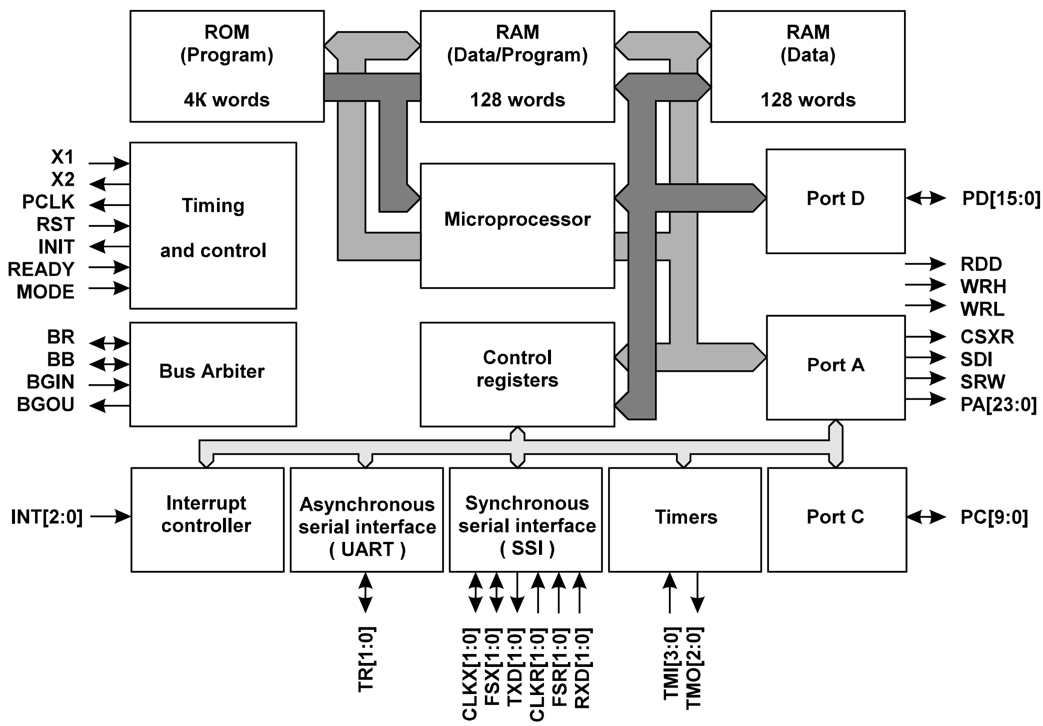

Fig. 2.1. Simplified functional block diagram of the IN16C01

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As one can see in the figure the microcontroller consists of the following units:

- CPU core
- RAM
- PROM
- Timer system (counter/timer, watchdog timer)
- UART
- Synchronous serial interface (SSI)
- Parallel ports D, C

The IN16C01 is a synchronous VLSI with fully static operation, i.e. the microcontroller's clock may be shut off indefinitely without the device losing its state. Once the clock is restored the microcontroller will begin executing as if there had been no interruption.

The current IN16C01 realisation is assumed to have the maximum clock frequency of 10 MHz.

2.1 CPU core

The brains of the IN16C01 is the CPU core.

Main CPU core features are:

- Stack oriented RISC architecture
- 24-bit address
- 16/32-data
- Modified Harvard architecture with independent simultaneous access to the program and data spaces
- Two data stacks of 8 sixteen-bit words each
- Sixteen 24 bit words for return stack
- Eight 24 bit words for address stack
- All instructions are executed in one or two clock cycles
- Interrupt response of two clock cycles
- 16x16 multiply in one clock cycle
- Multiply-accumulate (with 38 bit accumulator) in two clock cycles
- Divide operation support

The stack oriented architecture means that the processed data are stored in a stack (the data stack). Vast majority of the microcontroller's instructions use one or two top stack words as their operands. The particular feature of the IN16C01 is that it has four stacks: two stacks for data, a return stack and an address stack. All the stacks can operate simultaneously. *The data stacks* contain processed data. *The return stack* contains 'return from subroutine' addresses or variables addresses. *The address stack* contains variables addresses.

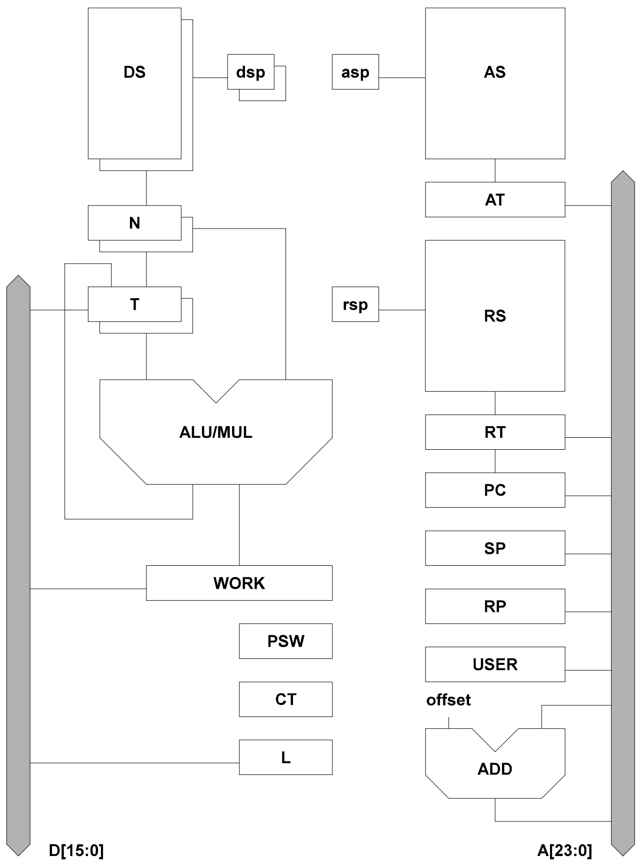

Fig. 2.2. Block diagram of the CPU core

The block diagram of the CPU core is shown in fig. 2.2. As one can see from the figure, the CPU contains the following units:

DS

The data stack. The stack consists of *internal stack memory* (two fields of eight 16-bit words) and the 'top' and 'next' registers: T and N.

T

The 32-bit 'top' register of the data stack. The register is accessible as a 16-bit register (**t** or **%t**) or a 32-bit register (**T).** The register is always used as one of the ALU operands.

N

The 32-bit 'next' register of the data stack. The register is always used as the second ALU operand and is employed for arithmetic operations.

The data, written into the data stack memory, are always taken from the N register. The data, read from the data stack memory, are written into the N register. The N register can be moved into the T register via the ALU. During the data stack push operation, the T register can be written directly into the N register.

Move operations between the T and N registers and between the N register and the data stack are independent from each other and can be executed simultaneously.

RS

The return stack. The stack consists of *internal return stack memory* of sixteen 24-bit words and the RT register. The return stack is accessible via the RT register only.

RT

The 24-bit 'top' register of the return stack. During RT register read, the return stack can be 'popped'. During RT register write, the return stack can be 'pushed'. The RT register is used in subroutine calls and return from subroutine instructions, and to local variables storing as well.

AS

The address stack. The stack consists of *internal address stack memory* of eight 24-bit words and the AT register. The address stack is accessible via the AT register only.

AT

The 24-bit 'top' register of the address stack. The register stores variables' addresses. During AT register read, the address stack can be 'popped'. During RT register write, the address stack can be 'pushed'.

asp, dsp, rsp

The address, data and return stacks' pointers. These registers are not accessible to software.

L

The 16-bit instruction register.

PC

The 24-bit program counter.

CT

The 16-bit general purpose register. The register can be used as a counter. The register contents can be analysed by conditional branch instructions and can be decremented concurrently with an ALU operation. The register is used as a counter in flow mode instructions.

USER

The 24-bit address register. The register's contents are used as a *base address* during external registers access.

SP

The 24-bit general purpose register. The register can contain an address and can be used to address *the data memory* as well.

RP

The 24-bit general purpose register. The register can contain an address and can be used to address *the data memory* as well.

WORK

The 32-bit general purpose register. The register can be used in integer multiply and multiply-accumulate operations.

ALU

The 16-bit *arithmetic-logic unit* with a multiplier. The ALU's two operands are the T and N registers.

PSW

16-bit processor status word..

2.2 Memory

The microcontroller address space is divided into *data* and *program* memory. The IN16C01 accesses the internal data and program memories concurrently using separate buses. An external memory access is accomplished via common bus with separate address and data. The SDI input signal defines the type of the space selected (data or program). The internal data memory can not be modified.

The CPU core addresses 16-bit words in memory. One clock cycle is needed to read or write a memory word.

The microcontroller supports a possibility to write high/low bytes in a 16-bit word. There are special prefixes in the IN16C01 instruction set: **BYTE_L** and **BYTE_H.** These prefixes control WRL and WRH signals.

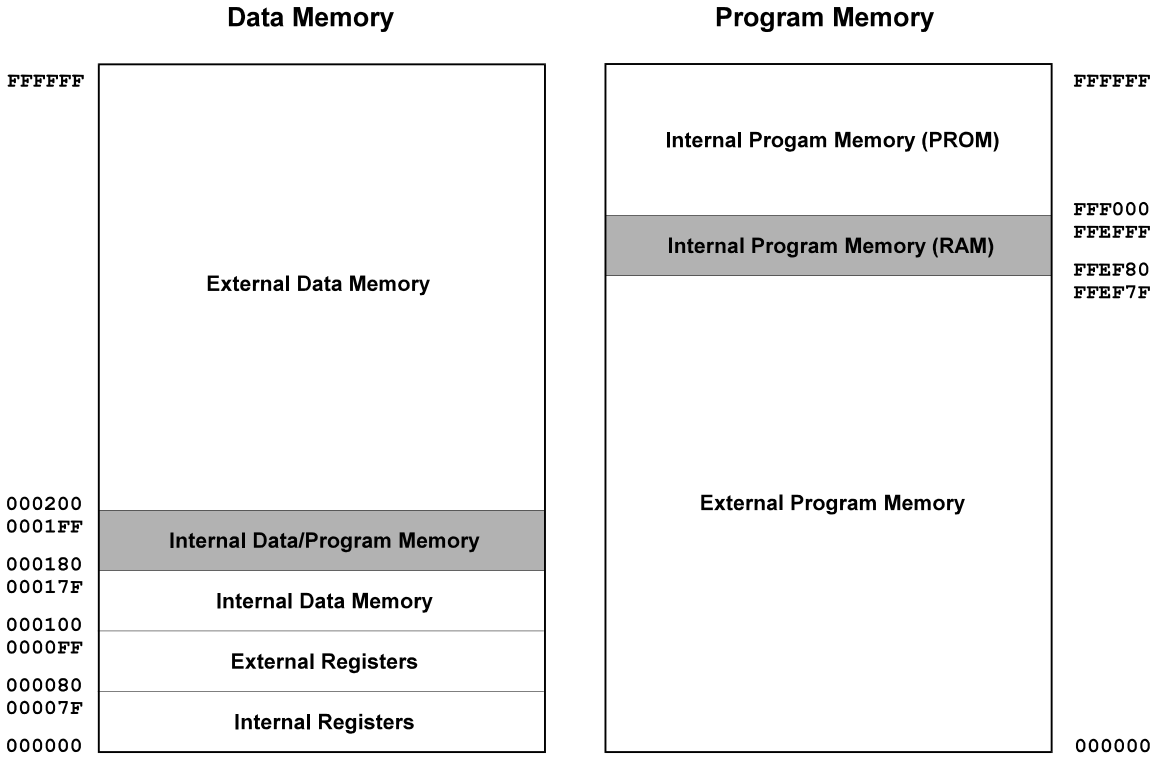

Fig 2.3. Memory Map of the IN16C01

3 The Microcontroller Pins

The IN16C01 is available in PQFP 100 package (see fig. 3.1.).

Table 5.1. The IN16C01 pin assignment

Pin number	Mnemonic	In/Out	Function
1	TXD_R	in/out	transmitter's data SSI_R
2	VDD		supply
3	VSS		ground
4	CLKX_R	in/out	transmitter's clock SSI_R
5	FSX_L	in/out	transmitter's clock SSI_L
6	TXD_L	in/out	transmitter's data SSI_L
7	CLKX_L	in/out	transmitter's clock SSI_L
8	CLKR_L	in	receiver's clock SSI_L
9	FSR_L	in	receiver's clock SSI_L
10	RXD_L	in	receiver's data SSI_L
11	PD15	in/out	15-th bit of the D port
12	PD14	in/out	14-th bit of the D port
13	PD13	in/out	13-th bit of the D port
14	PD12	in/out	12-th bit of the D port
15	PD11	in/out	11-th bit of the D port
16	PD10	in/out	10-th bit of the D port
17	PD9	in/out	9-th bit of the D port
18	PD8	in/out	8-th bit of the D port

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Pin number	Mnemonic	In/Out	Function
19	PD7	in/out	7-th bit of the D port
20	PD6	in/out	6-th bit of the D port
21	PD5	in/out	5-th bit of the D port
22	PD4	in/out	4-th bit of the D port
23	PD3	in/out	3-rd bit of the D port
24	PD2	in/out	2-nd bit of the D port
25	PD1	in/out	1-st bit of the D port
26	PD0	in/out	0-th bit of the D port
27	VDD		supply
28	VSS		ground
29	SDI	out	data/program input
30	CSXR	out	external device select
31	SRW	out	port D read/write
32	PA0	out	0-th bit of the A port
33	PA1	out	1-st bit of the A port
34	PA2	out	2-nd bit of the A port
35	PA3	out	3-th bit of the A port
36	PA4	out	4-th bit of the A port
37	PA5	out	5-th bit of the A port
38	PA6	out	6-th bit of the A port
39	PA7	out	7-th bit of the A port
40	PA8	out	8-th bit of the A port
41	PA9	out	9-th bit of the A port
42	PA10	out	10-th bit of the A port
43	PA11	out	11-th bit of the A port
44	PA12	out	12-th bit of the A port
45	PA13	out	13-th bit of the A port
46	PA14	out	14-th bit of the A port
47	PA15	out	15-th bit of the A port
48	PA16	out	16-th bit of the A port
49	PA17	out	17-th bit of the A port
50	PA18	out	18-th bit of the A port
51	PA19	out	19-th bit of the A port
52	VDD		supply
53	VSS		ground
54	PA20	out	20-th bit of the A port
55	PA21	out	21-th bit of the A port
56	PA22	out	22-th bit of the A port
57	PA23	out	23-th bit of the A port
58	RT0	in/out	transmitter’s data SCI.
59	RT1	in/out	receiver’s data SCI.
60	PC0	in/out	0-th bit of the C port
61	PC1	in/out	1-st bit of the C port
62	PC2	in/out	2-nd bit of the C port
63	PC3	in/out	3-rd bit of the C port

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Pin number	Mnemonic	In/Out	Function
64	PC4	in/out	4-th bit of the C port
65	PC5	in/out	5-th bit of the C port
66	PC6	in/out	6-th bit of the C port
67	PC7	in/out	7-th bit of the C port
68	PC[8]	in/out	8-th bit of the C port
69	PC[9]	in/out	9-th bit of the C port
70	INT2	in	interrupt request
71	INT1	in	interrupt request
72	INT0	in	interrupt request
73	MODA	in	mode A
74	TMI3	in	timer 3 control
75	MODE	in	mode E
76	X1	in	microcontroller's clock in
77	VDD		supply
78	VSS		ground
79	X2	out	microcontroller's clock out
80	TMO0	out	timer 0 output
81	TMO1	out	timer 1 output
82	TMO2	out	timer 2 output
83	PCLK	out	microcontroller's clock out
84	INIT	out	reset output
85	READY	in	data ready
86	TMI2	in	timer 2 control
87	TMI1	in	timer 1 control
88	TMI0	in	timer 0 control
89	RST	in	reset
90	BB	in/out	external bus hold
91	BR	in/out	external bus request
92	BGIN	in	external bus grant
93	BGOU	out	external bus grant
94	RDD	out	port D read
95	WRH	out	port D write
96	WRL	out	port D write
97	CLKR_R	in	receiver's clock SSI_R
98	FSR_R	in	receiver's clock SSI_R
99	RXD_R	in	receiver's data SSI_R
100	FSX_R	in/out	transfer clock SSI_R

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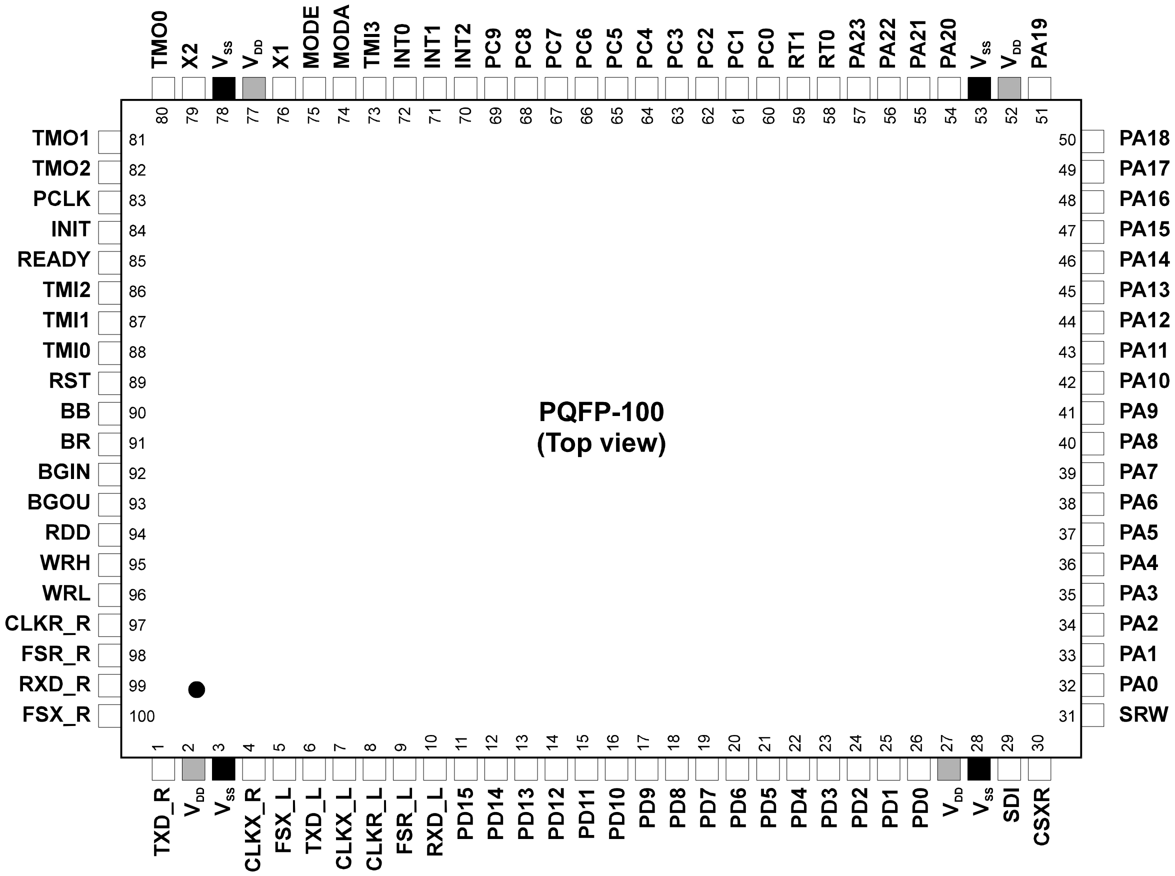

Fig. 3.1. The IN16C01 pin assignment

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