1. Description

IN16C554A is an enhanced quadruple version of the 16C550UART (Universal Asynchronous Receiver Transmitter). IN16C554A is in part an upgrade version of IN16C554, as it is designed for 3.3V only and has AUTO-CTS, AUTO-RTS functions.

In IN16C554A, Each channel can be put into FIFO mode to relieve the CPU of excessive software overhead. In this mode, internal FIFOs are activated and 16 bytes plus 3 bit of error data per byte can be stored in both receive and transmit modes.

Each channel performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. The Status information includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions such as parity, overrun, framing, and break interrupt.

IN16C554A includes a programmable baud rate generator which is capable of dividing the timing reference clock input by divisors of 1 to 2^{16}-1, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this clock to drive the receiver logic.IN16C554A has complete MODEM-control capability and an interrupt system that can be programmed to the user's requirements, minimizing the computing required to handle the communication links. Moreover IN16C554A can select hardware flow control. Hardware flow control significantly reduces software overhead and increases system efficiency.

2. Features

- In the FIFO mode, Each channel's transmitter and receiver is buffered with 16-byte FIFO to reduce the number of interrupts to CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, parity) to or from the serial data.
- Holding Register and Shift Register eliminate need for precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status and data interrupts.
- Programmable Baud Rate Generators which allow division of any input reference clock by 1 to 2^{16}-1 and generate an internal 16X clock.
- Independent receiver clock input
  Modem control functions (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#).
- Fully programmable serial interface characteristics.
  - 5-, 6-, 7-, or 8-bit characters
  - Even-, Odd-, or No-Parity bit
  1-, 1.5-, 2-Stop bit generation. (Like other general UARTs, IN16C554 checks only one stop bit, no matter how many they are)

- False start bit detection
- Generates or Detects Line Break
- Internal diagnostic capabilities : Loopback controls for communications link fault isolation.
- Full prioritized interrupt system controls

- Hardware (RTS#/CTS#) Flow Control

3. Ordering Information

Table 1: Ordering Information

Part Number	Package	Operating Temperature Range	Device Status
IN16C554A-TQ80	80-Pin TQFP	-20 ℃ to +85 ℃	Active
IN16C554A-PL68	68-Pin PLCC	-20 ℃ to +85 ℃	Active
IN16C554A-TQ64	64-Pin TQFP	-20 ℃ to +85 ℃	Active

4. Block Diagram

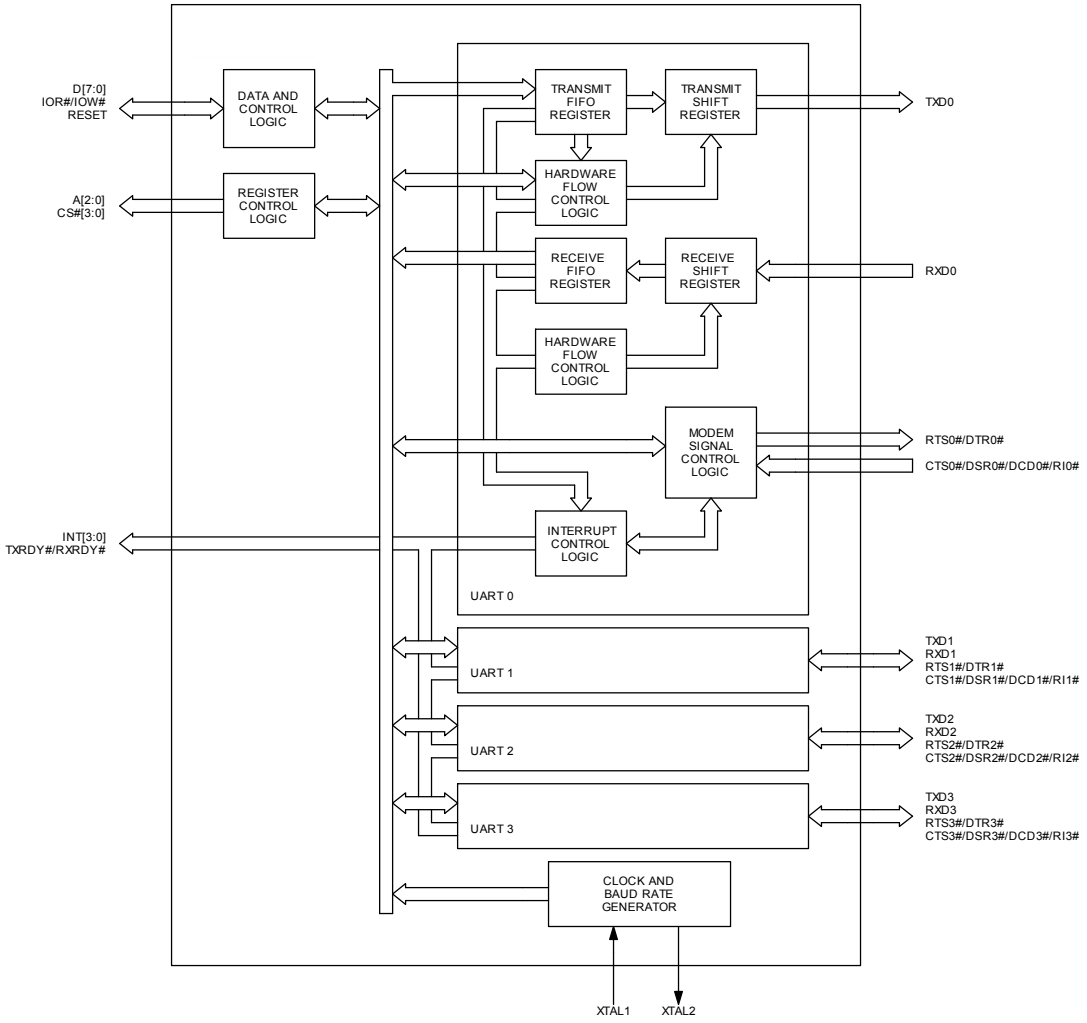
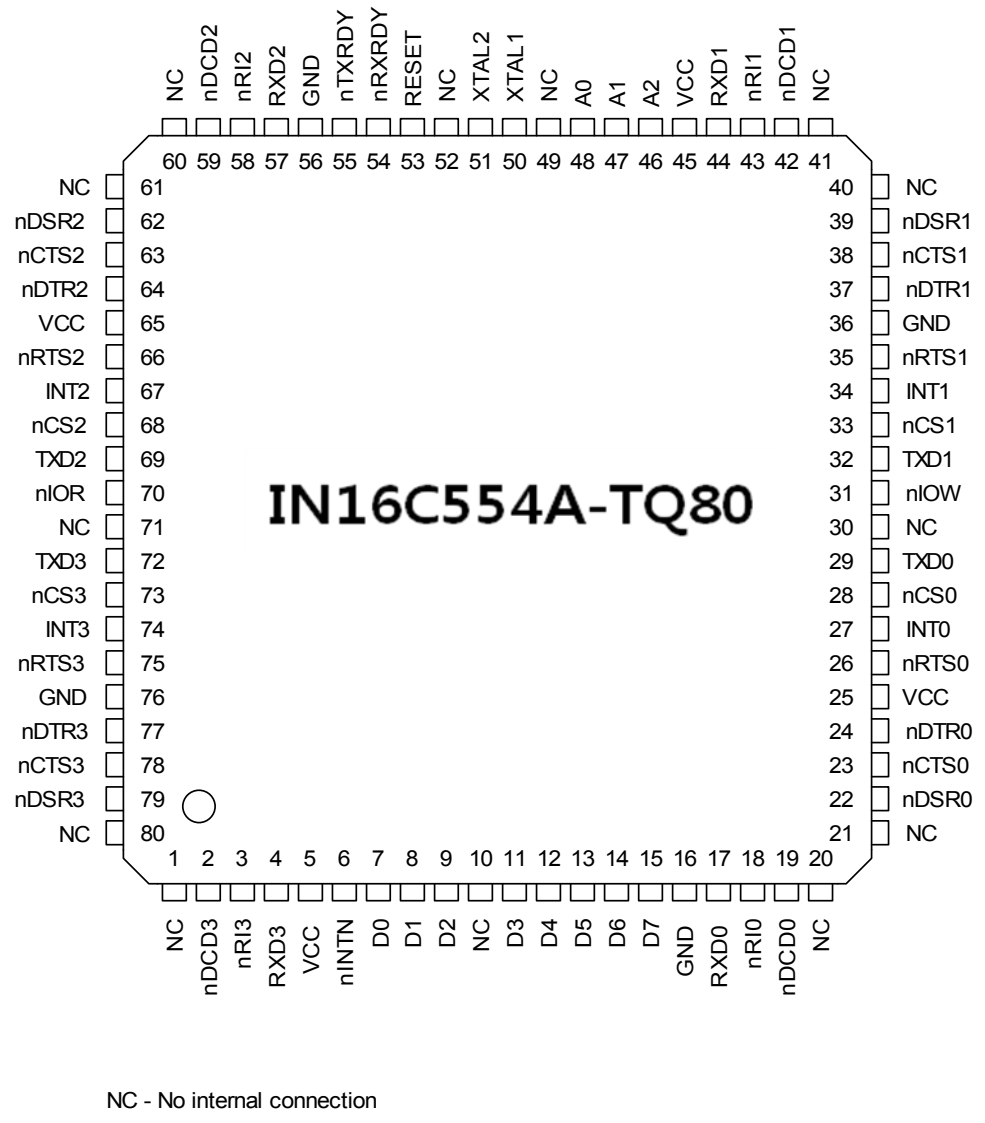


Figure 1: Block Diagram

5. Pin Configuration

5.1 Pin Configuration for 80-Pin TQFP Package



NC - No internal connection

Figure 2: 80-Pin TQFP Pin Configuration

5.2 Pin Configuration for 68-Pin PLCC Package

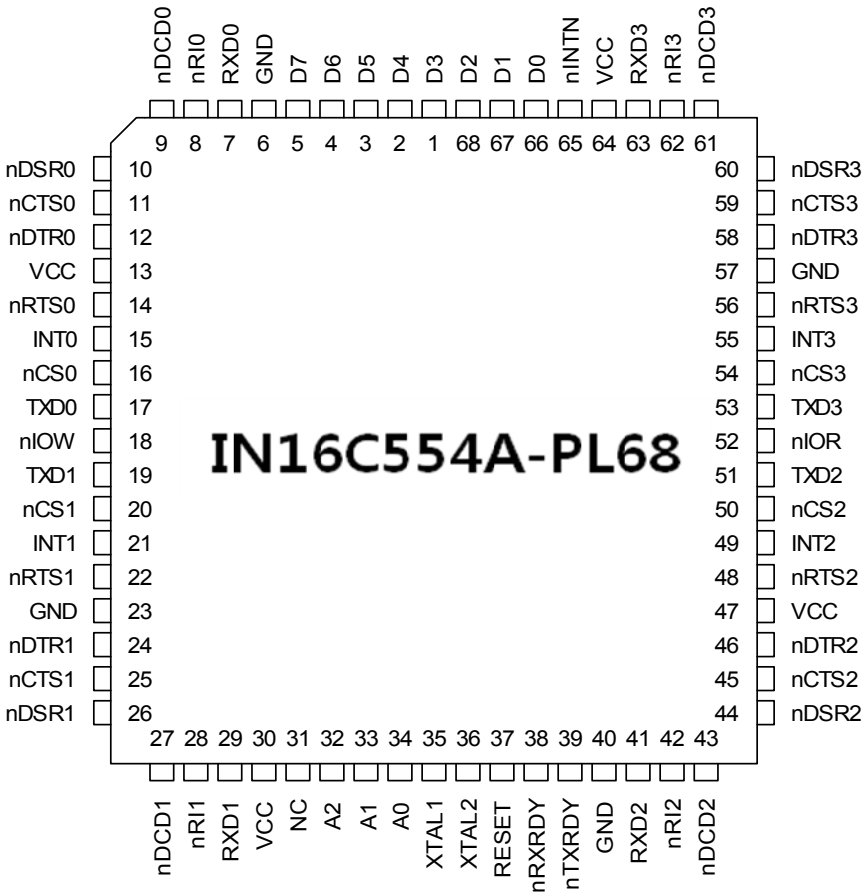


Figure 3: 68-Pin PLCC Pin Configuration

5.2 Pin Configuration for 64-pin-TQFP Package

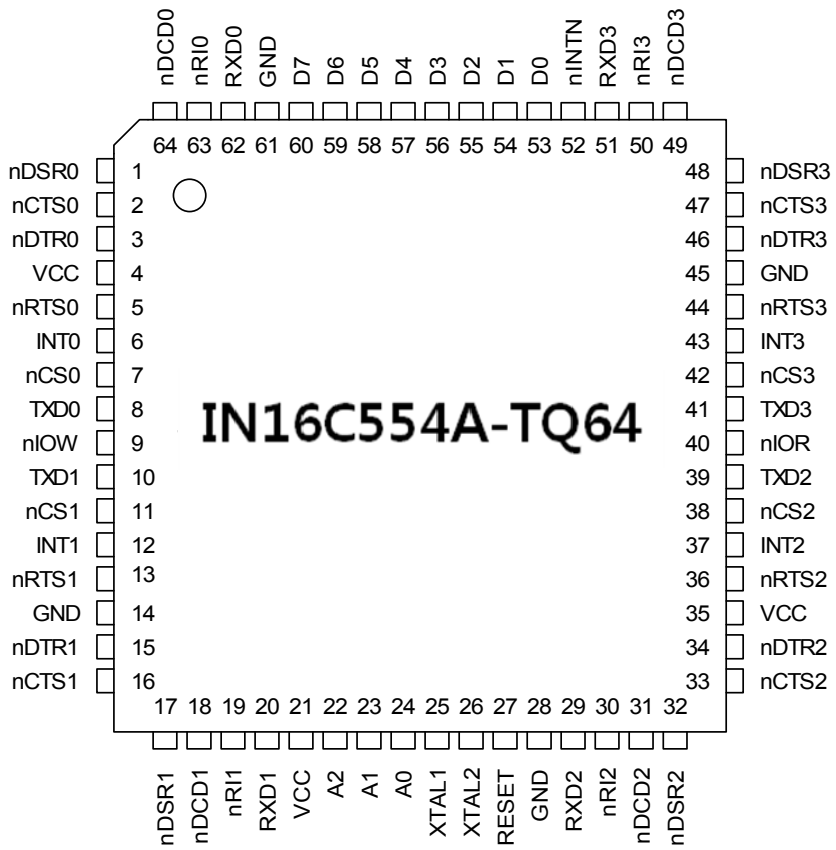


Figure 4: 64-Pin TQFP Pin Configuration

5.3 Pin Description

Table 2: Pin Description

Data Bus Interface					
Name	**Pin**			**Type**	**Description**
	TQFP80	**PLCC68**	**TQFP64**		
A0 A1 A2	48 47 46	34 33 32	24 23 22	I I I	Address Bus Lines [2:0]. These 3 address lines select one of the internal registers in UART channel 0-3 during a data bus transaction.
D0 D1 D2 D3 D4 D5 D6 D7	7 8 9 11 12 13 14 15	66 67 68 1 2 3 4 5	53 54 55 56 57 58 59 60	I/O I/O I/O I/O I/O I/O I/O I/O	Data Bus Lines [7:0]. These pins are tri-state data bus for data transfer to or from the controlling CPU.
IOR#	70	52	40	I	Read Data (active low strobe). A valid low level on IOR# will load the data of an internal register defined by address lines A [2:0] onto the UART data bus for access by an external CPU.
IOW#	31	18	9	I	Write Data (active low strobe). A valid low level on IOW# will transfer the data from external CPU to an internal register that is defined by address lines A [2:0].
CS0# CS1# CS2# CS3#	28 33 68 73	16 20 50 54	7 11 38 42	I I I I	Chip Select 0, 1, 2, and 3 (active low). These pins enable data transfers between the external CPU and the UART for the respective channel.
INT0/GINT INT1 INT2 INT3	27 34 67 74	15 21 49 55	6 12 37 43	O O O O	External interrupt output. When activated, INTx output informs CPU that UART has an interrupt to be serviced.
INTSEL	6	65	52	I	Interrupt Select. When INTSEL is left open or low state, the tri-state interrupts available on INT0-3 are enabled by MCR[3]. But, when INTSEL is in high state, INT0-3 are always enabled.
TXRDY#	55	39		O	Transmitter Ready (active low). This is asserted by TX FIFO/THR status for transmit channels 0-3.
RXRDY#	54	38		O	Receiver Ready (active low). This is asserted by RX FIFO/RHR status for receive channels 0-3.

Table 2: Pin Description…*continued*

Modem and Serial I/O Interface					
Name	**Pin**			**Type**	**Description**
	TQFP80	**PLCC68**	**TQFP64**		
TXD0	29	17	8	O	Transmit Data. These pins are individual transmit data output. During the local loop-back mode, the TXD output pin is disabled and TXD data is internally connected to the RXD input.
TXD1	32	19	10	O	
TXD2	69	51	39	O	
TXD3	72	53	41	O	
RXD0	17	7	62	I	Receive Data. These pins are individual receive data input. During the local loop-back mode, the RXD input pin is disabled and RXD data is internally connected to the TXD output.
RXD1	44	29	20	I	
RXD2	57	41	29	I	
RXD3	4	63	51	I	
RTS0#	26	14	5	O	Request to Send (active low). These pins indicate that the UART is ready to send data to the modem, and affect transmit and receive operations only when Auto-RTS function is enabled.
RTS1#	35	22	13	O	
RTS2#	66	48	36	O	
RTS3#	75	56	44	O	
CTS0#	23	11	2	I	Clear to Send (active low). These pins indicate the modem is ready to accept transmitted data from the UART, and affect transmit and receive operations only when Auto-CTS function is enabled.
CTS1#	38	25	16	I	
CTS2#	63	45	33	I	
CTS3#	78	59	47	I	
DTR0#	24	12	3	O	Data Terminal Ready (active low). These pins indicate UART is ready to transmit or receive data.
DTR1#	37	24	15	O	
DTR2#	64	46	34	O	
DTR3#	77	58	46	O	
DSR0#	22	10	1	I	Data Set Ready (active low). These pins indicate modem is powered-on and is ready for data exchange with UART.
DSR1#	39	26	17	I	
DSR2#	62	44	32	I	
DSR3#	79	60	48	I	
DCD0#	19	9	64	I	Carrier Detect (active low). These pins indicate that a carrier has been detected by modem.
DCD1#	42	27	18	I	
DCD2#	59	43	31	I	
DCD3#	2	61	49	I	
RI0#	18	8	63	I	Ring Indicator (active low). These pins indicate the modem has received a ringing signal from telephone line. A low to high transition on these input pins generates a modem status interrupt, if enabled.
RI1#	43	28	19	I	
RI2#	58	42	30	I	
RI3#	3	62	50	I	

Other Interfaces					
Name	**Pin**			**Type**	**Description**
	TQFP80	**PLCC68**	**TQFP64**		
XTAL1	50	35	25	I	Crystal or External Clock Input.
XTAL2	51	36	26	O	Crystal or Buffered Clock Output.

Table 2: Pin Description…*continued*

Other Interfaces					
Name	**Pin**			**Type**	**Description**
	TQFP80	**PLCC68**	**TQFP64**		
RESET	53	37	27	I	Reset (active high). This pin will reset the internal registers and all the outputs.
VCC	5 25 45 65	13 30 47 64	4 21 35	I	Power Supply Input. 3.3V (2.7V ~ 3.6V)
GND	16 36 56 76	6, 23 40 57	14 28 45 61	I	Signal and Power Ground.
NC	1 10 20 21 30 40 41 49 52 60 61 71 80	31		-	No Internal Connection.

6. Functional Description

The IN16C554A UART is pin-to-pin compatible with the TL16C554A and SB16C554 UARTs. The IN16C554A has same function with IN16C554 except for flow control and voltage that are used in operations.

IN16C554A can select hardware flow control. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS# output and CTS# input signals.

6.1 Hardware Flow Control

Hardware flow control is executed by Auto-RTS and Auto-CTS. Auto-RTS and Auto-CTS can be enabled/disabled by programming MCR [5]. If Auto-RTS is enabled, it reports that it cannot receive more data by asserting RTS# when RX FIFO has no space. Then after the data stored in RX FIFO is read by CPU, it reports that it can receive new data by deasseting RTS# when the amount of existing data in RX FIFO is less than trigger level. When Auto-CTS is enabled and CTS# is cleared to '0', transmitting data to TX FIFO has to be suspended because external device has reported that it cannot accept more data. When data transmission has been suspended and CTS# is set to '1', data in TX FIFO is retransmitted because external device has reported that it can accept more data. These operations prevent overrun during communication and if hardware flow control is disabled and transmit data rate exceeds RX FIFO service latency, overrun error occurs.

6.1.1 Auto-RTS

To enable Auto-RTS, MSR [5], [1] should be set to '1'. Once enabled, RTS# outputs '0'. If the number of received data in RX FIFO reaches a trigger level, RTS# will be changed to '1' and if not, holds '0'. This state indicates that RX FIFO can accept more data. After RTS# changed to '1' and reported to the CPU that it cannot accept more data, the CPU reads the data in RX FIFO and then the amount of data in RX FIFO reduces. When the amount of data in RX FIFO has a space to store data, RTS# changes to '0' and reports that it can accept more data. That is, if RTS# is '0' now, RTS# is not changed to '1' until the amount in RX FIFO reaches to trigger level. But if RTS# is '1' now, RTS# is not changed to '0' until the RX FIFO has at least one available byte space.

While Auto-RTS is enabled, you can verify if RTS# is '0' or '1' by FSR[5]. If FSR[5] is '0', RTS# is '0' and if '1', RTS# is '1', too. When IER[6] is set to '1' and RTS# is changed from '0' to '1' by Auto-RTS function, interrupt occurs and it is displayed on ISR[5:0]. Interrupts by Auto-RTS function are removed if MSR is read. RTS# is changed from '0' to '1' after the first STOP bit is received. Figure 5 shows the RTS# timing chart while Auto-RTS is enabled.

In Figure 5, Data Byte n-1 is received and RTS# is deasserted when the amount of data in RX FIFO is larger than the value written in FUR. UART completes transmitting new data (DATA BYTE n) which has started being transmitted even though external UART recognizes RTS# has been deasserted. After that, the device stops transmitting more data.

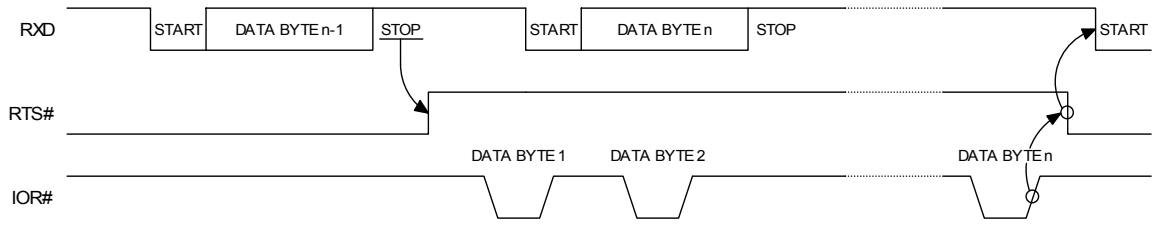


Figure 5: RTS# Functional Timing

6.1.2 Auto-CTS

Setting MSR [5] to '1' enables Auto-RTS. If enabled, data in TX FIFO are determined to be transmitted or suspended by the value of CTS#. If '0', it means external UART can receive new data and data in TX FIFO are transmitted through TXD pin. If '1', it means external UART can not accept more data and data in TX FIFO are not transmitted. But data being transmitted by then complete transmission. These procedures are performed irrespective of FIFO modes. While Auto-CTS is enabled, you can verify the input value of CTS# by FSR[1]. If '0', CTS# is '0' and it means external UART can accept new data, If '1', CTS# is '1' and it means external UART can not accept more data and data in TX FIFO are not being transmitted. If IER[7] is set to '1', interrupt is generated by Auto-CTS when the input of CTS# is changed from '0' to '1', and it is shown on ISR[5:0]. Interrupts generated by Auto-CTS are removed if MSR is read.

6.2 Programmable Baud Rate Generator

The IN16C554A has a programmable baud rate generator. The baud rate generator divides this clock frequency by a programmable divisor (DLL and DLM) between 1 and (2^{16} – 1) to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by transmitter for data bit shifting and receiver for data sampling.
The divisor of the baud rate generator is:

$$\text{Divisor} = \frac{\left(\text{XTAL1 Crystal Input Frequency}\right)}{(\text{Desired Baud Rate} \times 16)}$$

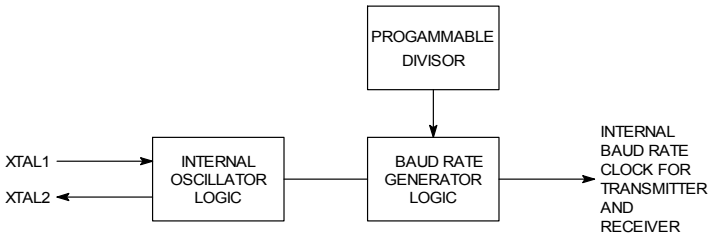


Figure 6: Baud Rate Generator Block Diagram

DLL and DLM must be written to in order to program the baud rate. DLL and DLM are the least and most significant byte of the baud rate divisor, respectively. If DLL and DLM are both zero, the IN16C554A is effectively disabled, as no baud clock will be generated.

Table 3 shows the baud rate and divisor value as well as crystal with frequency 1.8432MHz, 3.6864MHz, 7.3728MHz, and 14.7456MHz, respectively.

Figure 7 shows the crystal clock circuit reference.

Table 3: Baud Rates

Desired Baud Rate	16X Digit Divisor			
	1.8432MHz	3.6864MHz	7.3728MHz	14.7456MHz
50	0900h	1200h	2400h	4800h
75	0600h	0C00h	1800h	3000h
150	0300h	0600h	0C00h	1800h
300	0180h	0300h	0600h	0C00h
600	00C0h	0180h	0300h	0600h
1200	0060h	00C0h	0180h	0300h
1800	0040h	0080h	0100h	0200h
2000	003Ah	0074h	00E8h	01D0h
2400	0030h	0060h	00C0h	0180h
3600	0020h	0040h	0080h	0100h
4800	0018h	0030h	0060h	00C0h
7200	0010h	0020h	0040h	0080h
9600	000Ch	0018h	0030h	0060h
19.2K	0006h	000Ch	0018h	0030h
38.4K	0003h	0006h	000Ch	0018h
57.6K	0002h	0004h	0008h	0010h
115.2K	0001h	0002h	0004h	0008h
230.4K	–	0001h	0002h	0004h
460.8K	–	–	0001h	0002h
921.6K	–	–	–	0001h

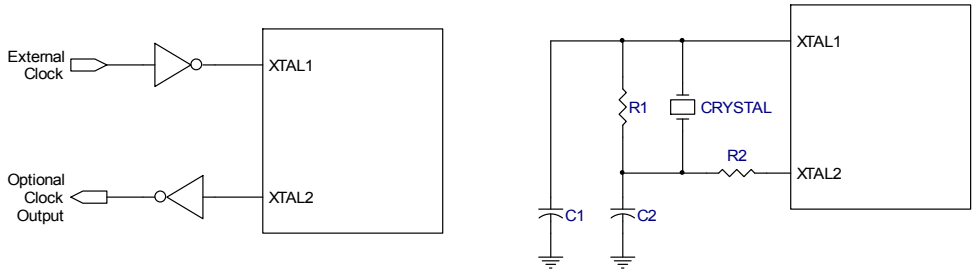


Figure 7: Baud Rate Generator Block Diagram

Table 4: Component Values

Frequency Range (MHz)	C1 (pF)	C2 (pF)	R1 (Ω)	R2(Ω)
1.8~8	22	68	220K	470 ~ 1.5K
8~16	33~68	33 ~ 68	220K ~ 2.2M	470 ~ 1.5K

6.3 Break and Time-out Conditions

Break Condition:

Break Condition is occurred when TXD signal outputs '0' and sustains for more than one character.

It is occurred if LCR[6] is set to '1' and deleted if '0'. If break condition is occurred when normal data are transmitted on TXD, break signal is transmitted and internal serial data are also transmitted, but they are not outputted to external TXD pin. When Break condition is deleted, then they are transmitted to TXD pin.

Figure 7 below shows the Break Condition Block Diagram.

Time-out Condition:

When serial data is received from external UART, characters are stored in RX FIFO. When the number of characters in RX FIFO reaches the trigger level, interrupt is generated for the CPU to treat characters in RX FIFO. But when the number of characters in RX FIFO does not reach the trigger level and no more data arrives from external device, interrupt is not generated and therefore CPU cannot recognize it. IN16C554A offers time-out function for this situation. Time-out function generates an interrupt and reports to CPU when the number of RX FIFO is less than trigger level and no more data receives for four character time.

Time-out interrupt is enabled when IER[2] is set to '1' and can be verified by ISR.

7. Register Descriptions

Address A[2:0]	LCR[7] = 0	LCR[7] = 1 LCR[7:0] ≠ BFh
0h	THR/RBR	DLL
1h	IER	DLM
2h	FCR/ISR	
3h	LCR	
4h	MCR	
5h	LSR	
6h	MSR	
7h	SPR	

Table 5: Internal Registers Map…*continued*

Address A[2:0]	Register	Read/Write	Comments
	Registers		
0h	THR : Transmit Holding Register RBR : Receive Buffer Register	Write-only Read-only	LCR[7] = 0
1h	IER : Interrupt Enable Register	Read/Write	LCR[7] = 0
2h	FCR : FIFO Control Register ISR : Interrupt Status Register	Write-only Read-only	LCR[7] = 0 LCR[7] = 1, LCR ≠ BFh
3h	LCR : Line Control Register	Read/Write	—
4h	MCR : Modem Control Register	Read/Write	LCR[7] = 0 LCR[7] = 1, LCR ≠ BFh, LCR[7] = 0
5h	LSR : Line Status Register	Read-only	LCR[7] = 0 LCR[7] = 1, LCR ≠ BFh
6h	MSR : Modem Status Register	Read-only	LCR[7] = 0 LCR[7] = 1, LCR ≠ BFh
7h	SPR : Scratch Pad Register	Read/Write	LCR[7] = 0 LCR[7] = 1, LCR ≠ BFh
0h	DLL : Divisor Latch LSB	Read/Write	LCR[7] = 1, LCR ≠ BFh
1h	DLM : Divisor Latch MSB	Read/Write	LCR[7] = 1, LCR ≠ BFh

Table 6: Internal Registers Description

Addr. A[2:0]	Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Page 0 Registers									
0h	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1h	IER	0	0	0	0	Modem Status Interrupt Enable	Receive Line Status Interrupt Enable	THR Empty Interrupt Enable	Receive Data Available Interrupt Enable
2h	ISR	FIFOs Enabled	FIFOs Enabled	0	0	Interrupt Priority Bit 3	Interrupt Priority Bit 2	Interrupt Priority Bit 1	Interrupt Priority Bit 0
2h	FCR	RX Trigger Level (MSB)	RX Trigger Level (LSB)	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
3h	LCR	Divisor Enable	Set TX Brake	Set Parity	Parity Type Select	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
4h	MCR	0	0	Autoflow Control enable	0/Loop Back	OUT/ INTx Enable	reserved	RTS#	DTR#
5h	LSR	RX FIFO Data Error	THR & TSR Empty	THR Empty	Receive Break	Framing Error	Parity Error	Overrun Error	Receive Data Ready
6h	MSR	DCD#	RI#	DSR#	CTS#	ΔDCD#	ΔRI#	ΔDSR#	ΔCTS#
7h	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1h	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

7.1 Interrupt Enable Register (IER)

IER enables each of the four types of Interrupt, namely receive data ready, transmit empty, line status, modem status. All interrupts are disabled if bit[7:0] are cleared. Interrupt is enabled by setting appropriate bits. Table 9 shows IER bit settings.

Table 7: Interrupt Enable Register Description

Bit	Symbol	Description
7:4	IER[7:4]	These four bits of the IER are cleared
3	IER[3]	Modem Status Interrupt Enable 0 : Disable the modem status register interrupt (default). 1: Enable the modem status register interrupt.
2	IER[2]	Receive Line Status Interrupt Enable 0 : Disable the receive line status interrupt (default). 1: Enable the receive line status interrupt.
1	IER[1]	Transmit Holding Register Interrupt Enable 0 : Disable the THR interrupt (default). 1 : Enable the THR interrupt.
0	IER[0]	Receive Buffer Register Interrupt Enable 0 : Disable the RBR interrupt (default). 1 : Enable the RBR interrupt.

7.2 Interrupt Status Register (ISR)

The UART provides multiple levels of prioritized interrupts to minimize software work load. ISR provides the source of interrupt in a prioritized manner.
Table 10 shows ISR[7:0] bit settings.

Table 8: Interrupt Status Register Description

Bit	Symbol	Description
7:6	ISR[7:6]	ISR[7:6] are set when FCR[0]=1 Mirror the content of FCR[0].

Table 8: Interrupt Status Register Description…*continued*

Bit	Interrupt Priority List and Reset Functions			
5:0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
00_0001	—	None	None	—
00_0110	1	Receiver Line Status	OE, PE, FE, BI	Reading the LSR.
00_0100	2	Receive Data Available	Receiver data available, reaches trigger level.	Reading the RBR or FIFO falls below trigger level.
00_1100	2	Character Timeout Indication	At least one data is in RX FIFO and there are no more data in FIFO during four character time.	Reading the RBR.
00_0010	3	Transmit Holding Register Empty	When THR is empty or TX FIFO passes above trigger level (FIFO enable).	Reading the ISR or write data on THR.
00_0000	4	Modem Status	CTS#, DSR#, DCD#, RI#	Reading the MSR.

7.3 FIFO Control Register (FCR)

FCR is used for enabling the FIFOs, clearing the FIFOs, setting transmit/receive FIFO trigger level, and selecting the DMA modes. Table 11 shows FCR bit settings.

Table 9: FIFO Control Register Description

Bit	Symbol	Description
7:6	FCR[7:6]	RX FIFO Trigger Level Select 00 : 1 characters (default) 01 : 4 characters 10 : 8 characters 11 : 14 characters
5:4	FCR[5:4]	FCR[5:4] are reserved
3	FCR[3]	DMA Mode Select 0 : Set DMA mode 0 (default) 1 : Set DMA mode 1
2	FCR[2]	TX FIFO Reset 0 : No TX FIFO reset (default) 1 : Reset TX FIFO pointers and TX FIFO level counter logic. This bit will return to '0' after resetting FIFO.
1	FCR[1]	RX FIFO Reset 0 : No RX FIFO reset (default) 1 : Reset RX FIFO pointers and RX FIFO level counter logic. This bit will return to '0' after resetting FIFO.
0	FCR[0]	FIFO enable 0 : Disable the TX and RX FIFO (default). 1 : Enable the TX and RX FIFO

7.4 Line Control Register (LCR)

LCR controls the asynchronous data communication format. The word length, the number of stop bits, and the parity type are selected by writing the appropriate bits to the LCR. Table 12 shows LCR bit settings.

Table 10: Line Control Register Description

Bit	Symbol	Description
7	LCR[7]	Divisor Latch Enable. 0 : Disable the divisor latch (default). 1 : Enable the divisor latch.
6	LCR[6]	Break Enable. 0 : No TX break condition output (default). 1 : Forces TXD output to '0', for alerting the communication terminal to a line break condition.
5	LCR[5]	Set Stick Parity.

		LCR[5:3] = xx0 : No parity is selected. LCR[5:3] = 0x1 : Stick parity disabled. (default) LCR[5:3] = 101 : Stick parity is forced to '1'. LCR[5:3] = 111 : Stick parity is forced to '0'.
4	LCR[4]	Parity Type Select. LCR[5:3] =001 : Odd parity is selected. LCR[5:3] =011 : Even parity is selected.
3	LCR[3]	Parity Enabled. 0 : No parity (default). 1 : A parity bit is generated during the transmission and the receiver checks for receive parity.
2	LCR[2]	Number of Stop Bits. LCR[2:0] = 0xx : 1 stop bit (word length = 5, 6, 7, 8). LCR[2:0] = 100 : 1.5 stop bits (word length = 5). LCR[2:0] = 11x or 1x1 : 2 stop bits (word length = 6, 7. 8).
1:0	LCR[1:0]	Word Length Bits. 00 : 5 bits (default). 01 : 6 bits. 10 : 7 bits. 11 : 8 bits.

7.5 Modem Control Register (MCR)

MCR controls the interface with the modem, data set, or peripheral device that is emulating the modem. Table 13 shows MCR bit settings.

Table 11: Modem Control Register Description

Bit	Symbol	Description
7:6	MCR [7:6]	These two bits are always cleared
5	MCR[5]	Autoflow control enable. 0 : Auto-RTS and auto-CTS disabled 1 : If MCR[1]=1, Auto-RTS and auto-CTS enabled (autoflow control enabled) If MCR[1]=1, Auto-CTS only enabled.
4	MCR[4]	Internal Loop Back Enable. 0 : Disable loop back mode (default). 1 : Enable internal loop back mode. In this mode the MCR[3:0] signals are looped back into MSR[7:4] and TXD output is looped back to RXD input internally.
3	MCR[3]	OUT/Interrupt Output Enable. 0 : INTx outputs disabled (default). During loop back mode, OUT2 output '0' and it controls MSR[7] to '1'. 1 : INTx outputs enabled. During loop back mode, OUT2 output

		'1' and it controls MSR[7] to '0'. OUT is not available as an output pin on the IN16C554A.
2	MCR[2]	It has no effect on operation.
1	MCR[1]	RTS# Output. 0 : Force RTS# output to '1'. During loop back mode, controls MSR[4] to '1'. 1 : Force RTS# output to '0'. During loop back mode, controls MSR[4] to '0'.
0	MCR[0]	DTR# Output. 0 : Force DTR# output to '1'. During loop back mode, controls MSR[5] to '1'. 1 : Force DTR# output to '0'. During loop back mode, controls MSR[5] to '0'.

7.6 Line Status Register (LSR)

LSR provides the status of data transfers between the UART and the CPU. When LSR is read, LSR[4:2] reflect the error bits (BI, FE, PE) of the character at the top of the RX FIFO. The errors in a character are identified by reading LSR and then reading RBR. Reading LSR does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the RBR. Table 14 shows LSR bit settings.

Table 12: Line Status Register Description

Bit	Symbol	Description
7	LSR[7]	RX FIFO data error Indicator. 0 : No RX FIFO error (default). 1 : At least one parity error, framing error, or break indication is in the RX FIFO. This bit is cleared when there is no more error in any of characters in the RX FIFO.
6	LSR[6]	THR and TSR Empty Indicator. 0 : THR or TSR is not empty. 1 : THR and TSR are empty.
5	LSR[5]	THR Empty Indicator. 0 : THR is not empty. 1 : THR is empty. It indicates that the UART is ready to accept a new character for transmission. In addition, it uses the UART to generate an interrupt to the CPU when the THR empty interrupt enable is set to '1'.
4	LSR[4]	Break Interrupt Indicator. 0 : No break condition (default). 1 : The receiver received a break signal (RXD was '0' for at least one character frame time). In FIFO mode, only one character is loaded

		into the RX FIFO.
3	LSR[3]	Framing Error Indicator. 0 : No framing error (default). 1 : Framing error. It indicates that the received character did not have a valid stop bit.
2	LSR[2]	Parity Error Indicator. 0 : No parity error (default). 1 : Parity error. It indicates that the receive character did not have the correct even or odd parity, as selected by the LCR[4]
1	LSR[1]	Overrun Error Indicator. 0 : No overrun error (default). 1 : Overrun error. It indicates that the character in the RBR or RX FIFO was not read by the CPU, thereby ignored the receiving character.
0	LSR[0]	Receive Data Ready Indicator. 0 : No character in the RBR or RX FIFO. 1 : At least one character in the RBR or RX FIFO.

7.7 Modem Status Register (MSR)

MSR provides the current status of control signals from modem or auxiliary devices. MSR[3:0] are set to '1' when input from modem changes and cleared to '0' as soon as CPU reads MSR. Table 15 shows MSR bit settings.

Table 13: Modem Status Register Description

Bit	Symbol	Description
7	MSR[7]	DCD Input Status. Complement of Data Carrier Detect (DCD#) input. In loop back mode this bit is equivalent to OUT2 in the MCR.
6	MSR[6]	RI Input Status. Complement of Ring Indicator (RI#) input. In loop back mode this bit is equivalent to OUT1 in the MCR.
5	MSR[5]	DSR Input Status. Complement of Data Set Ready (DSR#) input. In loop back mode this bit is equivalent to DTR in the MCR.
4	MSR[4]	CTS Input Status. Complement of Clear To Send (CTS#) input. In loop back mode this bit is equivalent to RTS in the MCR.
3	MSR[3]	ΔDCD Input Status. 0 : No change on CD# input (default). 1 : Indicates that the DCD# input has changed state.

2	MSR[2]	ΔRI Input Status. 0 : No change on RI# input (default). 1 : Indicates that the RI# input has changed state from '0' to '1'.
1	MSR[1]	ΔDSR Input Status. 0 : No change on DSR# input (deault). 1 : Indicates that the DSR# input has changed state.
0	MSR[0]	ΔCTS Input Status. 0 : No change on CTS# input (deault). 1 : Indicates that the CTS# input has changed state.

7.8 Scratch Pad Register (SPR)

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratch pad register to be used by the programmer to hold data temporarily.

7.9 Divisor Latches (DLL, DLH)

Two 8-bit registers which store the 16-bit divisor for generation of the clock in baud rate generator. DLH stores the most significant part of the divisor, and DLL stores the least significant part of the divisor. Divisor of zero is not recommended.

Note that DLL and DLH can only be written to before sleep mode is enabled, i.e., before IER[4] is set. Chapter 6.2 describes the details of divisor latches.

Table 14: IN16C554A Reset Conditions

Registers	Reset State
RBR	[7:0] = 'XXXX_XXXX'
IER	[7:0] = '0000_0000'
FCR	[7:0] = '0000_0000'
ISR	[7:0] = '0000_0001'
LCR	[7:0] = '0000_0000'
MCR	[7:0] = '0000_0000'
LSR	[7:0] = '0110_0000'
MSR	[7:4] = '0000' [3:0] = Logic levels of the inputs inverted
SPR	[7:0] = '0000_0000'
DLL	[7:0] = '1111_1111'
DLM	[7:0] = '1111_1111'
Output Signals	**Reset State**
TXD, RTS#, DTR#	Logic 1
TXRDY#	Logic 0
RXRDY#	Logic 1
INT	Tri-State Condition = INTSEL is open or low state Logic 0 = INTSEL is high state

8. Programmer's Guide

The base set of registers that is used during high-speed data transfer has a straightforward access method. The extended function registers require special access bits to be decoded along with the address lines. The following guide will help with programming these registers. Note that the descriptions below are for individual register access. Some streamlining through interleaving can be obtained when programming all the registers.

Table 15: Register Programming Guide

Command	Action
Set Baud Rate to VALUE1, VALUE2	Read LCR, save in temp Set LCR to 80h Set DLL to VALUE1 Set DLM to VALUE2 Set LCR to temp
Read Flow Control Status	Read LCR, save in temp1 Read MCR, save in temp2 Set LCR to ('0111_1111' **AND** temp1) Set MCR to ('0100_0000' **OR** temp2) Read FSR, save in temp3 Pass temp3 back to host Set MCR to temp2 Set LCR to temp1
Read TX FIFO / RX FIFO Count Value	Read LCR, save in temp1 Read MCR, save in temp2 Set LCR to ('0111_1111' **AND** temp1) Set MCR to ('0100_0000' **OR** temp2) Read TCR, save in temp3 Read RCR, save in temp4 Pass temp3 back to host Pass temp4 back to host Set MCR to temp2 Set LCR to temp1

9. Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		–	3.6	V
V_I	Input voltage		−0.5	5.5	V
V_O	Output voltage		GND + 0.1	V_{CC} – 0.1	V
T_{amb}	Operating ambient temperature	In free-air	−20	+85	℃
T_{stg}	Storage temperature		−60	+150	℃

DC Electrical Characteristics

Symbol	Parameter	Conditions	3.3V			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_{IH}	High-level input voltage		V_{CC} x 0.7	–	5.5	V
V_{IL}	Low-level input voltage		0	–	V_{CC} x 0.3	V
V_O	Output voltage		0	–	V_{CC}	V
V_{OH}	High-level output voltage	IOH = −8mA	2.4	–	–	V
V_{OL}	Low-level output voltage	IOL = 8mA	–	–	0.4	V
C_I	Input capacitance		–	–	9	pF
	Oscillator/Clock speed		–	–	85	MHz
	Clock duty cycle		–	50	–	%
I_{CC}	Supply current	f=14.7456MHz	–	–	37.8	mA
$I_{CCsleep}$	Sleep current	f=14.7456MHz	–	–	2.5	mA

Symbol	Parameter	Min	Max	Unit
t_{rd}	Pulse duration, IOR# low	24		ns
t_{csr}	Set up time, CSx# valid before IOR# low †	10		ns
t_{ar}	Set up time, A2~A0 valid before IOR# low †	10		ns
t_{ra}	Hold time, A2~A0 valid after IOR# high †	2		ns
t_{rcs}	Hold time, CSx# valid after IOR# high †	0		ns
t_{frc}	Delay time, $t_{ar}+t_{rd}+t_{rc}$ ‡	54		ns
t_{rc}	Delay time, IOR# high to IOR# or IOW# low	20		ns
t_{wr}	Pulse duration, IOW#↓	24		ns
t_{csw}	Setup time, CSx# valid before IOW#↓	10		ns
t_{aw}	Setup time, A2~A0 valid before IOW#↓	10		ns
t_{ds}	Setup time, D7~D0 valid before IOW#↑	15		ns
t_{wa}	Hold time, A2~A0 valid after IOW#↑	2		ns
t_{wcs}	Hold time, CSx# valid after IOW#↑	2		ns
t_{dh}	Hold time, D7~D0 valid after IOW#↑	5		ns
t_{fwc}	Delay time, $t_{aw}+t_{wr}+t_{wc}$	54		ns
t_{wc}	Delay time, IOW#↑ to IOW# or IOR#↓	20		ns
t_{rvd}	Enable time, IOR#↓ to D7~D0 valid		24	ns
t_{hz}	Disable time, IOR# to D7~D0 released	4		ns
t_{irs}	Delay time, INTx↓ to TXDx↓ at start	8	24	RCLK
t_{sti}	Delay time, TXDx↓ at start to INTx↑	8	8	RCLK
t_{si}	Delay time, IOW# high or low (WR THR) to INTx↑	16	32	RCLK
t_{sxa}	Delay time, TXDx↓ at start to TXRDY#↓		8	RCLK
t_{hr}	Propagation delay time, IOW#(WR THR)↓ to INTx↓		12	ns
t_{ir}	Propagation delay time, IOR#(RD IIR)↑ to INTx↓		12	ns
t_{wxi}	Propagation delay time, IOW#(WR THR) ↓ to TXRDY#↑		10	ns
t_{sint}	Delay time, stop bit to INTx↑ or stop bit to RXRDY# or read RBR to set interrupt	1		RCLK
t_{rint}	Propagation delay time, Read RBR/LSR to INTx↓/LSR interrupt↓		12	ns
t_{rint}	Propagation delay time, IOR# RCLK↓ to RXRDY#↑		12	ns
t_{mdo}	Propagation delay time, IOW#(WR MCR)↑ to RTSx#, DTRx#↑		12	ns
t_{sim}	Propagation delay time, modem input CTSx#, DSRx#, and DCDx#↓↑ to INTx↑		12	ns
t_{rim}	Propagation delay time, IOR#(RD MSR)↑ to interrupt↓		3	ns
t_{sim}	Propagation delay time, Rix#↑ to INTx#↓		12	ns

† The internal address strobe is always in active state.

‡ In the FIFO mode, td1= xxns (min) between reads of the FIFO and the status register.

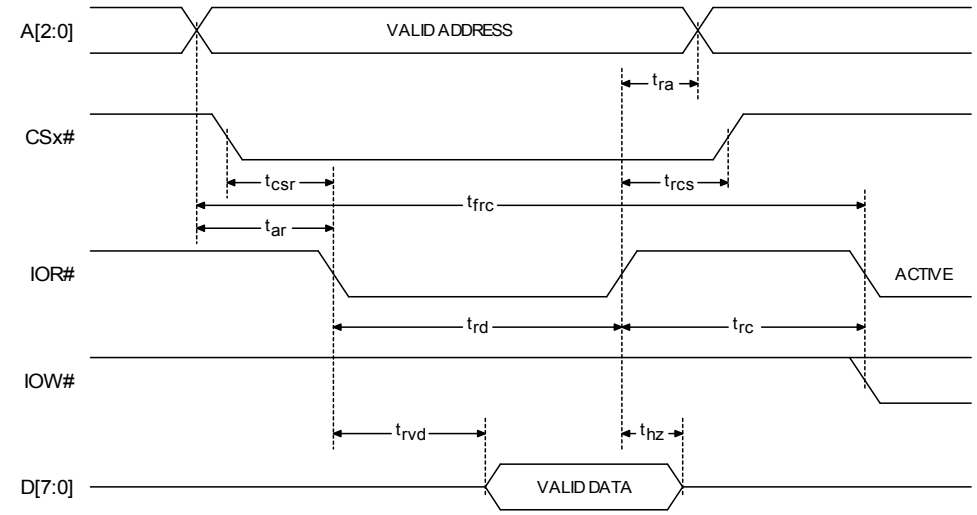


Figure 8: Read Cycle Timing

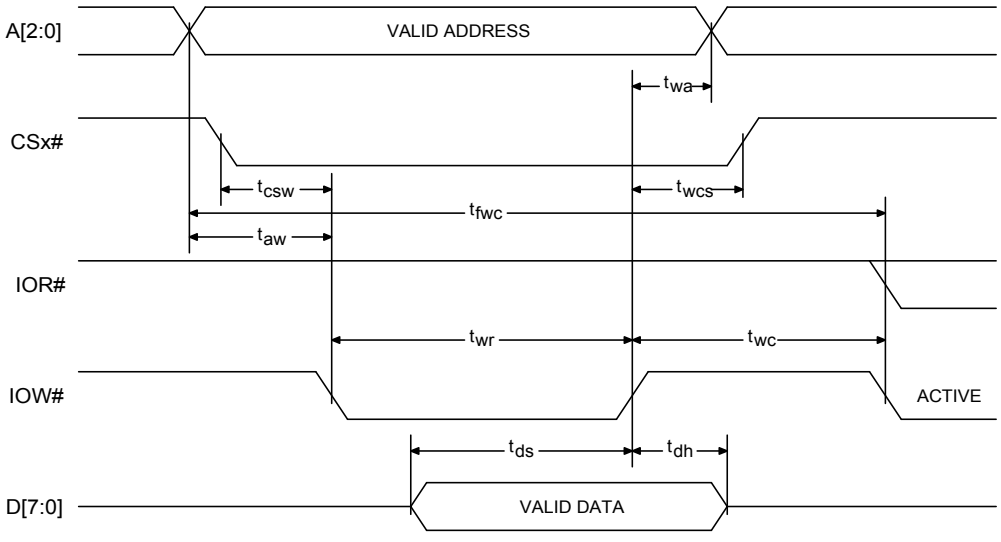


Figure 9: Write Cycle Timing

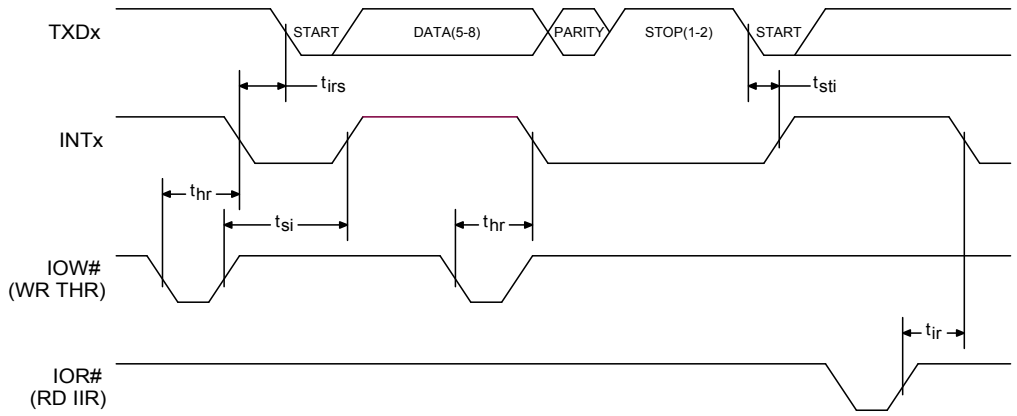


Figure 10: Transmitter Timing

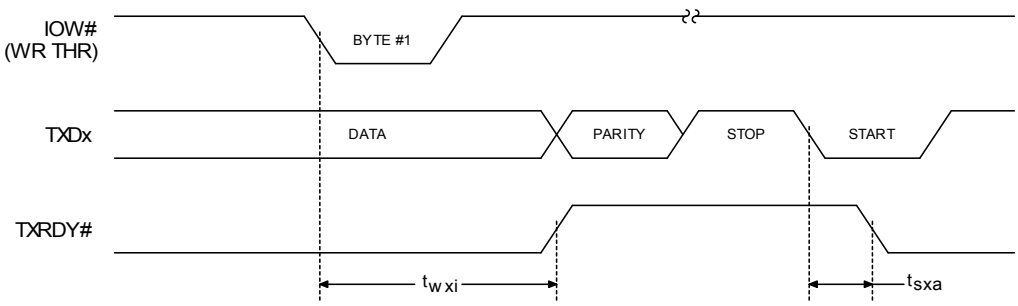


Figure 11: Transmitter Ready Mode 0 Timing

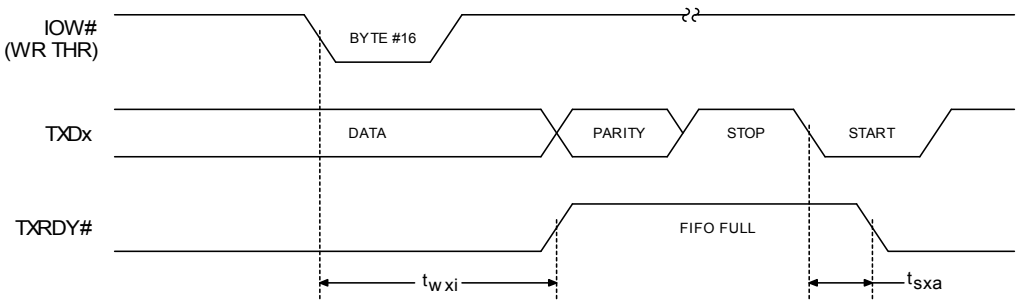


Figure 12: Transmitter Ready Mode 1 Timing

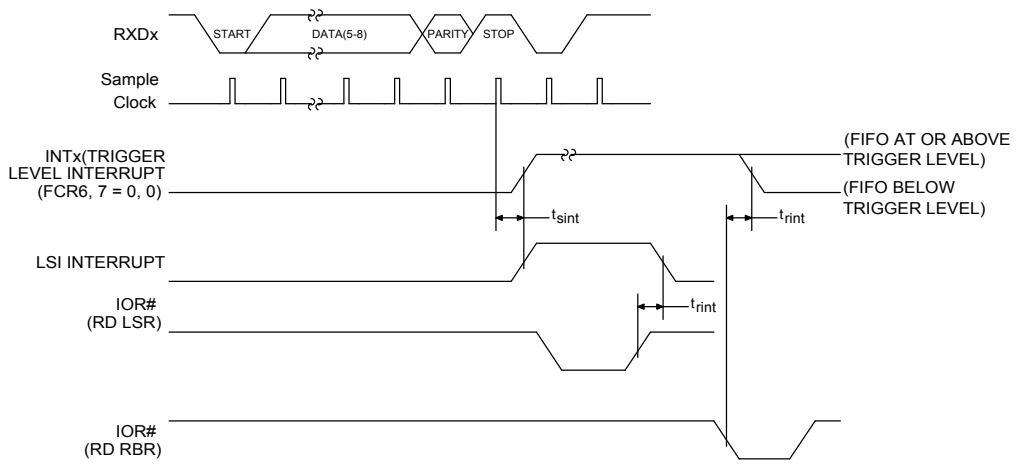


Figure 13: Receiver FIFO First Byte (Sets RBR) Timing

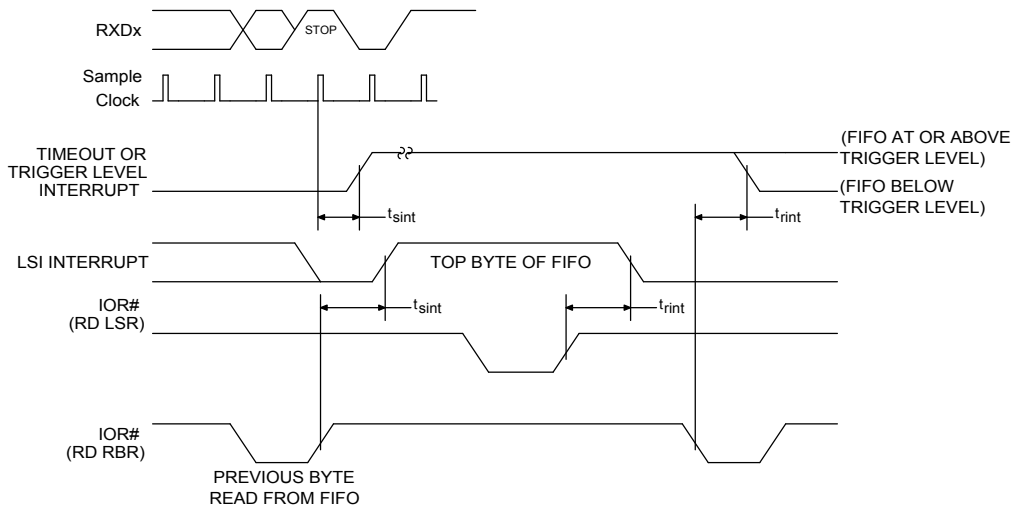


Figure 14: Receiver FIFO After First Byte (After RBR Set) Timing

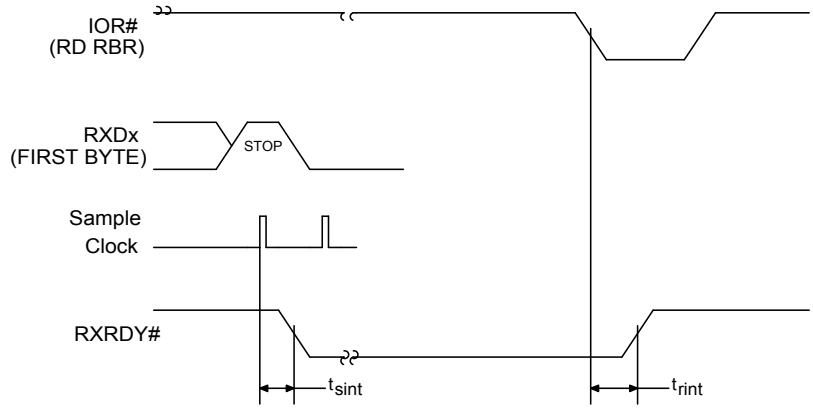


Figure 15: Receiver Ready Mode 0 Timing

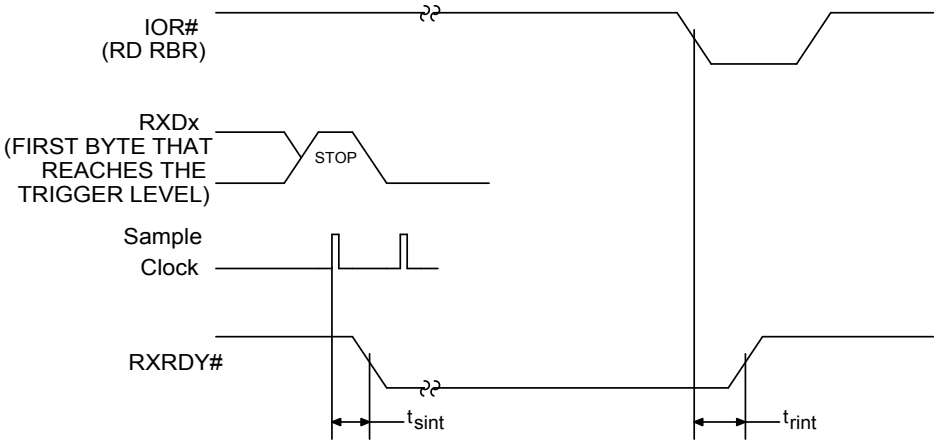


Figure 16: Receiver Ready Mode 1 Timing

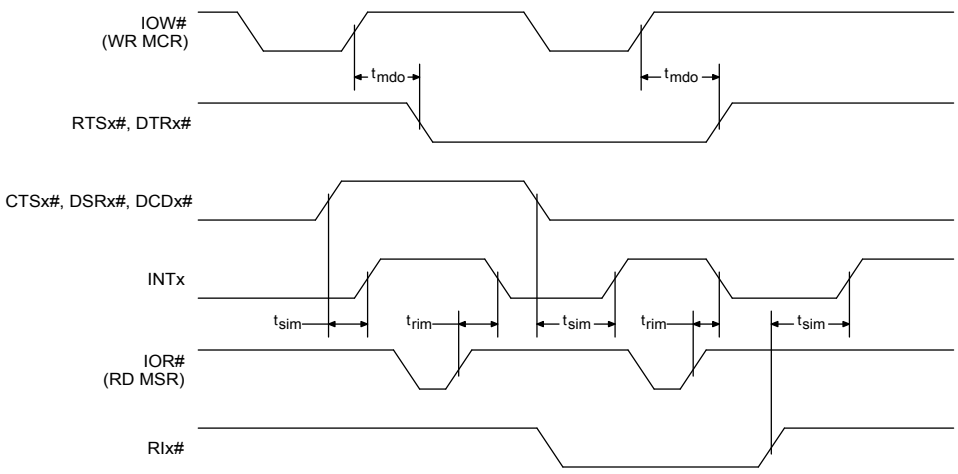
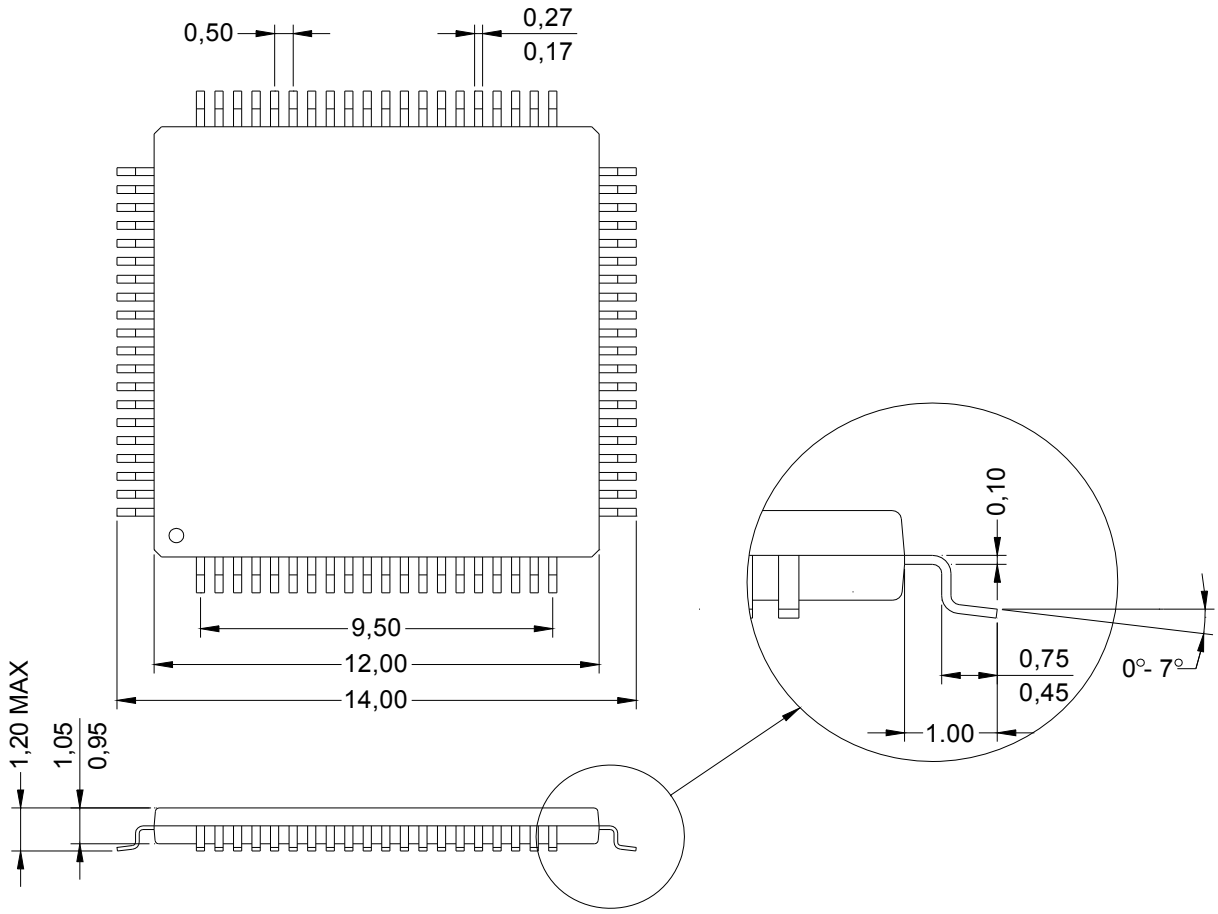


Figure 17: Modem Control Timing

10. Package Outline

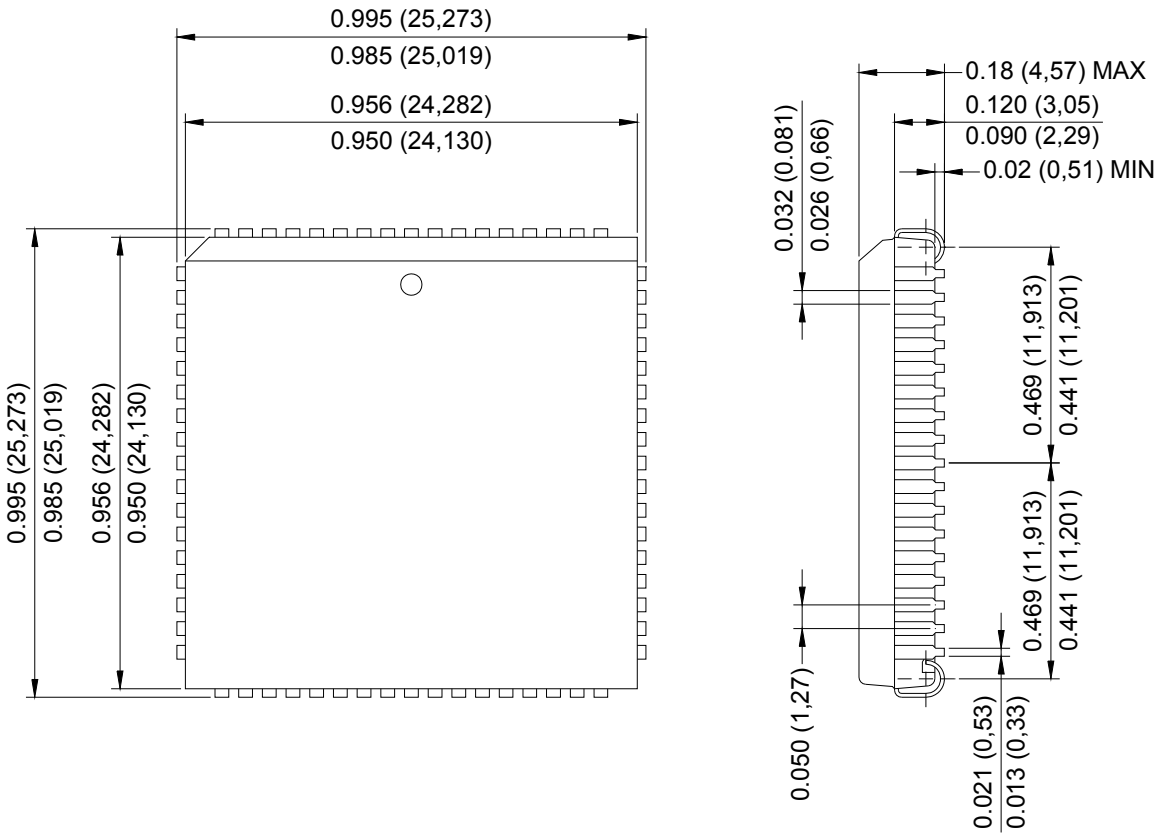
80-Pin TQFP: Thin Plastic Quad Flat Package; Body 12 x 12 x 1.0 mm



Note :

1. All dimensions are in millimeters.
2. Falls within ANSI Y14.5-1982

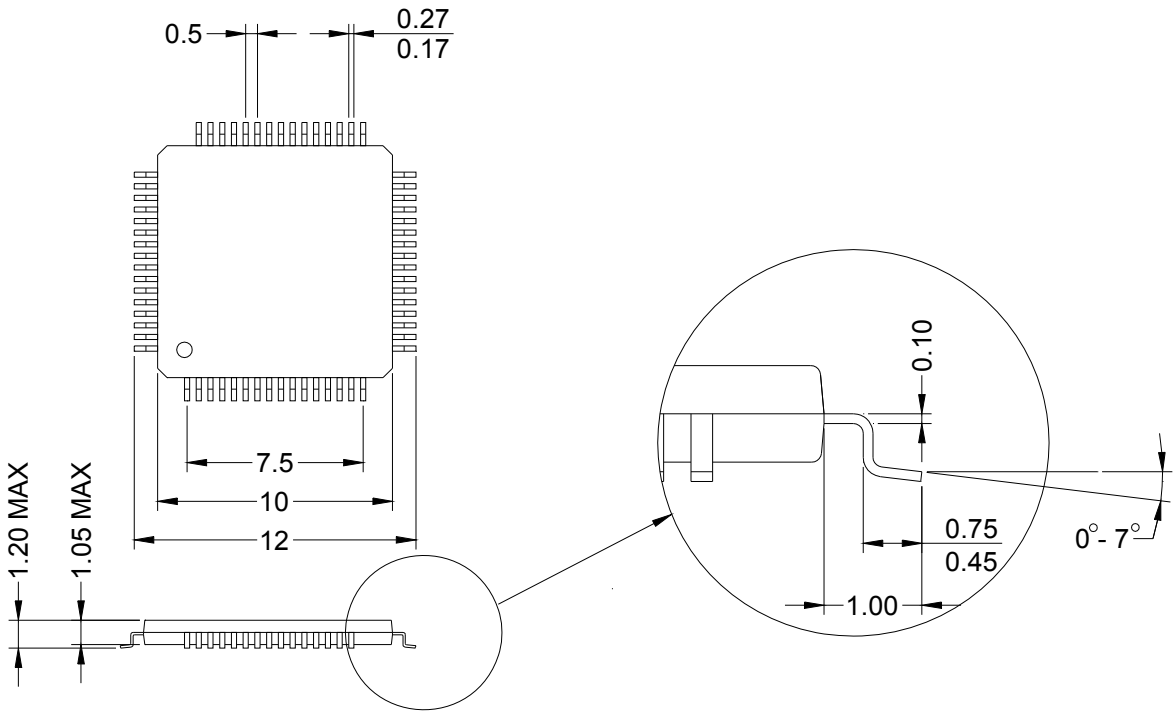
68-Pin PLCC: Plastic Leaded Chip Carrier



Note :

1. All dimensions are in inches (millimeters).
2. Falls within ANSI Y14.5-1982

64-Pin TQFP: Thin Plastic Quad Flat Package; Body 10 x 10 x 1.0 mm



Note :

1. All dimensions are in inches (millimeters).
2. Falls within ANSI Y14.5-1982