

**IN74LV138**

**3-to-8 line decoder/demultiplexer;  
inverting**

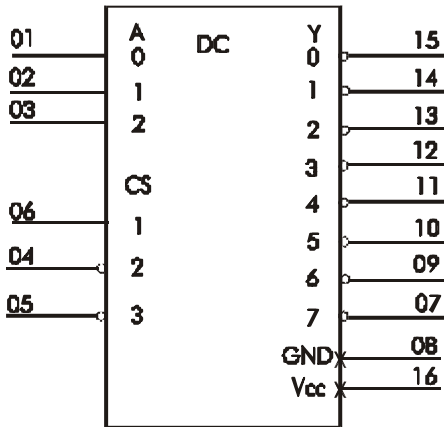
The IN74LV138 is a low-voltage Si-gate CMOS device and is pin and function compatible 74HCT138.

The IN74LV138 accepts three binary weighted address inputs - ( $A_0, A_1, A_2$ ) and when enabled, provide 8 - mutually exclusive active LOW outputs ( $Y_0$  to  $Y_7$ ).

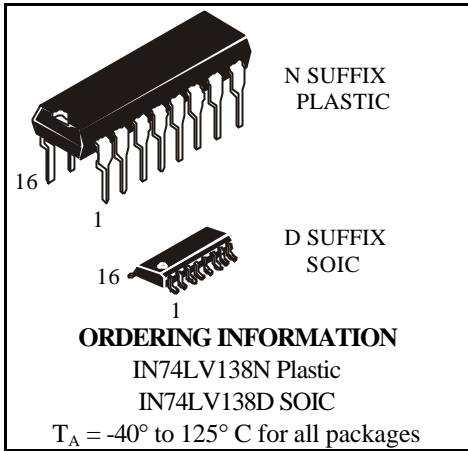
The "138" features three enable inputs: two active LOW ( $\overline{CS_2}, \overline{CS_3}$ ) and one active HIGH ( $CS_1$ ). Every output will be HIGH unless  $\overline{CS_2}$ ,  $\overline{CS_3}$  are LOW and  $CS_1$  is HIGH.

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard

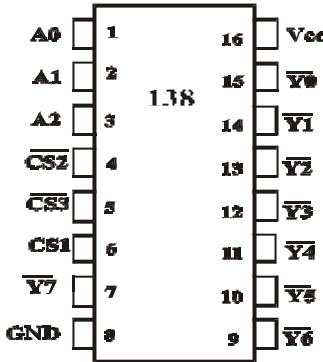
**LOGIC DIAGRAM**



PIN 16 = V<sub>CC</sub>  
PIN 8 = GND



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Outputs										
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	H	H	H	H	L	H	H	H	H
H	L	L	H	H	L	H	H	H	H	L	H	H	H
H	L	L	H	H	H	H	H	H	H	H	L	H	H

H = high level (steady state)  
L = low level (steady state)  
X = don't care

**MAXIMUM RATINGS** \*

Symbol	Parameter	Value	Conditions	Unit
V <sub>CC</sub>	DC supply voltage	-0.5 to +7.0		V
I <sub>IK</sub>	DC input diode current	±20	V <sub>I</sub> < - 0.5 or V <sub>I</sub> > V <sub>CC</sub> +0.5V	mA
I <sub>OK</sub>	DC output diode current	±50	V <sub>O</sub> < - 0.5 or V <sub>O</sub> > V <sub>CC</sub> +0.5V	mA
I <sub>O</sub>	DC output source or sink current	±25	-0.5V < V <sub>O</sub> < V <sub>CC</sub> +0.5V	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND current for types with standard outputs	±50		mA
T <sub>stg</sub>	Storage Temperature	-65 to +150		°C
P <sub>D</sub>	Power Dissipation per package Plastic DIP+ SOIC Package+	750 500		mW
T <sub>L</sub>	Lead temperature, 1.5 mm from Case for 4 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260		°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 +Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C  
 SOIC Package: - 8 mW/°C from 70° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC supply voltage	1.0	5.5	V
V <sub>IN</sub>	DC input voltage,	0	V <sub>CC</sub>	V
V <sub>O</sub>	DC output voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating ambient temperature range in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times except for Schmitt-trigger inputs	V <sub>CC</sub> = 1.0 ? 2.0V V <sub>CC</sub> = 2.0 ? 2.7V V <sub>CC</sub> = 2.7 ? 3.6V V <sub>CC</sub> = 3.6 ? 5.5V	0 500 200 100 50	ns/B

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> , Â	Guaranteed Limit						Unit
				25°C		î ð -40°C to 85°C		î ð -40°C to 125°C		
				min	max	min	max	min	max	
V <sub>IH</sub>	High-level input voltage		1.2	0.9	-	0.9	-	0.9	-	Â
			2.0	1.4	-	1.4	-	1.4	-	
			2.7 to 3.6	2.0	-	2.0	-	2.0	-	
			4.5 to 5.5	0.7 V <sub>CC</sub>	-	0.7 V <sub>CC</sub>	-	0.7 V <sub>CC</sub>	-	
V <sub>IL</sub>	Low-level input voltage		1.2	-	0.3	-	0.3	-	0.3	Â
			2.0	-	0.6	-	0.6	-	0.6	
			2.7 to 3.6	-	0.8	-	0.8	-	0.8	
			4.5 to 5.5	-	0.3 V <sub>CC</sub>	-	0.3 V <sub>CC</sub>	-	0.3 V <sub>CC</sub>	
V <sub>OH</sub>	High-level output voltage	-I <sub>O</sub> =100µA V <sub>IH</sub> or V <sub>IL</sub>	1.2	-	-	-	-	-	-	Â
			2.0	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.3	-	4.3	-	
V <sub>IH</sub> or V <sub>IL</sub> -I <sub>O</sub> =6.0 mA -I <sub>O</sub> =12.0 mA	3.0	2.48	-	2.40	-	2.20	-	B		
	4.5	3.70	-	3.60	-	3.50	-			
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =100µA	1.2	-	0.15	-	0.2	-	0.2	B
			2.0	-	0.15	-	0.2	-	0.2	
			3.0	-	0.15	-	0.2	-	0.2	
			-	-	-	-	-	-	-	
V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =6.0 mA I <sub>O</sub> =12.0 mA	3.0	-	0.33	-	0.40	-	0.50	B		
	4.5	-	0.40	-	0.55	-	0.65			
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> or GND	5.5	-	±0.1	-	±1.0	-	±1.0	î êÀ
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> or GND I <sub>O</sub> =0	5.5	-	8.0	-	80	-	160	î êÀ

AC ELECTRICAL CHARACTERISTICS ( $C_L=50$  pF,  $t_{LH} = t_{HL} = 2.5$  ns,  $V_{IL}=0$ B,  $V_{IH}=V_{CC}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit						Unit
			25°C		î ò -40°C to 85°C		î ò -40°C to 125°C		
			min	max	min	max	min	max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay, input A to output Y (Figures 1)	1.2	-	150	-	150	-	180	ns
		2.0		33		36		44	
		2.7		23		26		33	
		3.0		19		21		26	
		4.5		14		16		20	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay, CS1 to output Y (Figures 2)	1.2	-	170	-	170	-	200	ns
		2.0		35		39		49	
		2.7		26		29		36	
		3.0		21		23		29	
		4.5		17		19		24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Output transition time, CS2 or CS3 to output Y (Figures 3)		-	170	-	170	-	200	ns
				35		39		49	
				26		29		36	
				21		23		29	
				17		19		24	
C <sub>IN</sub>	Input capacitance	5.0 0=+25°Ñ		7.0					pF

C <sub>PD</sub>	Power dissipation capacitance (per enabled output)	Typical @25°C, V <sub>CC</sub> =5.5 V		pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	90		

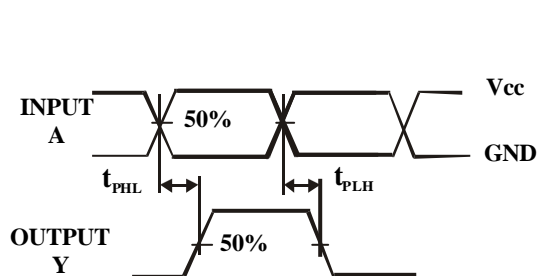


Figure 1. Switching Waveforms

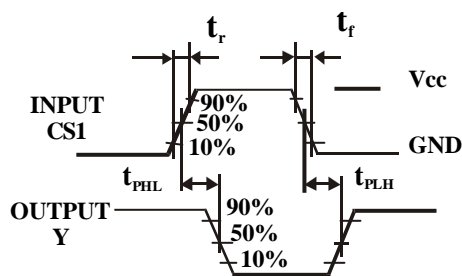


Figure 2. Switching Waveforms

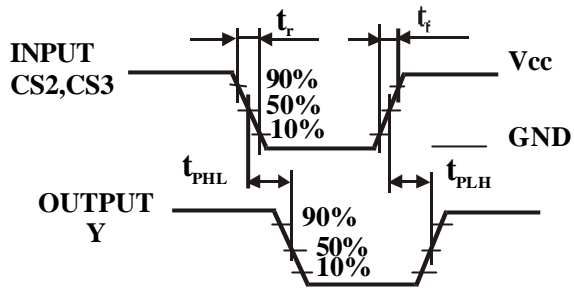
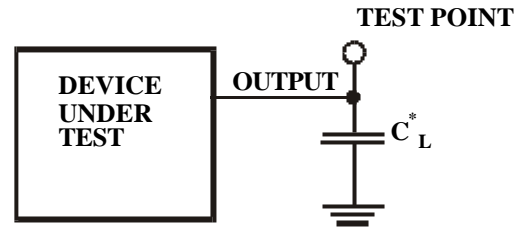


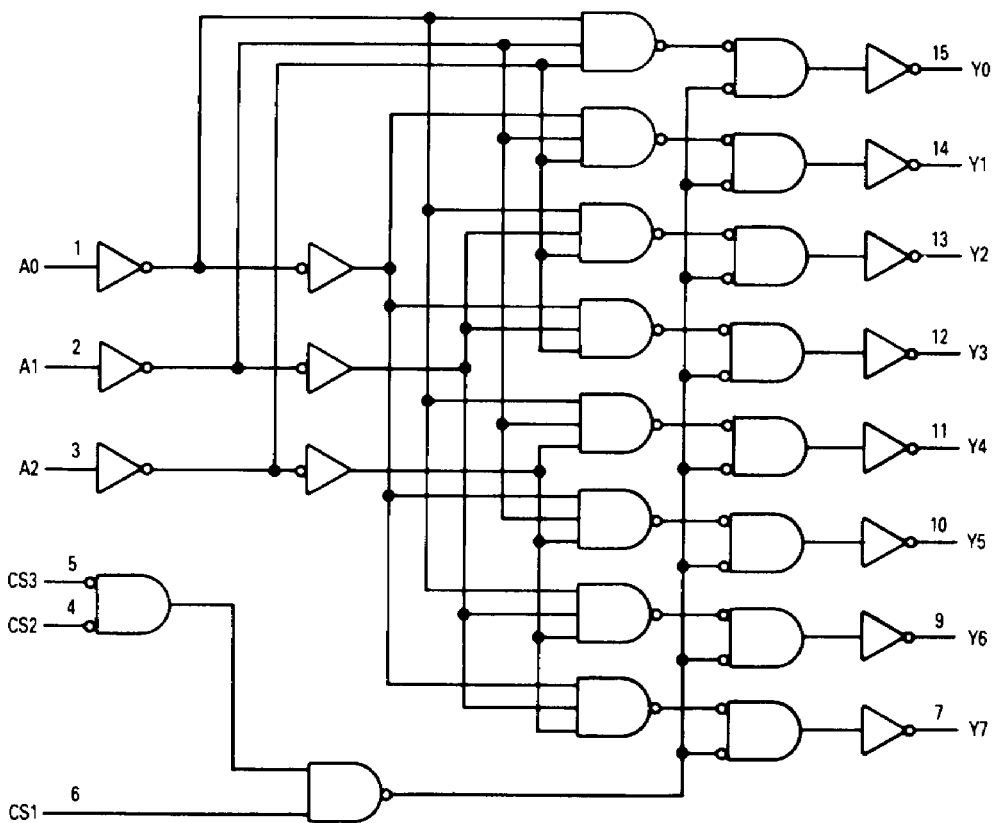
Figure 3. Switching Waveforms



\* Includes all probe and jig capacitance

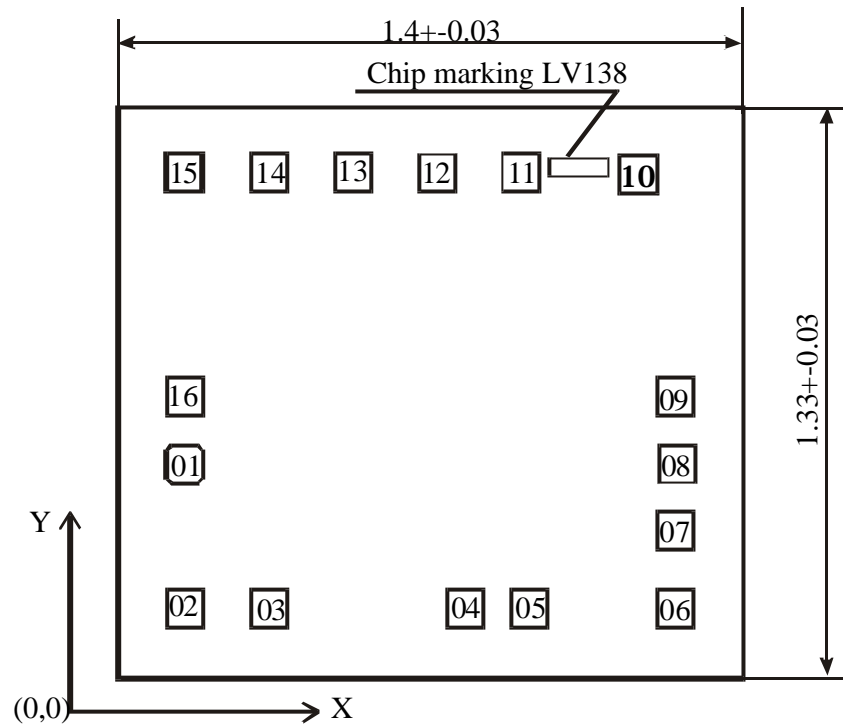
Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM





## CHIP PAD DIAGRAM



Location of marking (mm): left lower corner  $x = 0.950$ ,  $y = 1.175$ ;

Thickness of chip:  $0.46 \pm 0.02$  mm

## PAD LOCATION

Pad No.	Pad Name	X	Y	Pad size (mm)
01	AO	0.118	0.429	0.100 x 0.100
02	A1	0.118	0.115	0.100 x 0.100
03	A2	0.395	0.115	0.100 x 0.100
04	CS2	0.709	0.115	0.100 x 0.100
05	CS3	0.877	0.115	0.100 x 0.100
06	CS1	1.191	0.115	0.100 x 0.100
07	Y7	1.191	0.283	0.100 x 0.100
08	GND	1.191	0.441	0.100 x 0.100
09	Y6	1.191	0.599	0.100 x 0.100
10	Y5	1.084	1.111	0.100 x 0.100
11	Y4	0.798	1.111	0.100 x 0.100
12	Y3	0.640	1.111	0.100 x 0.100
13	Y2	0.472	1.111	0.100 x 0.100
14	Y1	0.314	1.111	0.100 x 0.100
15	Y0	0.131	1.111	0.100 x 0.100
16	Vcc	0.118	0.597	0.100 x 0.100

\* Note: Pad location is given as per passivation layer

