

IN74LV174

Hex D-type flip-flop with reset; positive edge-trigger

The 74LV174 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT174.

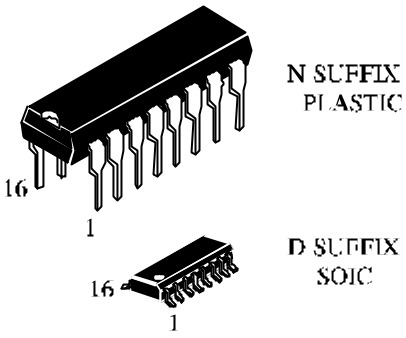
The 74LV174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the MR input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0 μA ; 0.1 μA at $\dot{O} = 25^\circ\text{N}$
- Output current: 6 mA at $V_{cc} = 3.0\text{ V}$; 12 mA at $V_{cc} = 4.5\text{ V}$
- High Noise Immunity Characteristic of CMOS Devices



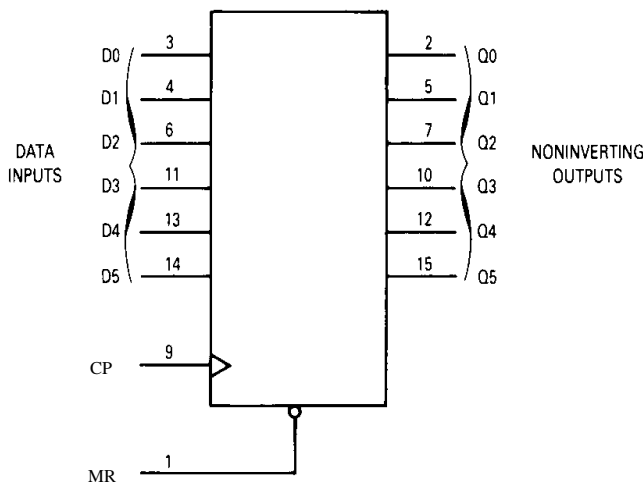
N SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION

IN74LV174N Plastic
 IN74LV174D SOIC
 IZ74LV174 Chip
 $T_A = -40^\circ$ to 125° C for all packages




LOGIC DIAGRAM



PIN ASSIGNMENT

$\overline{\text{MR}}$	1	16	V_{CC}
Q0	2	15	Q5
D0	3	14	D5
D1	4	13	D4
Q1	5	12	Q4
D2	6	11	D3
Q2	7	10	Q3
GND	8	9	CP

FUNCTION TABLE

Inputs			Outputs
$\overline{\text{MR}}$	CP	Dn	Qn
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

H= high level
 L = low level
 X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK}^{*1}	Input diode current	± 20	mA
I_{OK}^{*2}	Output diode current	± 50	mA
I_O^{*3}	Output source or sink current	± 25	mA
I_{CC}	V_{CC} current	± 50	mA
I_{GND}	GND current	± 50	mA
P_D	Power dissipation per package: * ⁴ Plastic DIP SO	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

*¹ $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$

*² $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$

*³ $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$

*⁴ Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.2	5.5	V
V_{IN}	DC Input Voltage	0	V_{CC}	V
V_{OUT}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns/V
	$1.0\text{ V} \leq V_{CC} < 2.0\text{ V}$	0	500	
	$2.0\text{ V} \leq V_{CC} < 2.7\text{ V}$	0	200	
	$2.7\text{ V} \leq V_{CC} < 3.6\text{ V}$	0	100	
	$3.6\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	0	50	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit						Unit	
				-40°C to 25°C		85°C		125°C			
				min	max	min	max	min	max		
V _{IH}	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V	
			2.0	1.4	-	1.4	-	1.4	-		
			2.7	2.0	-	2.0	-	2.0	-		
			3.0	2.0	-	2.0	-	2.0	-		
			3.6	2.0	-	2.0	-	2.0	-		
			4.5	3.15	-	3.15	-	3.15	-		
			5.5	3.85	-	3.85	-	3.85	-		
V _{IL}	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V	
			2.0	-	0.6	-	0.6	-	0.6		
			2.7	-	0.8	-	0.8	-	0.8		
			3.0	-	0.8	-	0.8	-	0.8		
			3.6	-	0.8	-	0.8	-	0.8		
			4.5	-	1.35	-	1.35	-	1.35		
			5.5	-	1.65	-	1.65	-	1.65		
V _{OH}	HIGH level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	1.2	1.05	-	1.0	-	1.0	-	V	
			2.0	1.85	-	1.8	-	1.8	-		
			2.7	2.55	-	2.5	-	2.5	-		
			3.0	2.85	-	2.8	-	2.8	-		
			3.6	3.45	-	3.4	-	3.4	-		
			4.5	4.35	-	4.3	-	4.3	-		
			5.5	5.35	-	5.3	-	5.3	-		
			V _I = V _{IH} or V _{IL} I _O = -6 mA	3.0	2.48	-	2.34	-	2.20	-	V
			V _I = V _{IH} or V _{IL} I _O = -12 mA	4.5	3.70	-	3.60	-	3.50	-	V
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	1.2	-	0.15	-	0.2	-	0.2	V	
			2.0	-	0.15	-	0.2	-	0.2		
			2.7	-	0.15	-	0.2	-	0.2		
			3.0	-	0.15	-	0.2	-	0.2		
			3.6	-	0.15	-	0.2	-	0.2		
			4.5	-	0.15	-	0.2	-	0.2		
			5.5	-	0.15	-	0.2	-	0.2		
			V _I = V _{IH} or V _{IL} I _O = 6 mA	3.0	-	0.33	-	0.40	-	0.50	V
			V _I = V _{IH} or V _{IL} I _O = 12 mA	4.5	-	0.40	-	0.55	-	0.65	V
I _I	Input current	V _I = V _{CC} or 0 V	5.5	-	±0.1	-	±1.0	-	±1.0	μA	
I _{CC}	Supply current	V _I = V _{CC} or 0 V I _O = 0 μA	5.5	-	8.0	-	80	-	160	μA	
I _{CC1}	Additional quiescent supply	V _I = V _{CC} - 0.6 V	2.7	-	0.2	-	0.5	-	0.85	mA	
			3.6	-	0.2	-	0.5	-	0.85		

current per input									
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AC ELECTRICAL CHARACTERISTICS ($C_L=50$ pF, $R_L = 1$ k Ω , $t_r=t_f=2.5$ ns)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t _{PHL} , t _{PLH}	Propagation delay CP to Qn	V _I = 0 V or V _{CC} Figure 1, 4	1.2	-	200	-	230	-	260	ns
			2.0	-	34	-	43	-	53	
			2.7	-	24	-	31	-	39	
			3.0	-	20	-	25	-	31	
			4.5	-	17	-	21	-	26	
t _{PHL}	Propagation delay MR to Qn	V _I = 0 V or V _{CC} Figure 2, 4	1.2	-	160	-	190	-	220	ns
			2.0	-	34	-	43	-	53	
			2.7	-	24	-	31	-	39	
			3.0	-	20	-	25	-	31	
			4.5	-	17	-	21	-	26	
t _w	Clock pulse width HIGH or LOW	V _I = 0 V or V _{CC} Figure 1, 4	1.2	100	-	140	-	180	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	14	-	17	-	20	-	
t _w	Master reset pulse width LOW	V _I = 0 V or V _{CC} Figure 1, 4	1.2	100	-	140	-	180	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	14	-	17	-	20	-	
t _{REM}	Removal time MR to CP	V _I = 0 V or V _{CC} Figure 3, 4	1.2	40	-	60	-	80	-	ns
			2.0	19	-	22	-	26	-	
			2.7	13	-	16	-	19	-	
			3.0	11	-	13	-	15	-	
			4.5	9	-	11	-	13	-	
t _{SU}	Set-up time Dn to CP	V _I = 0 V or V _{CC} Figure 3, 4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
t _h	Hold time Dn to CP	V _I = 0 V or V _{CC} Figure 2, 4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
C _I	Input capacitance	$\dot{O}_A = 25^\circ\text{C}$	5.0	-	7.0	-	-	-	pF	
C _{PD}	Power dissipation capacitance (per flip-flop)	V _I = 0 V or V _{CC} T _A = 25°C	5.5	-	34	-	-	-	pF	
f _{max}	Maximum clock pulse frequency	V _I = 0 V or V _{CC} Figure 1	1.2	-	2.0	-	1.0	-	1.0	MHz
			2.0	-	16	-	14	-	12	
			2.7	-	22	-	19	-	16	
			3.0	-	27	-	24	-	20	
			4.5	-	32	-	27	-	24	

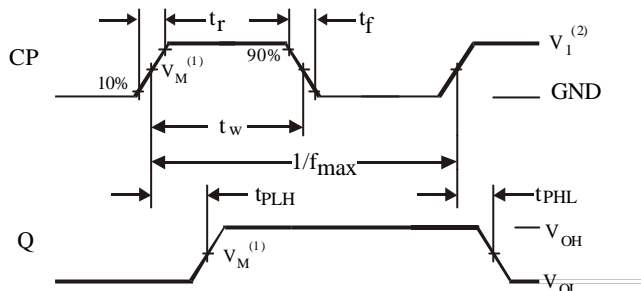


Figure 1. Switching Waveforms

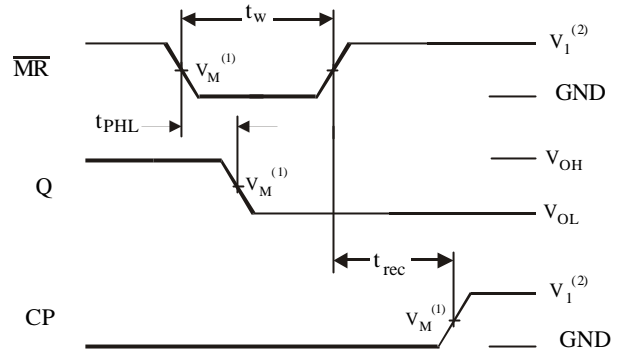


Figure 2. Switching Waveforms

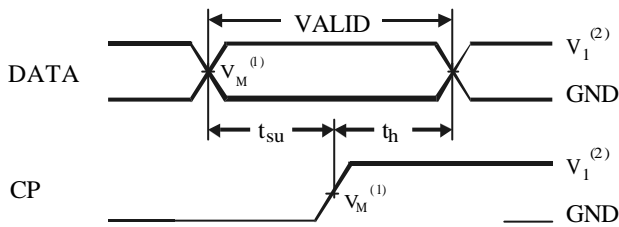
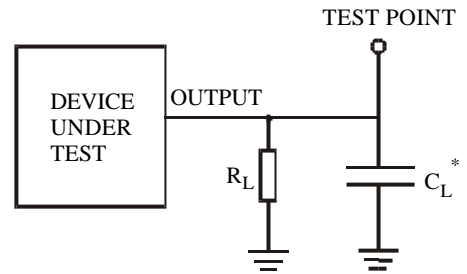


Figure 3. Switching Waveforms

Note:

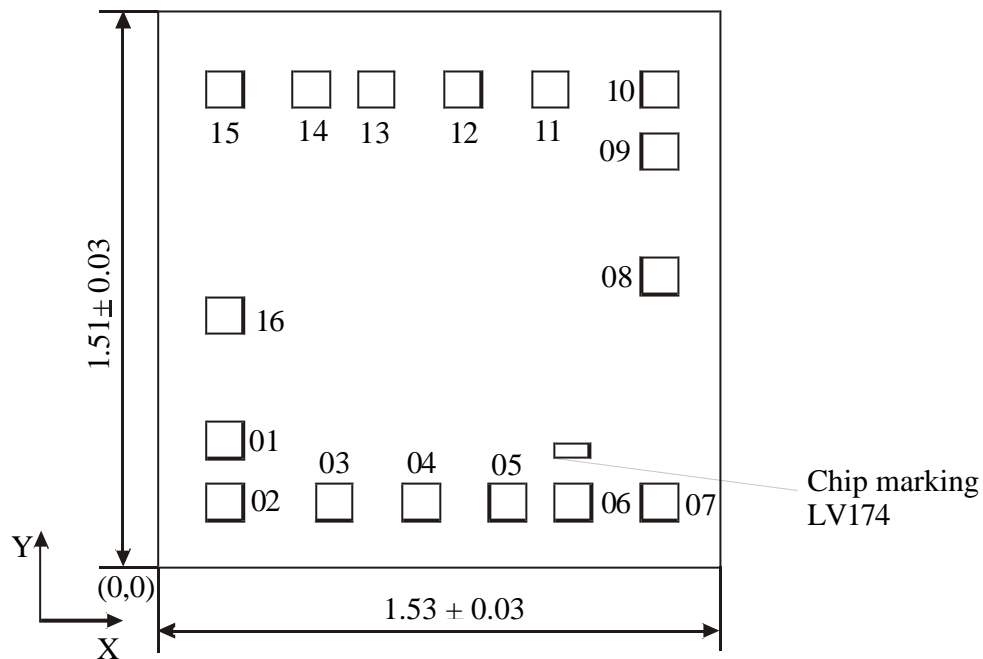
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} = 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} = 1.2 \text{ V}, 2.0 \text{ V}, 3.0 \text{ V}, 4.5 \text{ V}$
- (2) $V_1 = V_{CC}$ at $V_{CC} = 1.2 \text{ V}, 2.0 \text{ V}, 2.7 \text{ V}, 4.5 \text{ V}$
 $V_1 = 2.7 \text{ V}$ at $V_{CC} = 3.0 \text{ V}$



* Includes all probe and jig capacitance

Figure 4. Test Circuit

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=1.080$, $y=0.296$

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	MR	0.132	0.295	0.100 x 0.100
02	Q0	0.132	0.127	0.100 x 0.100
03	D0	0.430	0.127	0.100 x 0.100
04	D1	0.667	0.127	0.100 x 0.100
05	Q1	0.902	0.127	0.100 x 0.100
06	D2	1.080	0.127	0.100 x 0.100
07	Q2	1.315	0.127	0.100 x 0.100
08	GND	1.315	0.741	0.100 x 0.100
09	CP	1.315	1.079	0.100 x 0.100
10	Q3	1.315	1.247	0.100 x 0.100
11	D3	1.017	1.247	0.100 x 0.100
12	Q4	0.780	1.247	0.100 x 0.100
13	D4	0.545	1.247	0.100 x 0.100
14	D5	0.367	1.247	0.100 x 0.100
15	Q5	0.132	1.247	0.100 x 0.100
16	V _{CC}	0.132	0.633	0.100 x 0.100

Note: Pad location is given as per metallization layer