

OptiMOS[®] Power-Transistor
Features

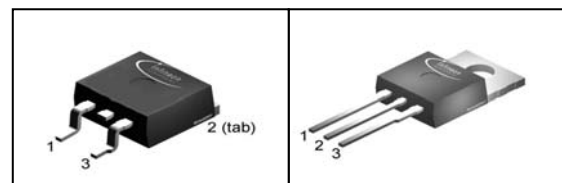
- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

Product Summary

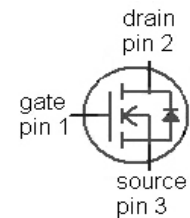
V_{DS}	55	V
$R_{DS(on),max}$ (SMD version)	11.7	mΩ
I_D	77	A

PG-TO263-3-2

PG-TO220-3-1



Type	Package	Ordering Code	Marking
IPB77N06S2-12	PG-TO263-3-2	SP0002-18173	2N0612
IPP77N06S2-12	PG-TO220-3-1	SP0002-18172	2N0612


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	77	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	56	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	308	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=77\text{ A}$	280	mJ
Gate source voltage ⁴⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	158	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	0.95	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁵⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=93\text{ }\mu\text{A}$	2.1	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=38\text{ A},$	-	9.8	12.0	m Ω
		$V_{GS}=10\text{ V}, I_D=38\text{ A},$ SMD version	-	9.5	11.7	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1770	-	pF
Output capacitance	C_{oss}		-	460	-	
Reverse transfer capacitance	C_{rss}		-	120	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=77\text{ A}, R_G=6.2\ \Omega$	-	14	-	ns
Rise time	t_r		-	27	-	
Turn-off delay time	$t_{d(off)}$		-	34	-	
Fall time	t_f		-	26	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=44\text{ V}, I_D=77\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	9	12	nC
Gate to drain charge	Q_{gd}		-	18	28	
Gate charge total	Q_g		-	45	60	
Gate plateau voltage	$V_{plateau}$		-	5.6	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	77	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	308	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=77\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	45	60	ns
Reverse recovery charge ²⁾	Q_{rr}		-	64	80	

¹⁾ Current is limited by die area; with an $R_{thJC} = 0.95\text{ K/W}$ the chip is able to carry 77 A at 25°C. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

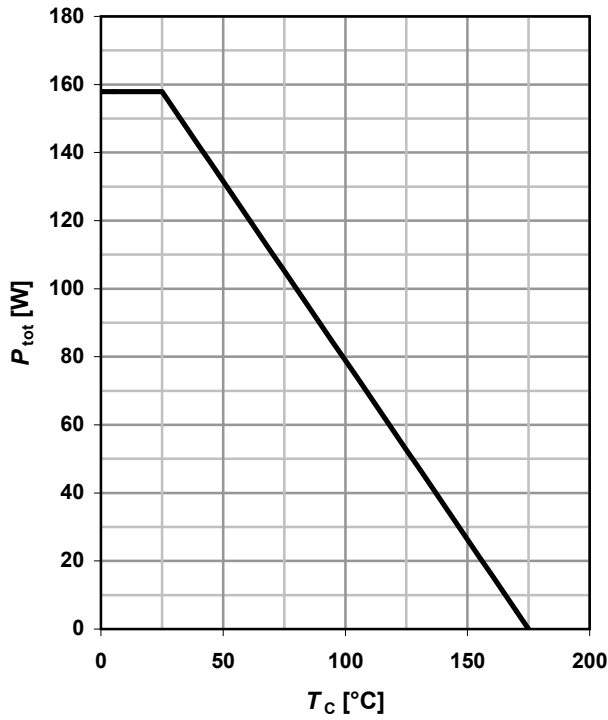
³⁾ See diagram 13.

⁴⁾ Qualified at -20V and +20V.

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

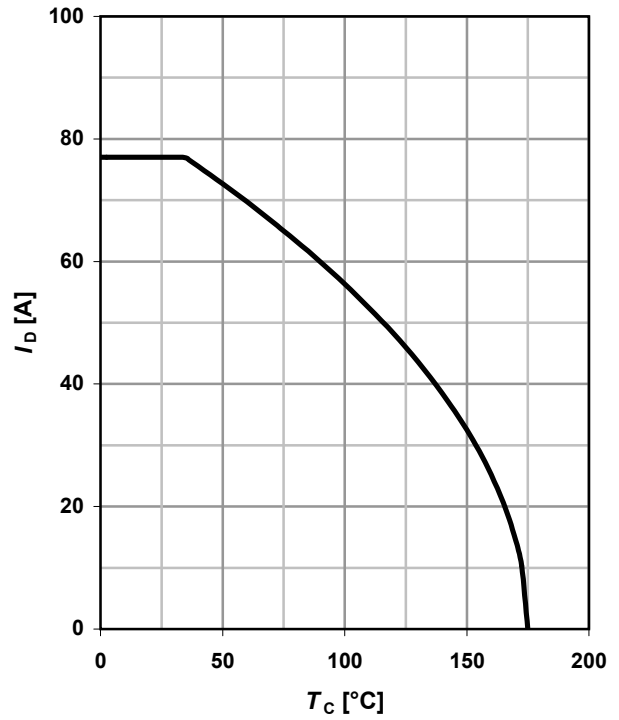
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 V$



2 Drain current

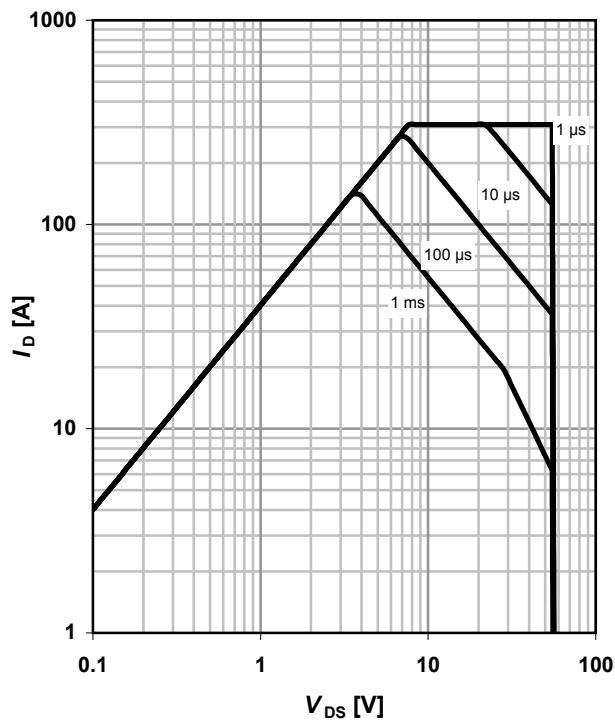
$I_D = f(T_C); V_{GS} \geq 10 V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25^\circ C; D = 0$

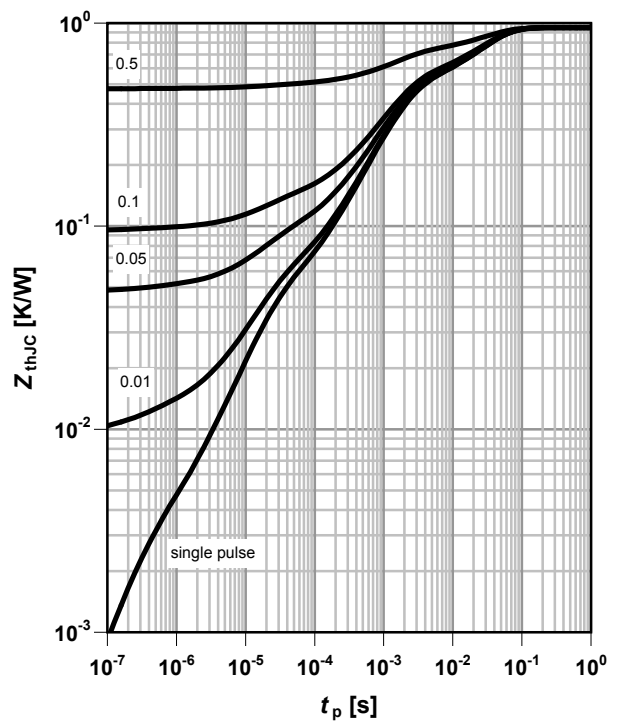
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

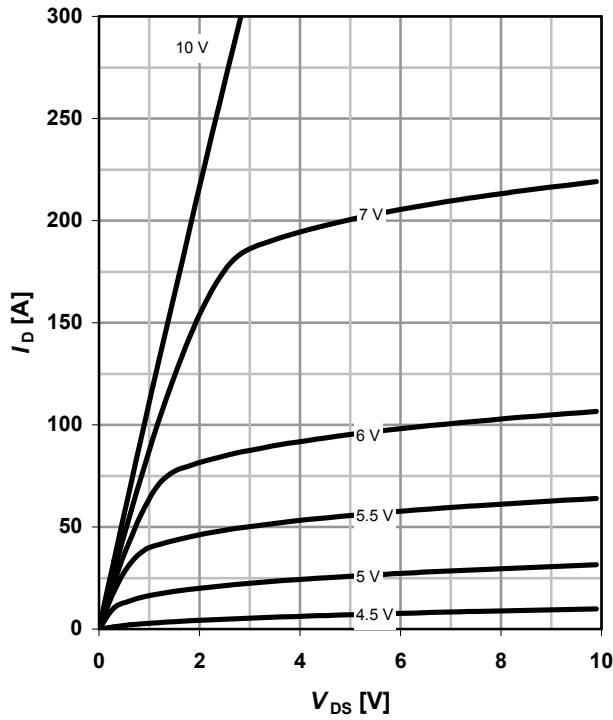
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

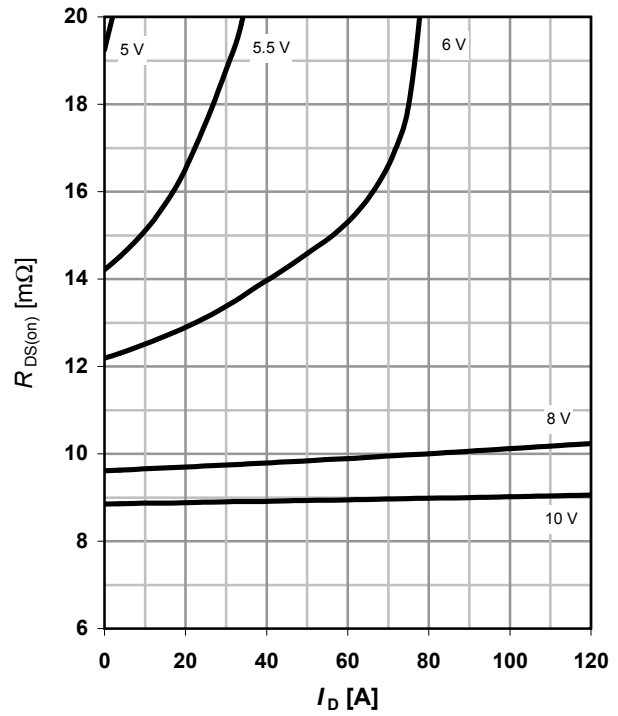
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

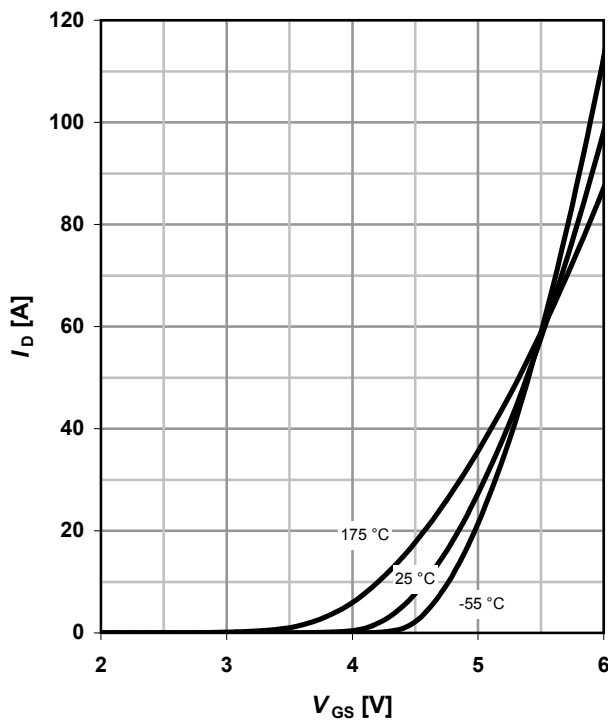
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

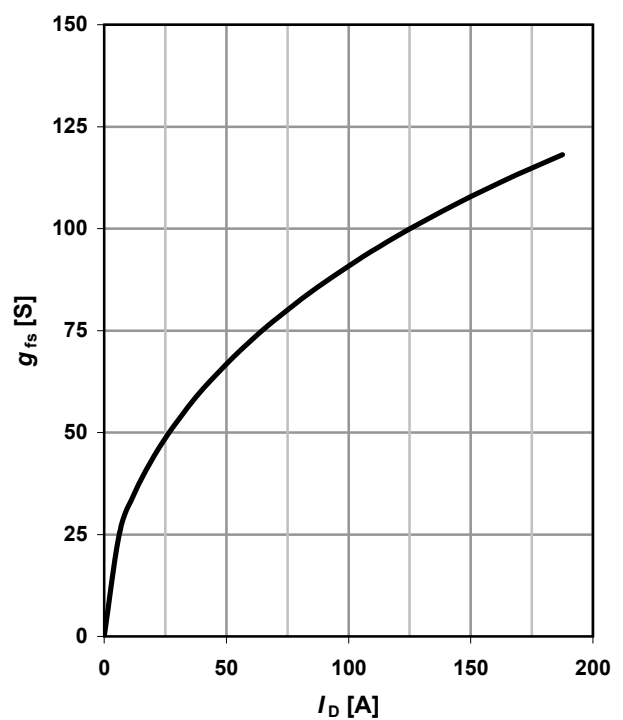
parameter: T_j



8 Typ. Forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

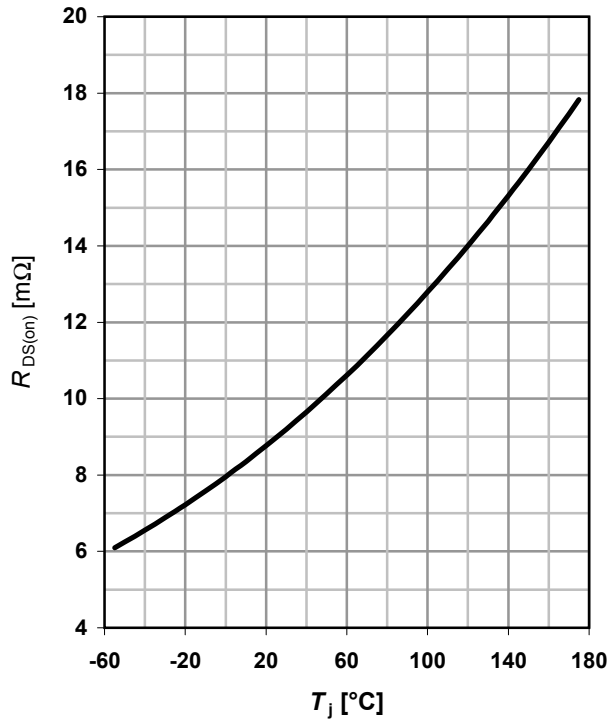
parameter: g_{fs}



9 Typ. Drain-source on-state resistance

$R_{DS(ON)} = f(T_j)$

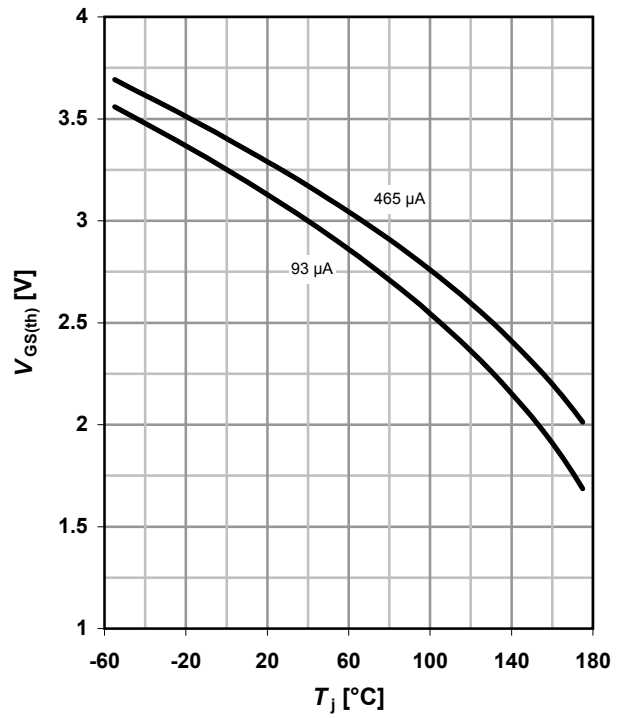
parameter: $I_D = 80 \text{ A}$; $V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

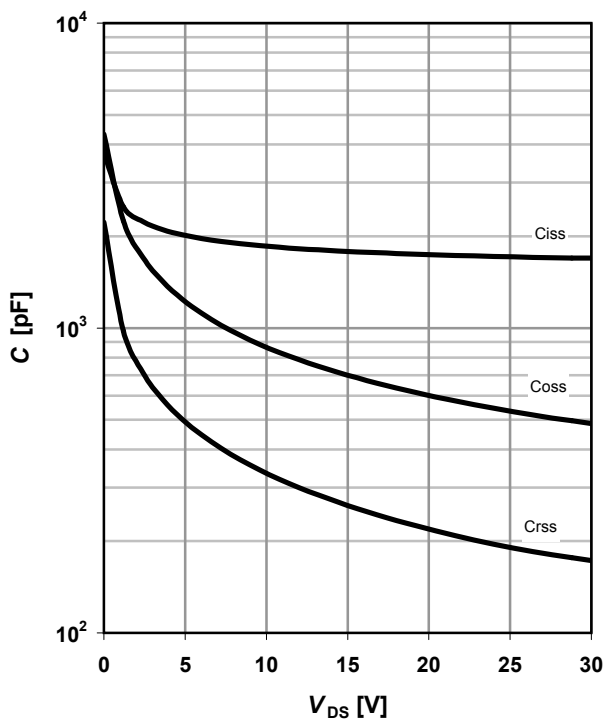
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

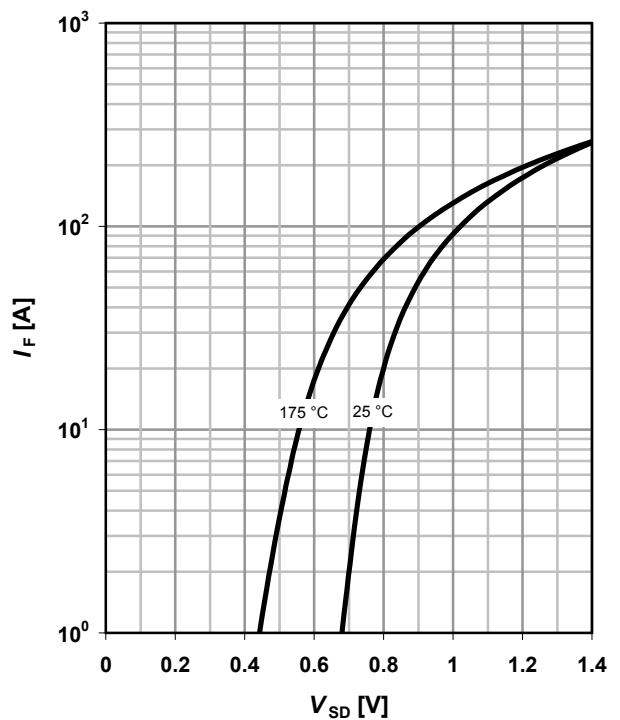
$C = f(V_{DS})$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$



12 Typical forward diode characteristics

$I_F = f(V_{SD})$

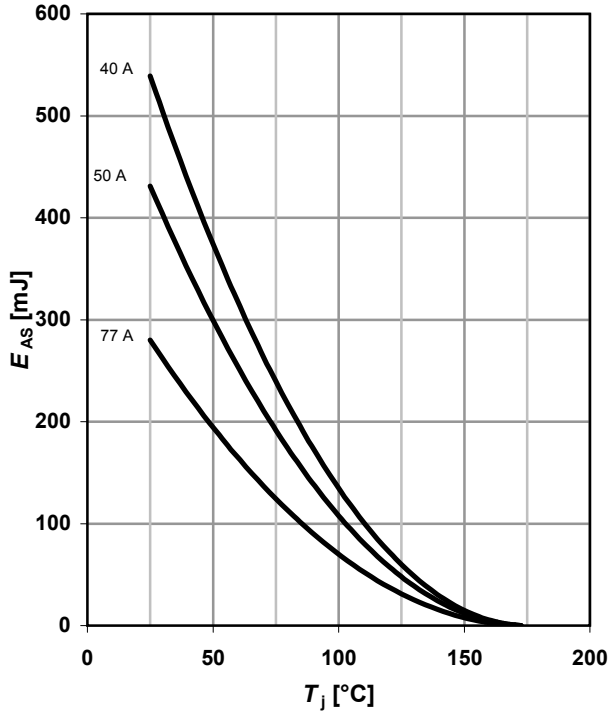
parameter: T_j



13 Typical avalanche energy

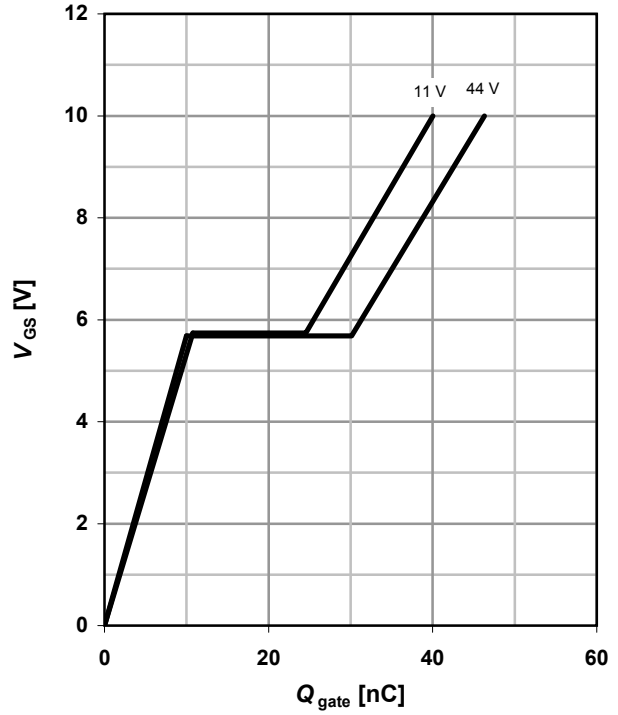
$E_{AS} = f(T_j)$

parameter: I_D



14 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 80 \text{ A pulsed}$



15 Typ. drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



16 Gate charge waveforms



Published by
Infineon Technologies AG
St.-Martin-Straße 53
D-81541 München
© Infineon Technologies AG 2004
All Rights Reserved.

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices, please contact your nearest Infineon Technologies Office (www.infineon.com)

Warnings

Due to technical requirements, components may contain dangerous substances.
For information on the types in question, please contact your nearest Infineon Technologies Office.

Infineon Technologies' components may only be used in life-support devices or systems with the expressed written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.