

IR2125(S) & (PbF)

CURRENT LIMITING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
 Fully operational to +500V
 Tolerant to negative transient voltage
 dV/dt immune
- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input
- 2.5V, 5V and 15V input logic compatible
- Also available LEAD-Free

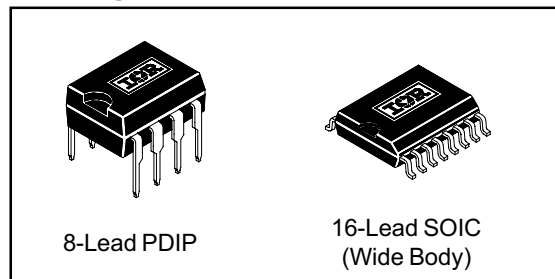
Description

The IR2125(S) is a high voltage, high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 2.5V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle by cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting conditions and latched shutdown. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 500 volts.

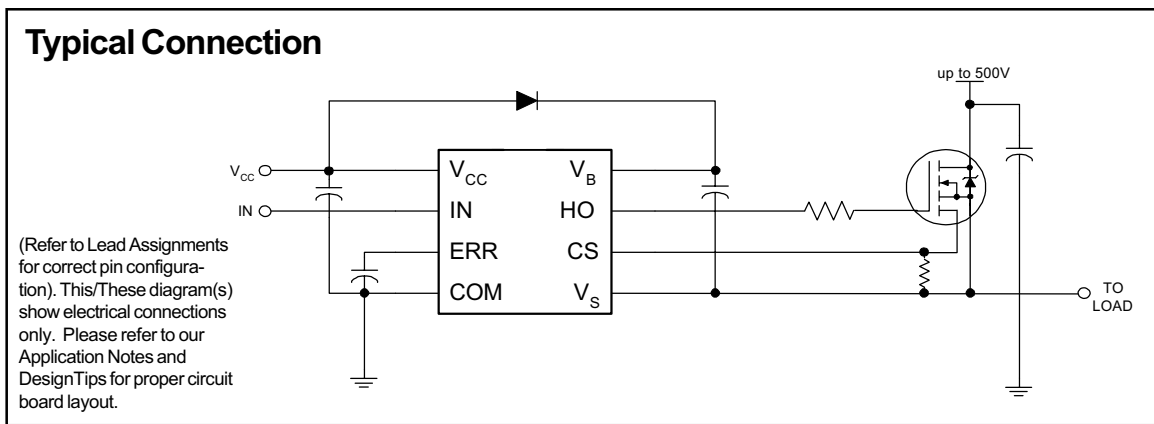
Product Summary

| | |
|---------------------------|-------------------------|
| V_{OFFSET} | 500V max. |
| I_{O+/-} | 1A / 2A |
| V_{OUT} | 12 - 18V |
| V_{Csth} | 230 mV |
| ton/off (typ.) | 150 & 150 ns |

Packages



Typical Connection



IR2125(S) & (PbF)

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units |
|---------------------|--|----------------------|-----------------------|-------|
| V _B | High Side Floating Supply Voltage | -0.3 | 525 | V |
| V _S | High Side Floating Offset Voltage | V _B - 25 | V _B + 0.3 | |
| V _{HO} | High Side Floating Output Voltage | V _S - 0.3 | V _B + 0.3 | |
| V _{CC} | Logic Supply Voltage | -0.3 | 25 | |
| V _{IN} | Logic Input Voltage | -0.3 | V _{CC} + 0.3 | |
| V _{ERR} | Error Signal Voltage | -0.3 | V _{CC} + 0.3 | |
| V _{CS} | Current Sense Voltage | V _S - 0.3 | V _B + 0.3 | |
| dV _S /dt | Allowable Offset Supply Voltage Transient | — | 50 | V/ns |
| P _D | Package Power Dissipation @ T _A ≤ +25°C (8 lead PDIP) | — | 1.0 | W |
| | (16 lead SOIC) | — | 1.25 | |
| R _{thJA} | Thermal Resistance, Junction to Ambient (8 lead PDIP) | — | 125 | °C/W |
| | (16Lead SOIC) | — | 100 | |
| T _J | Junction Temperature | — | 150 | °C |
| T _S | Storage Temperature | -55 | 150 | |
| T _L | Lead Temperature (Soldering, 10 seconds) | — | 300 | |

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|------------------|-----------------------------------|---------------------|---------------------|-------|
| V _B | High Side Floating Supply Voltage | V _S + 12 | V _S + 18 | V |
| V _S | High Side Floating Offset Voltage | Note 1 | 500 | |
| V _{HO} | High Side Floating Output Voltage | V _S | V _B | |
| V _{CC} | Logic Supply Voltage | 0 | 18 | |
| V _{IN} | Logic Input Voltage | 0 | V _{CC} | |
| V _{ERR} | Error Signal Voltage | 0 | V _{CC} | |
| V _{CS} | Current Sense Signal Voltage | V _S | V _B | |
| T _A | Ambient Temperature | -40 | 125 | °C |

Note 1: Logic operational for V_S of -5 to +500V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 3300 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figures 3 through 6.

| Symbol | Definition | Figure | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|--------|------|------|------|---------------|---|
| t_{on} | Turn-On Propagation Delay | 7 | — | 170 | 240 | ns | $V_{IN} = 0 \text{ \& } 5V$ $V_S = 0 \text{ to } 600V$ |
| t_{off} | Turn-Off Propagation Delay | 8 | — | 200 | 270 | | |
| t_{sd} | ERR Shutdown Propagation Delay | 9 | — | 1.7 | 2.2 | μs | |
| t_r | Turn-On Rise Time | 10 | — | 43 | 60 | ns | |
| t_f | Turn-Off Fall Time | 11 | — | 26 | 35 | | |
| t_{cs} | CS Shutdown Propagation Delay | 12 | — | 0.7 | 1.2 | μs | |
| t_{err} | CS to ERR Pull-Up Propagation Delay | 13 | — | 9.0 | 12 | | $C_{ERR} = 270 \text{ pF}$ |

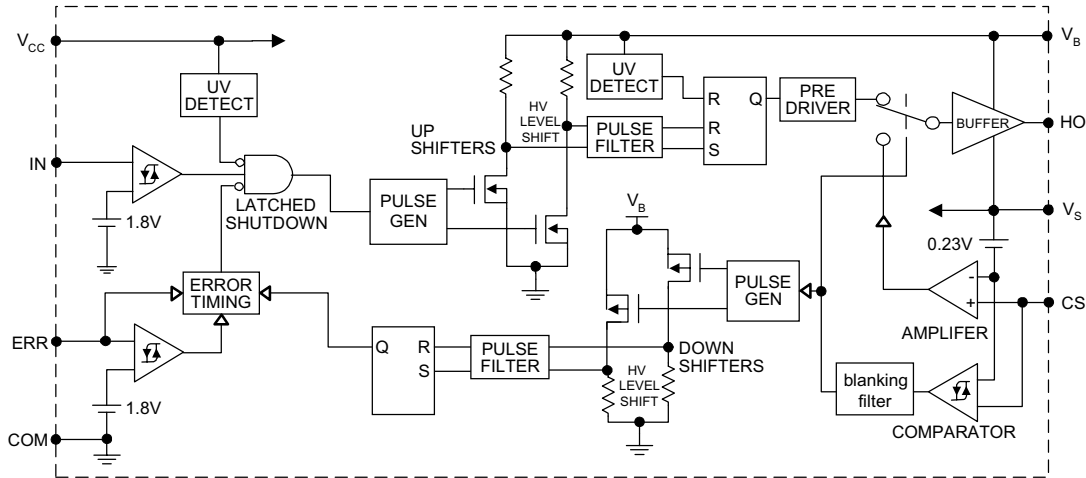
Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S .

| Symbol | Definition | Figure | Min. | Typ. | Max. | Units | Test Conditions | |
|-------------|---|--------|------|------|------|---------------|--|--|
| V_{IH} | Logic "1" Input Voltage | 14 | 2.2 | — | — | V | | |
| V_{IL} | Logic "0" Input Voltage | 15 | — | — | 0.8 | | | |
| V_{CSTH+} | CS Input Positive Going Threshold | 16 | 150 | 230 | 320 | mV | | |
| V_{CSTH-} | CS Input Negative Going Threshold | 17 | 130 | 210 | 300 | | | |
| V_{OH} | High Level Output Voltage, $V_{BIAS} - V_O$ | 18 | — | — | 100 | | $I_O = 0A$ | |
| V_{OL} | Low Level Output Voltage, V_O | 19 | — | — | 100 | | $I_O = 0A$ | |
| I_{LK} | Offset Supply Leakage Current | 20 | — | — | 50 | μA | $V_B = V_S = 500V$ | |
| I_{QBS} | Quiescent V_{BS} Supply Current | 21 | — | 400 | 1000 | | $V_{IN} = V_{CS} = 0V \text{ or } 5V$ | |
| I_{QCC} | Quiescent V_{CC} Supply Current | 22 | — | 700 | 1200 | | $V_{IN} = V_{CS} = 0V \text{ or } 5V$ | |
| I_{IN+} | Logic "1" Input Bias Current | 23 | — | 4.5 | 10 | | $V_{IN} = 5V$ | |
| I_{IN-} | Logic "0" Input Bias Current | 24 | — | — | 1.0 | | $V_{IN} = 0V$ | |
| I_{CS+} | "High" CS Bias Current | 25 | — | 4.5 | 10 | | $V_{CS} = 3V$ | |
| I_{CS-} | "Low" CS Bias Current | 26 | — | — | 1.0 | | $V_{CS} = 0V$ | |
| V_{BSUV+} | V_{BS} Supply Undervoltage Positive Going Threshold | 27 | 8.5 | 9.2 | 10.0 | | V | |
| V_{BSUV-} | V_{BS} Supply Undervoltage Negative Going Threshold | 28 | 7.7 | 8.3 | 9.0 | | | |
| V_{CCUV+} | V_{CC} Supply Undervoltage Positive Going Threshold | 29 | 8.3 | 8.9 | 9.6 | | | |
| V_{CCUV-} | V_{CC} Supply Undervoltage Negative Going Threshold | 30 | 7.3 | 8.0 | 8.7 | | | |
| I_{ERR} | ERR Timing Charge Current | 31 | 65 | 100 | 130 | μA | $V_{IN} = 5V, V_{CS} = 3V$ $ERR < V_{ERR+}$ | |
| I_{ERR+} | ERR Pull-Up Current | 32 | 8.0 | 15 | — | mA | $V_{IN} = 5V, V_{CS} = 3V$ $ERR > V_{ERR+}$ | |
| I_{ERR-} | ERR Pull-Down Current | 33 | 16 | 30 | — | | $V_{IN} = 0V$ | |
| I_{O+} | Output High Short Circuit Pulsed Current | 34 | 1.0 | 1.6 | — | A | $V_O = 0V, V_{IN} = 5V$ $PW \leq 10 \mu\text{s}$ | |
| I_{O-} | Output Low Short Circuit Pulsed Current | 35 | 2.0 | 3.3 | — | | $V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu\text{s}$ | |

IR2125(S) & (PbF)

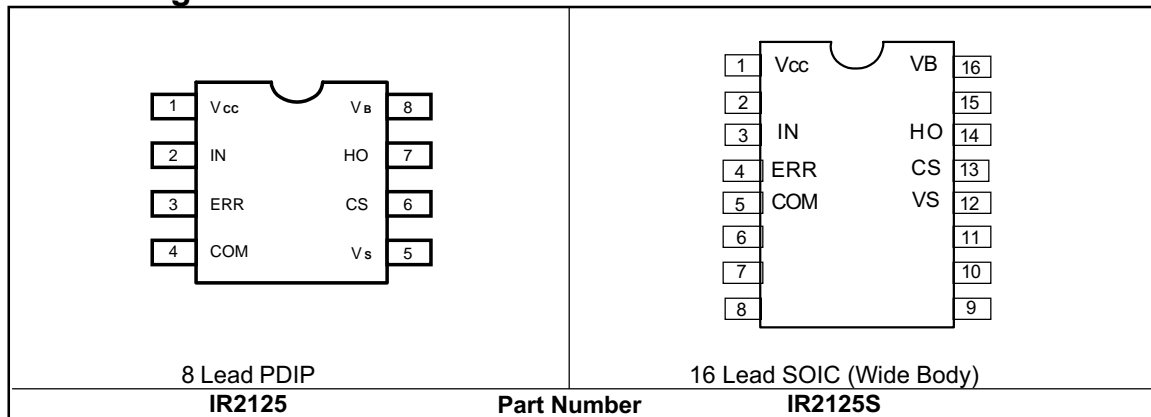
Functional Block Diagram



Lead Definitions

| Symbol | Description |
|-----------------|---|
| V _{CC} | Logic and gate drive supply |
| IN | Logic input for gate driver output (HO), in phase with HO |
| ERR | Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown |
| COM | Logic ground |
| V _B | High side floating supply |
| HO | High side gate drive output |
| V _S | High side floating supply return |
| CS | Current sense input to current sense comparator |

Lead Assignments



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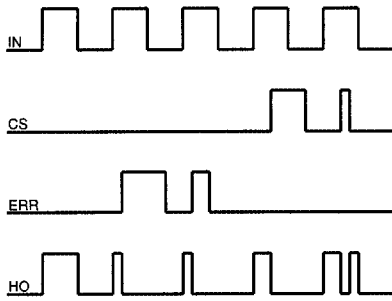


Figure 1. Input/Output Timing Diagram

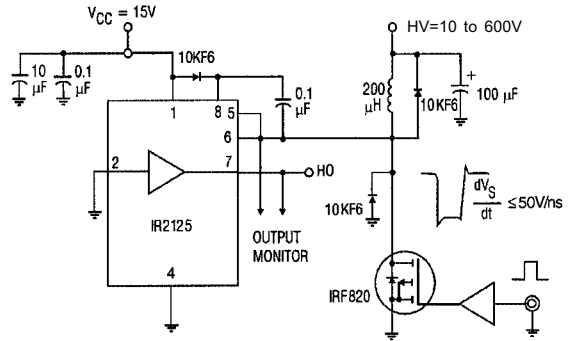


Figure 2. Floating Supply Voltage Transient Test Circuit

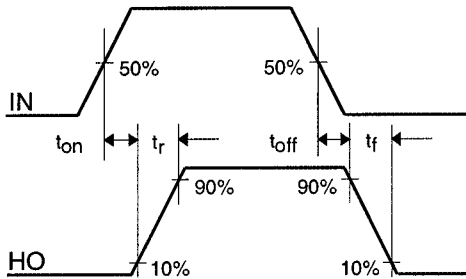


Figure 3. Switching Time Waveform Definitions

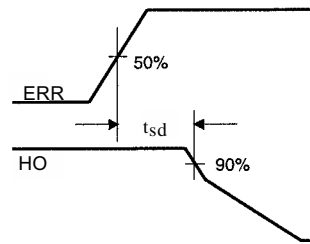


Figure 4. ERR Shutdown Waveform Definitions

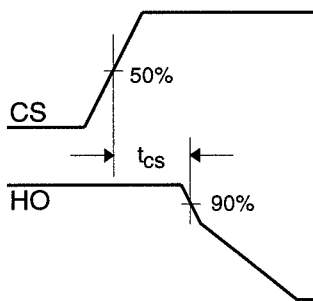


Figure 5. CS Shutdown Waveform Definitions

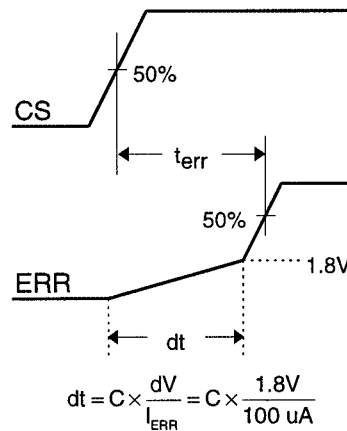


Figure 6. CS to ERR Waveform Definitions

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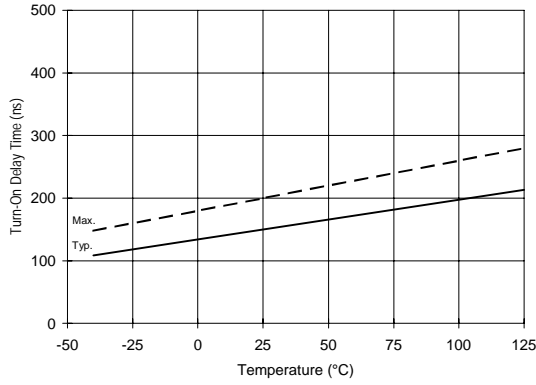


Figure 7A. Turn-On Time vs. Temperature

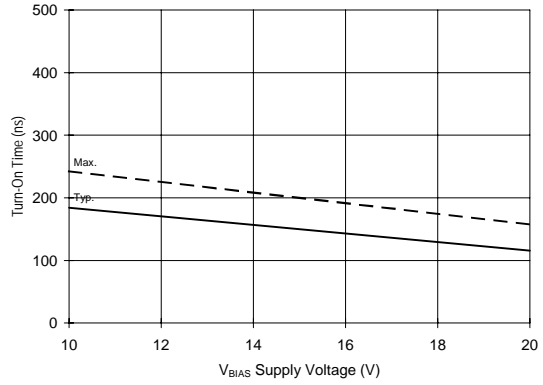


Figure 7B. Turn-On Time vs. Voltage

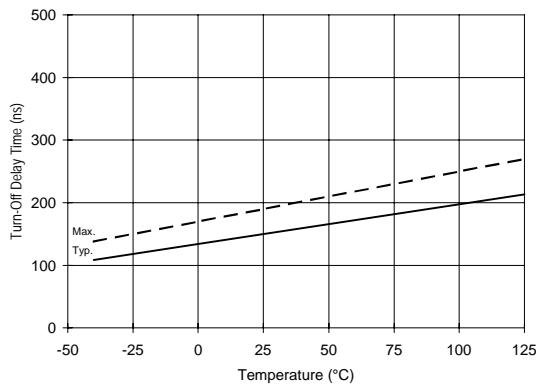


Figure 8A. Turn-Off Time vs. Temperature

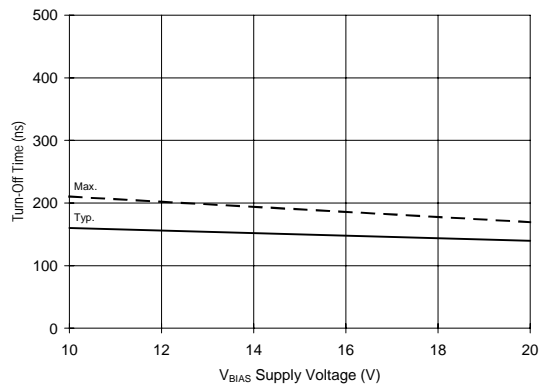


Figure 8B. Turn-Off Time vs. Voltage

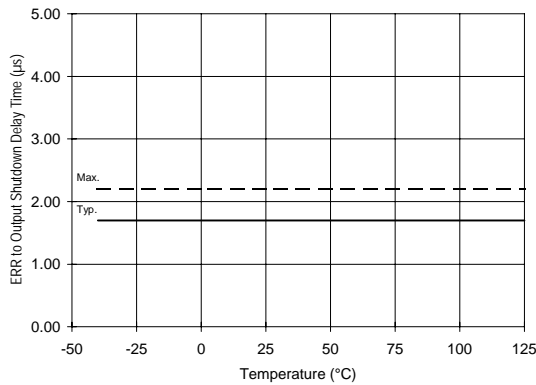


Figure 9A. ERR to Output Shutdown vs. Temperature

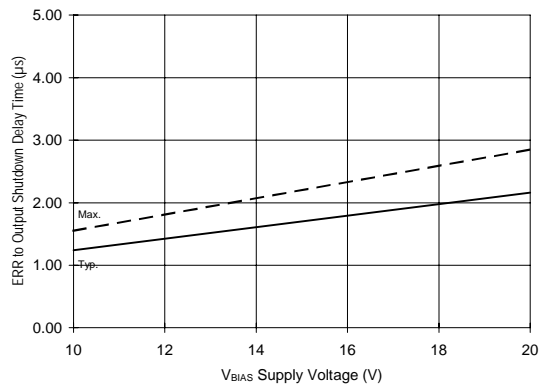


Figure 9B. ERR to Output Shutdown vs. Voltage

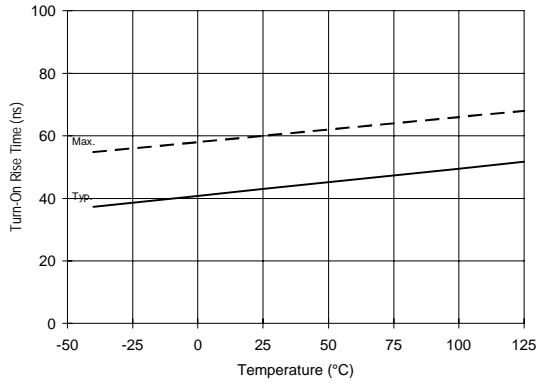


Figure 10A. Turn-On Rise Time vs. Temperature

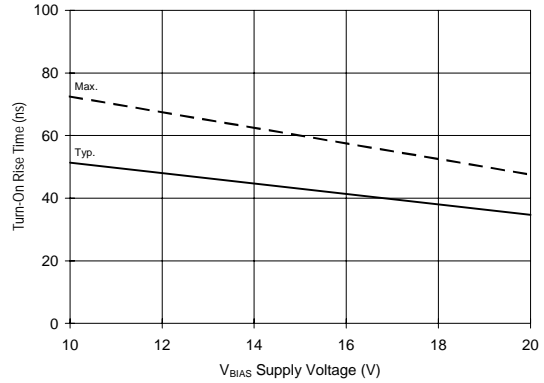


Figure 10B. Turn-On Rise Time vs. Voltage

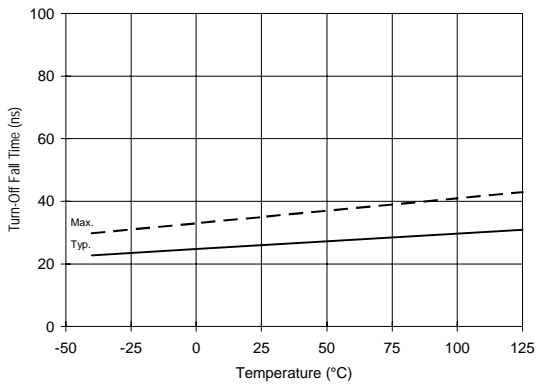


Figure 11A. Turn-Off Fall Time vs. Temperature

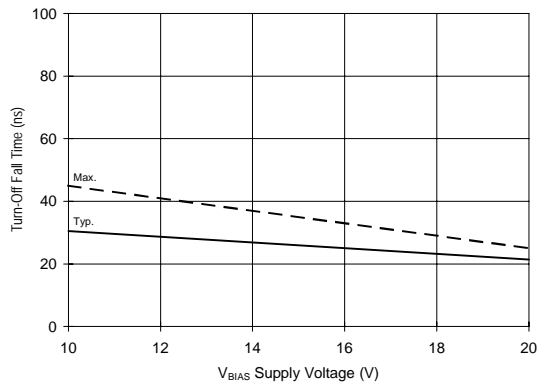


Figure 11B. Turn-Off Fall Time vs. Voltage

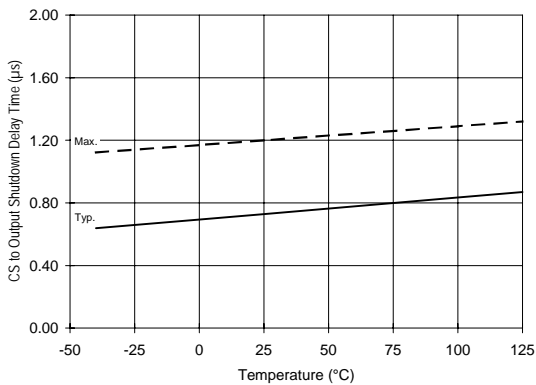


Figure 12A. CS to Output Shutdown vs. Temperature

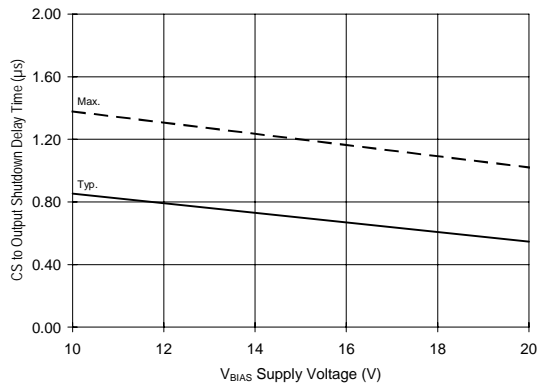


Figure 12B. CS to Output Shutdown vs. Voltage

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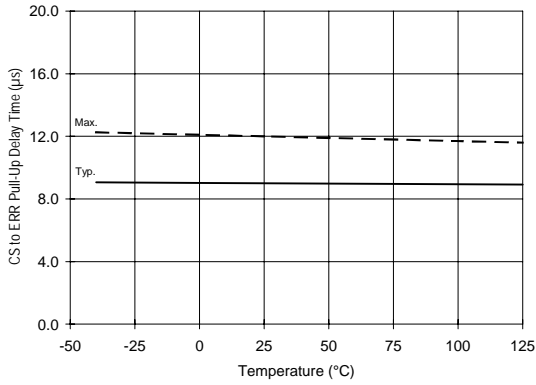


Figure 13A. CS to ERR Pull-Up vs. Temperature

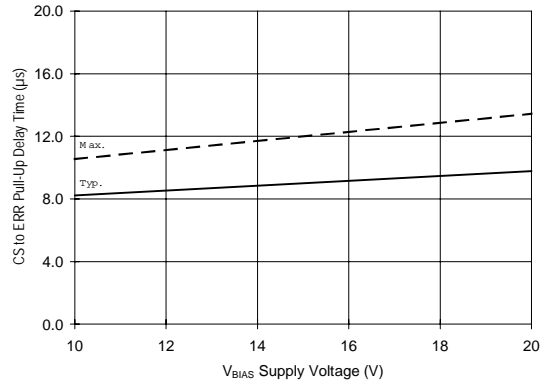


Figure 13B. CS to ERR Pull-Up vs. Voltage

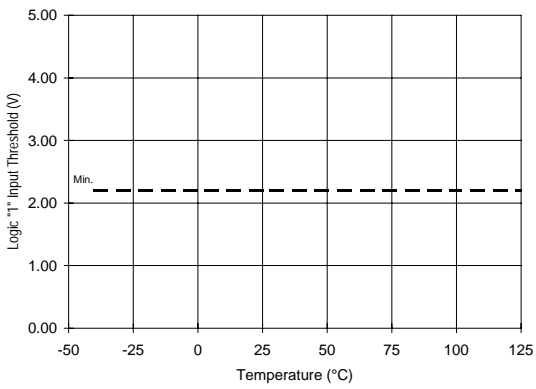


Figure 14A. Logic "1" Input Threshold vs. Temperature

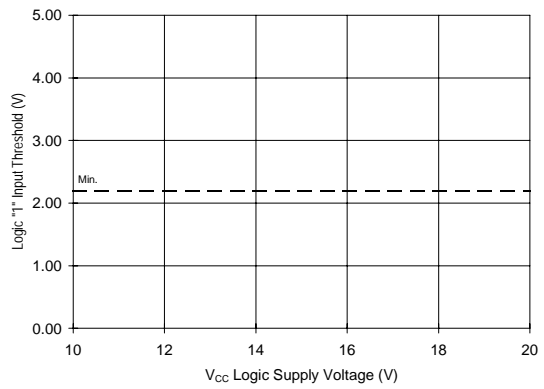


Figure 14B. Logic "1" Input Threshold vs. Voltage

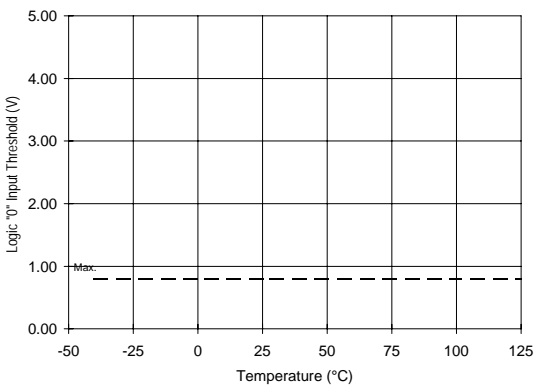


Figure 15A. Logic "0" Input Threshold vs. Temperature

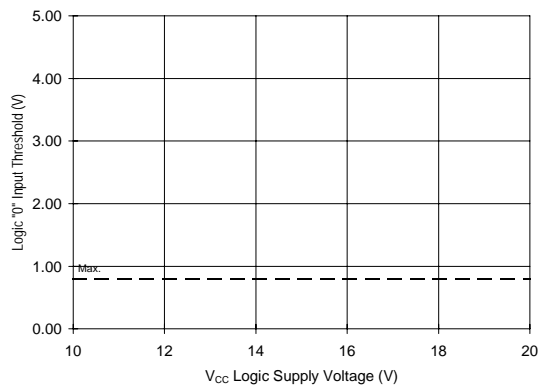


Figure 15B. Logic "0" Input Threshold vs. Voltage

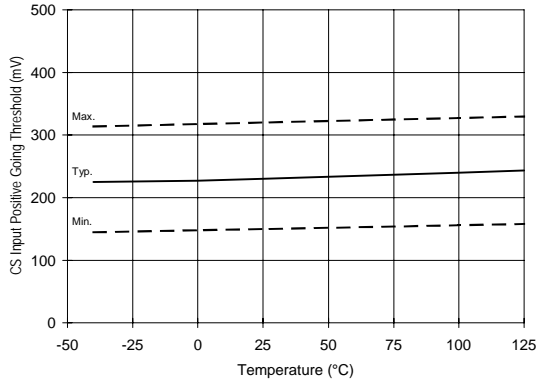


Figure 16A. CS Input Threshold (+) vs. Temperature

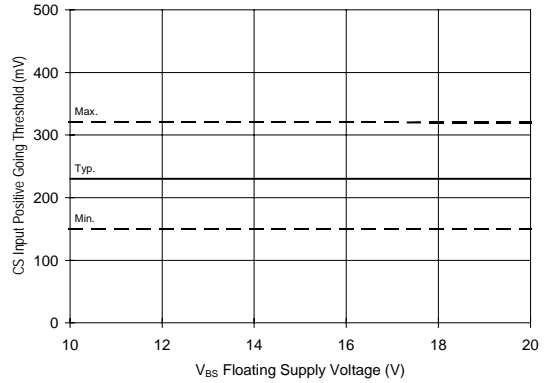


Figure 16B. CS Input Threshold (+) vs. Voltage

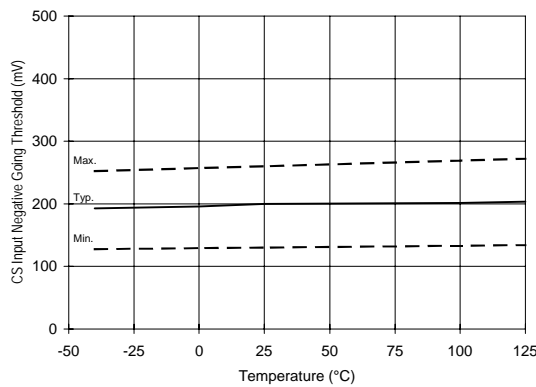


Figure 17A. CS Input Threshold (-) vs. Temperature

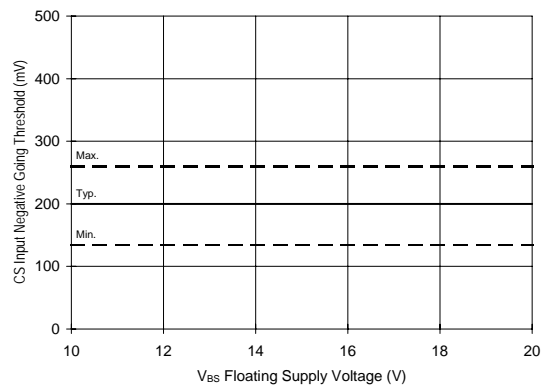


Figure 17B. CS Input Threshold (-) vs. Voltage

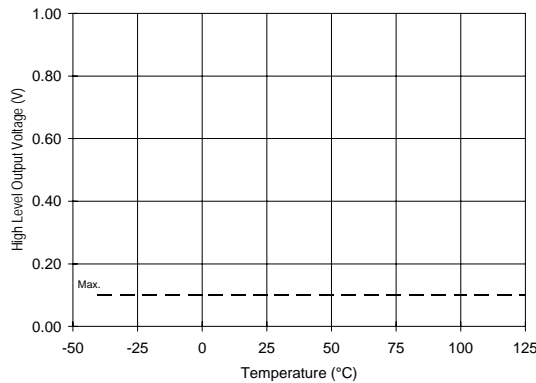


Figure 18A. High Level Output vs. Temperature

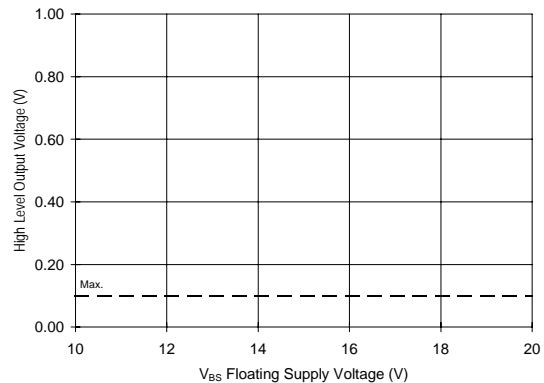


Figure 18B. High Level Output vs. Voltage

IR2125(S) & (PbF)

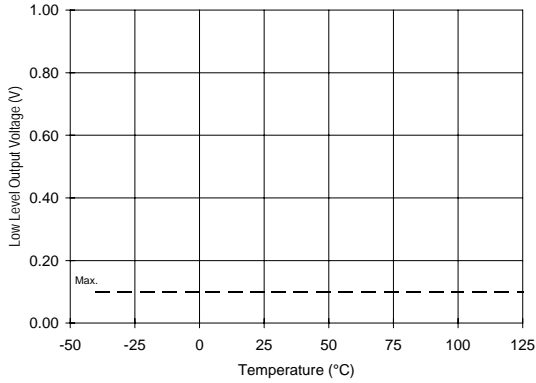


Figure 19A. Low Level Output vs. Temperature

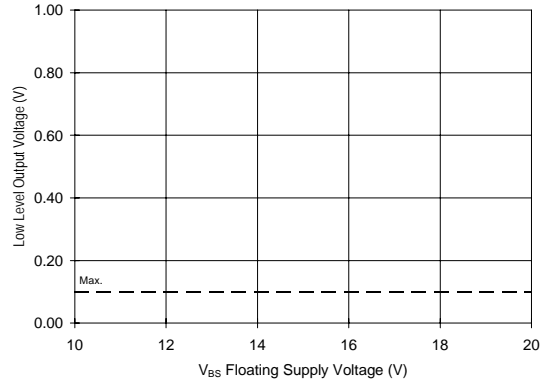


Figure 19B. Low Level Output vs. Voltage

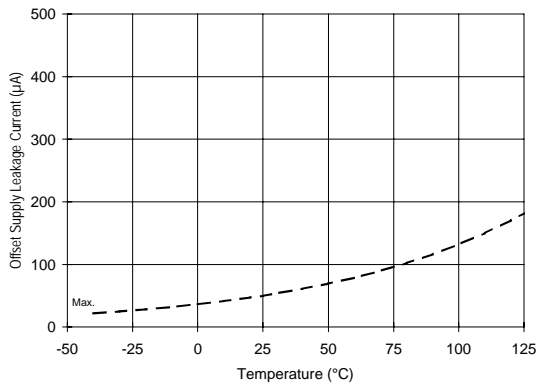


Figure 20A. Offset Supply Current vs. Temperature

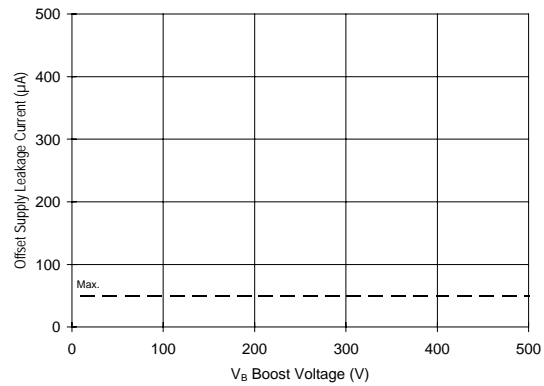


Figure 20B. Offset Supply Current vs. Voltage

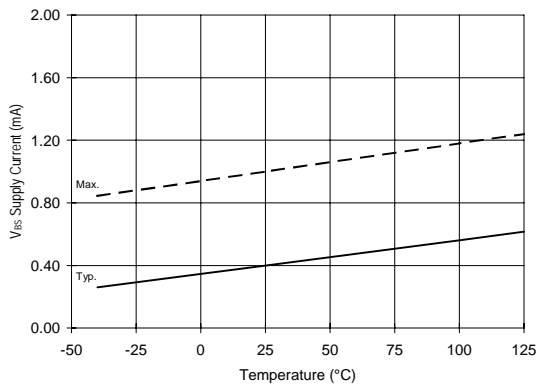


Figure 21A. V_{BS} Supply Current vs. Temperature

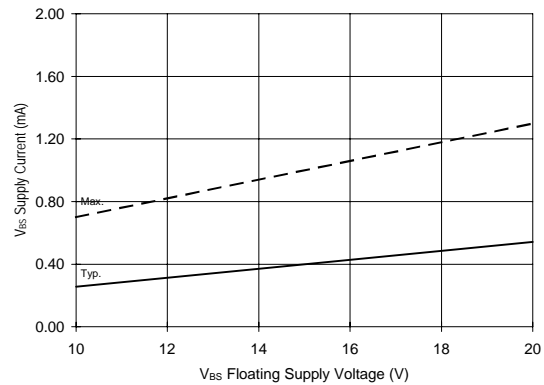


Figure 21B. V_{BS} Supply Current vs. Voltage

IR2125(S) & (PbF)

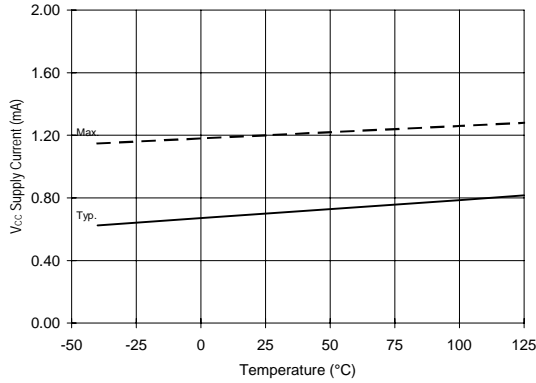


Figure 22A. V_{CC} Supply Current vs. Temperature

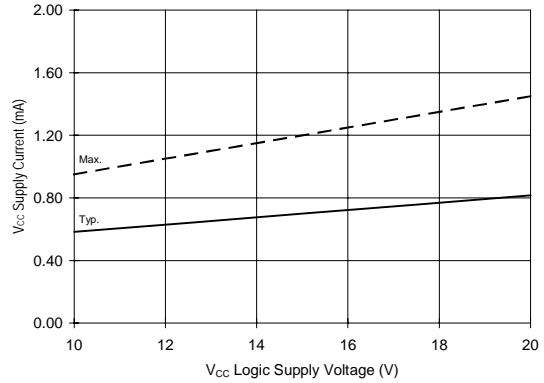


Figure 22B. V_{CC} Supply Current vs. Voltage

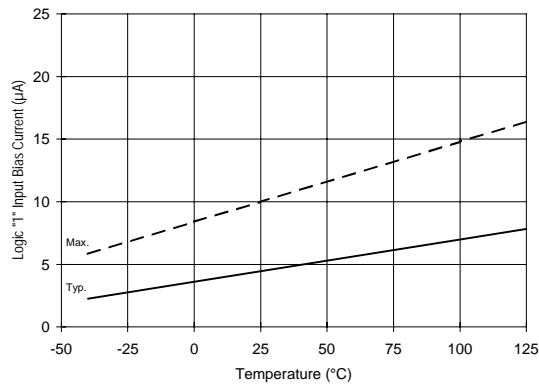


Figure 23A. Logic "1" Input Current vs. Temperature

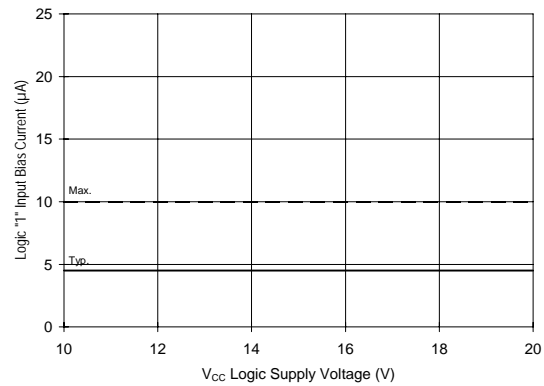


Figure 23B. Logic "1" Input Current vs. Voltage

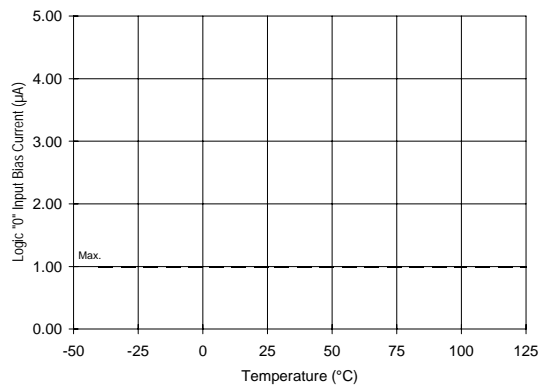


Figure 24A. Logic "0" Input Current vs. Temperature

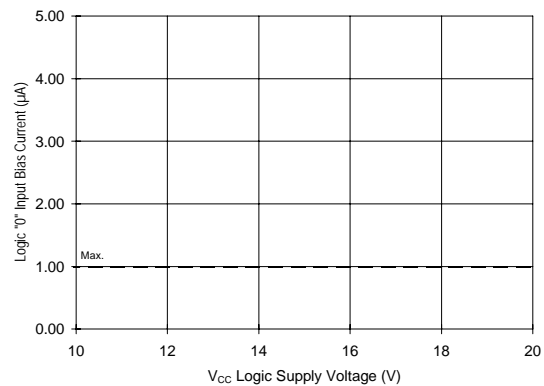


Figure 24B. Logic "0" Input Current vs. Voltage

IR2125(S) & (PbF)

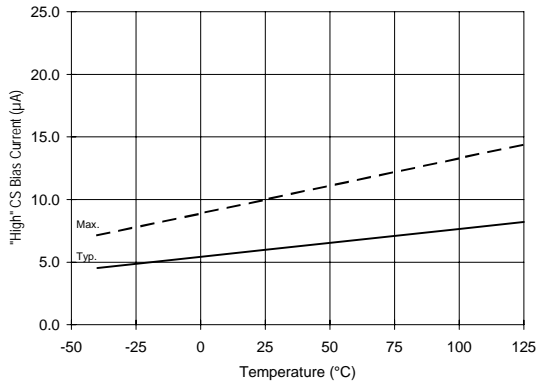


Figure 25A. “High” CS Bias Current vs. Temperature

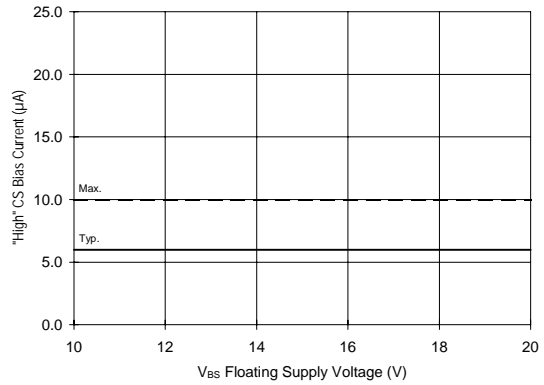


Figure 25B. “High” CS Bias Current vs. Voltage

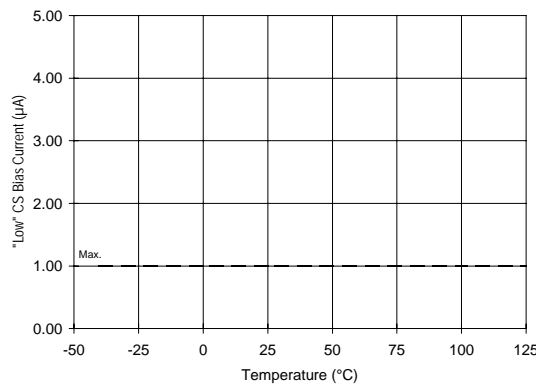


Figure 26A. “Low” CS Bias Current vs. Temperature

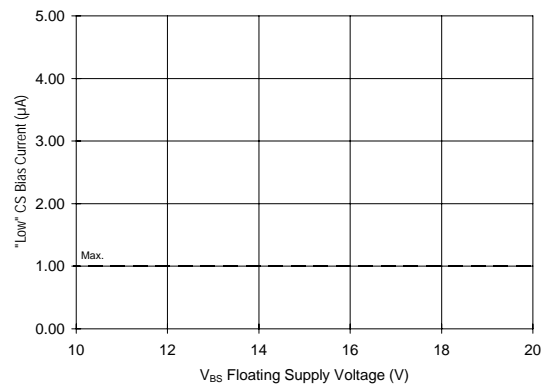


Figure 26B. “Low” CS Bias Current vs. Voltage

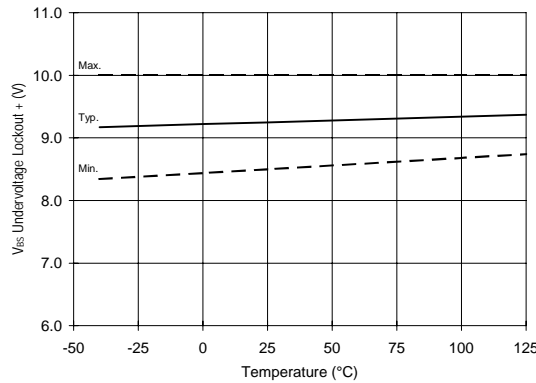


Figure 27. V_{BS} Undervoltage Lockout (+) vs. Temperature

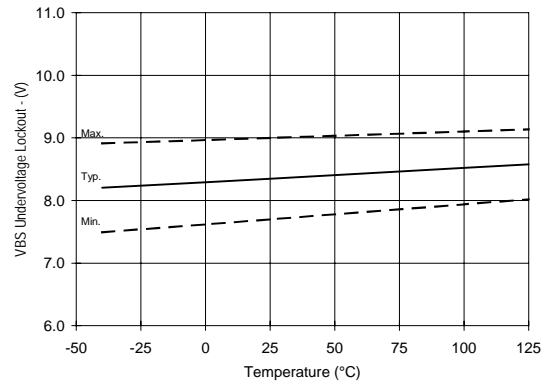


Figure 28. V_{BS} Undervoltage Lockout (-) vs. Temperature

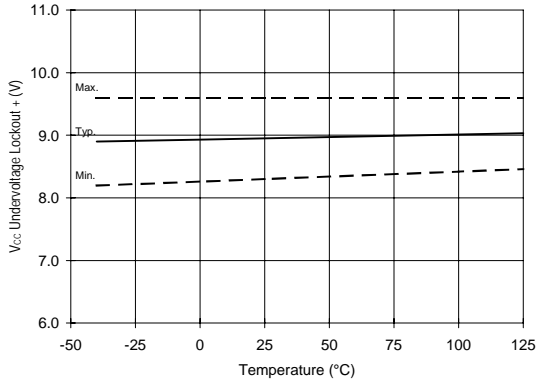


Figure 29. V_{CC} Undervoltage (+) vs. Temperature

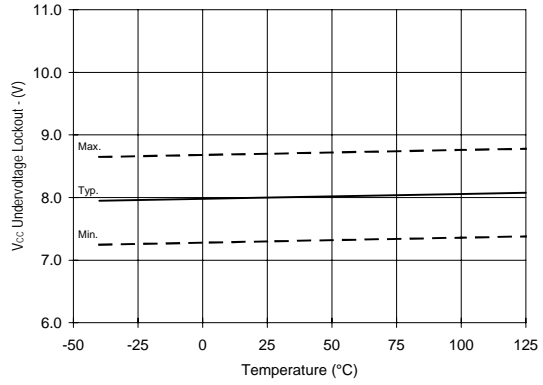


Figure 30. V_{CC} Undervoltage (-) vs. Temperature

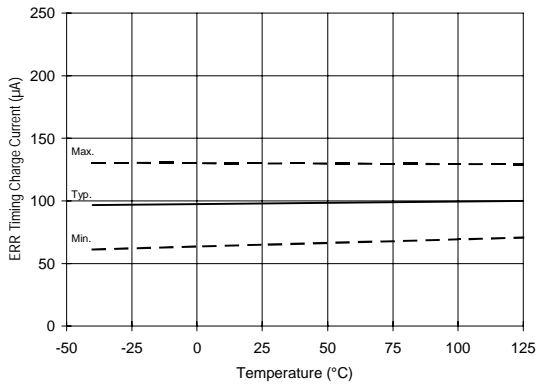


Figure 31A. ERR Timing Charge Current vs. Temperature

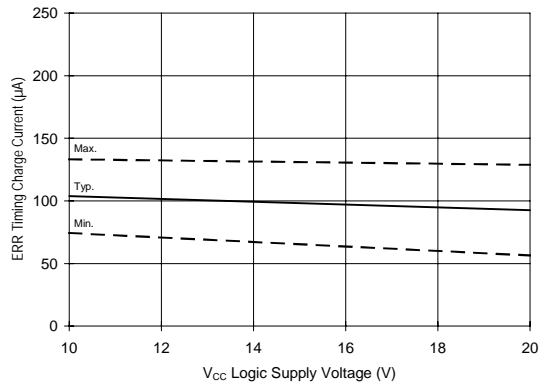


Figure 31B. ERR Timing Charge Current vs. Voltage

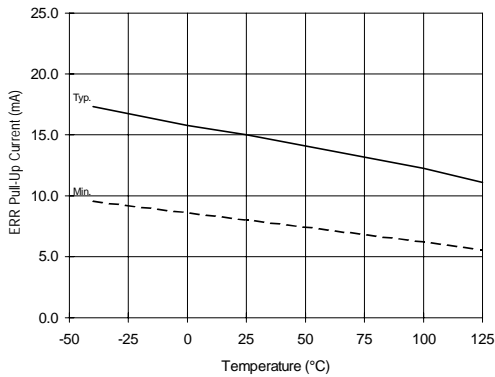


Figure 32A. ERR Pull-Up Current vs. Temperature

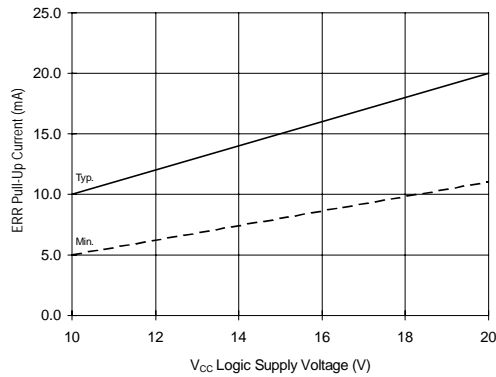


Figure 32B. ERR Pull-Up Current vs. Voltage

IR2125(S) & (PbF)

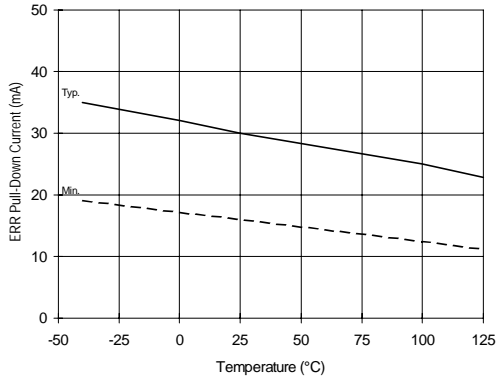


Figure 33A. ERR Pull-Down Current vs. Temperature

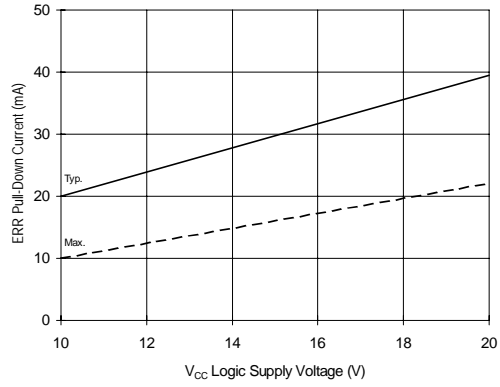


Figure 33B. ERR Pull-Down Current vs. Voltage

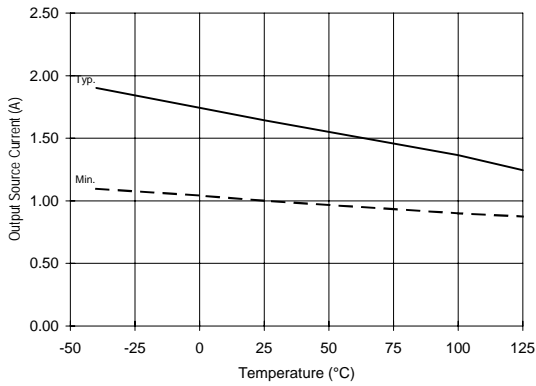


Figure 34A. Output Source Current vs. Temperature

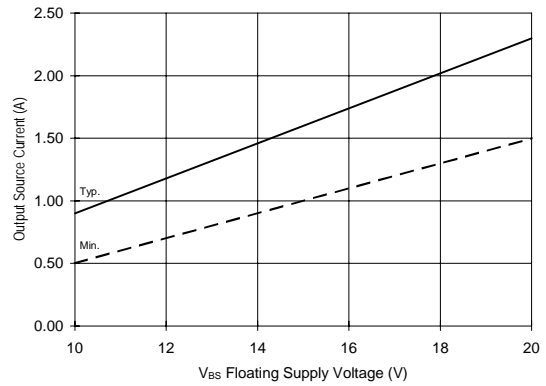


Figure 34B. Output Source Current vs. Voltage

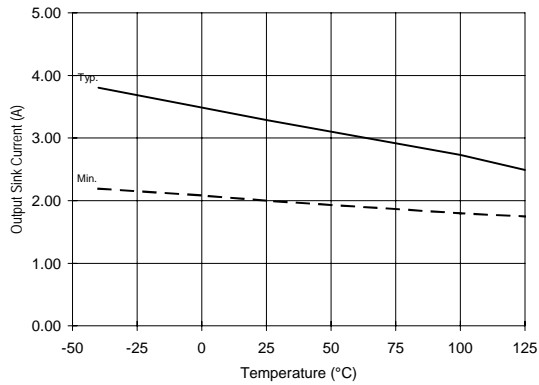


Figure 35A. Output Sink Current vs. Temperature

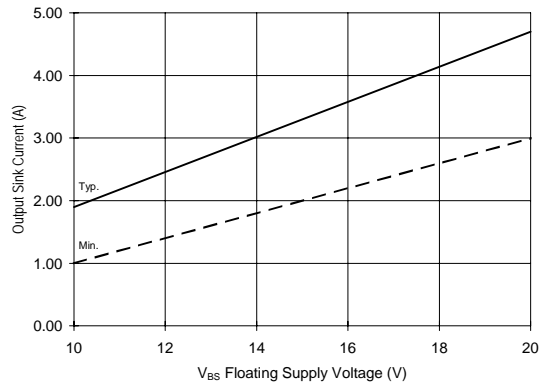


Figure 35B. Output Sink Current vs. Voltage

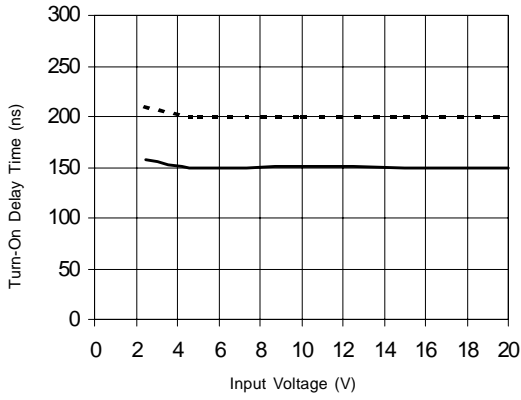


Figure 36A. Turn-On Time vs. Input Voltage

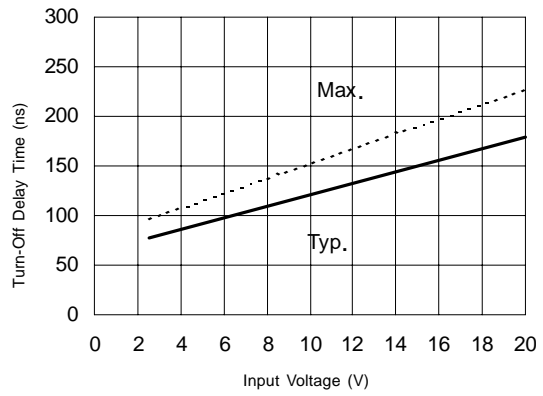


Figure 36B. Turn-Off Time vs. Input Voltage

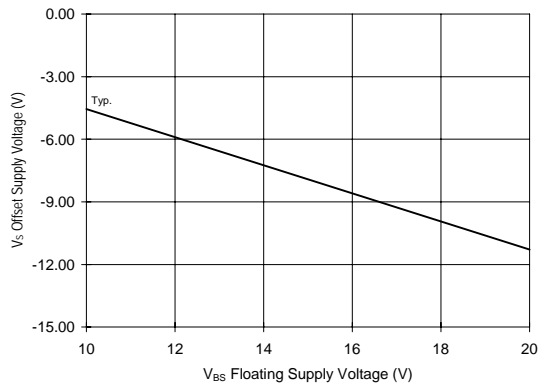
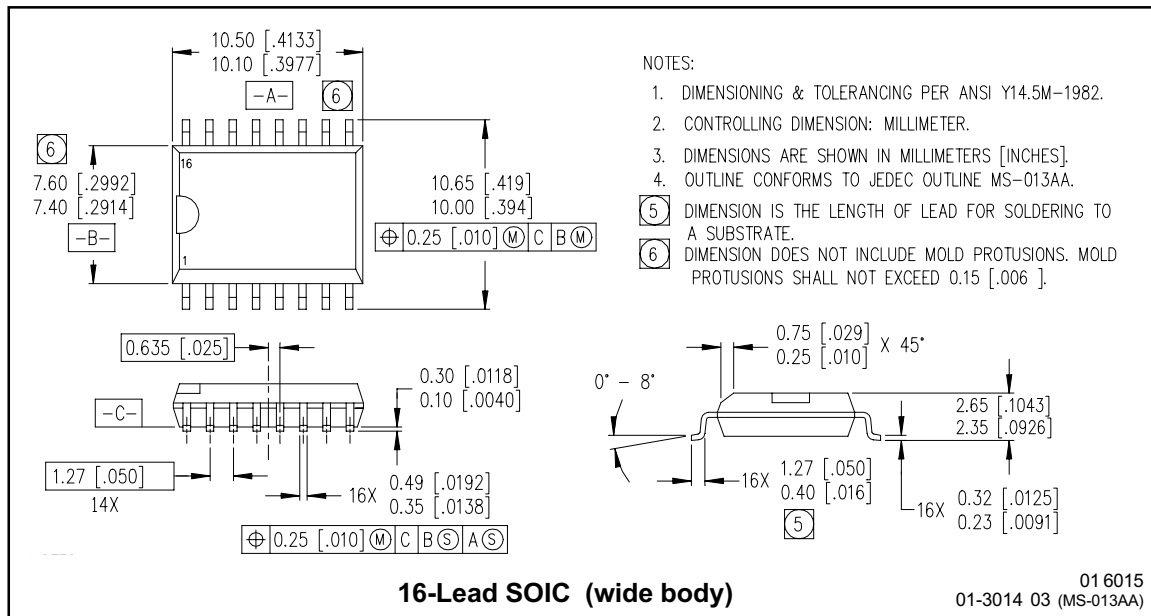
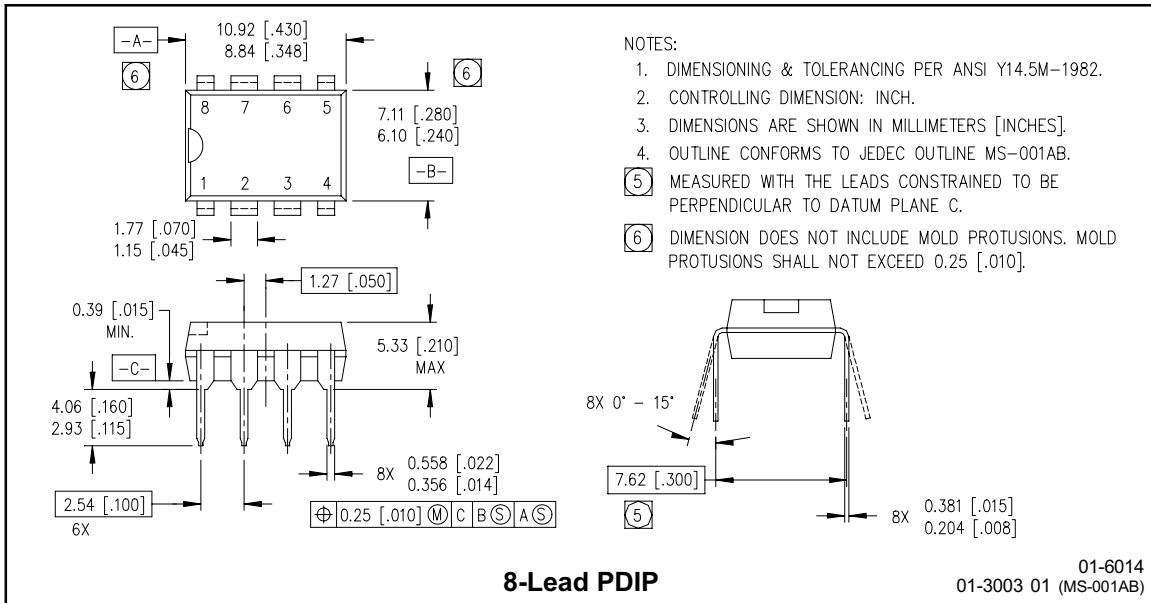


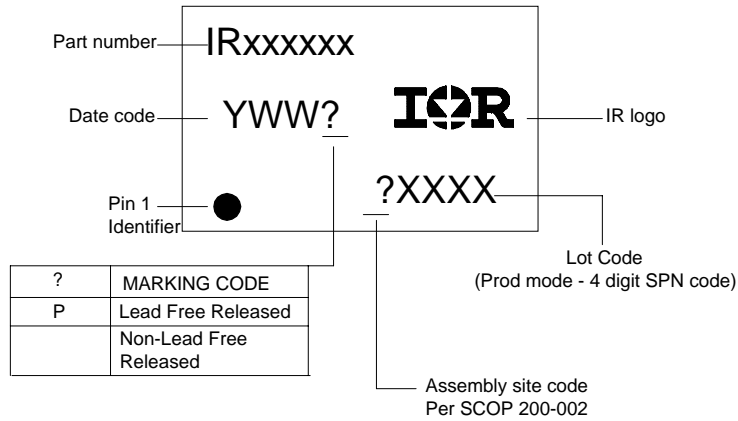
Figure 37. Maximum V_S Negative Offset vs. Supply Voltage

IR2125(S) & (PbF)

Case outlines



LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2125 order IR2125
 16-Lead SOIC IR2125S order IR2125S

Leadfree Part

8-Lead PDIP IR2125 order IR2125PbF
 16-Lead SOIC IR2125S order IR2125SPbF