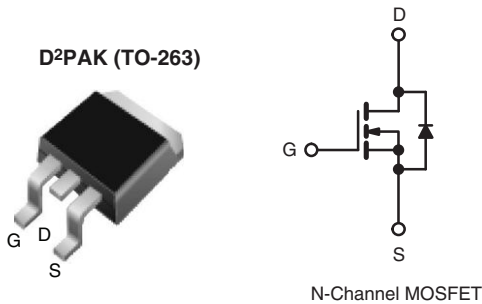


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.80
$Q_g$ (Max.) (nC)	14
$Q_{gs}$ (nC)	3.0
$Q_{gd}$ (nC)	7.9
Configuration	Single



### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Simple Drive Requirements
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF620S-GE3	SiHF620STRL-GE3 <sup>a</sup>	SiHF620STRR-GE3 <sup>a</sup>
Lead (Pb)-free	IRF620SPbF	IRF620STRLPbF <sup>a</sup>	IRF620STRRPbF <sup>a</sup>
	SiHF620S-E3	SiHF620STL-E3 <sup>a</sup>	SiHF620STR-E3 <sup>a</sup>

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		200	V
Gate-Source Voltage	$V_{GS}$		$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	5.2	A
		$T_C = 100\text{ }^\circ\text{C}$	3.3	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		18	W/ $^\circ\text{C}$
Linear Derating Factor			0.40	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.025	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		110	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$		5.2	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		5.0	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		50	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	$T_A = 25\text{ }^\circ\text{C}$		3.0	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt		5.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

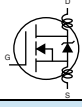
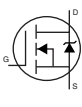
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 6.1\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 5.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 5.2\text{ A}$ ,  $dI/dt \leq 95\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.5	

**Note**

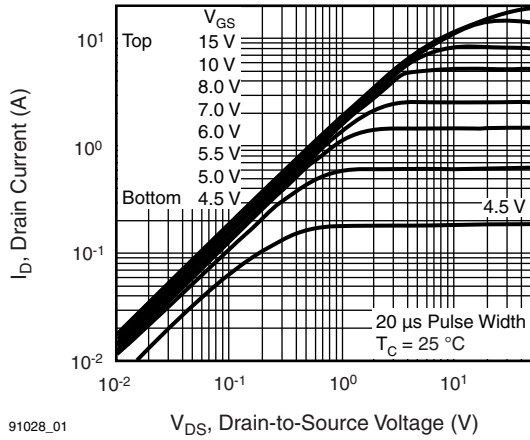
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX. UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		200	-	- V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.29	- V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0 V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100\text{ nA}$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$		-	-	25 $\mu\text{A}$	
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250 $\mu\text{A}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3.1\text{ A}^b$	-	-	0.80 $\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3.1\text{ A}^b$		1.5	-	- S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	260	-	
Output Capacitance	$C_{oss}$			-	100	-	pF
Reverse Transfer Capacitance	$C_{rss}$			-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 4.8\text{ A}, V_{DS} = 160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	14	
Gate-Source Charge	$Q_{gs}$			-	-	3.0	nC
Gate-Drain Charge	$Q_{gd}$			-	-	7.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, I_D = 4.8\text{ A}, R_g = 18\text{ }\Omega, R_D = 20\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	7.2	-	
Rise Time	$t_r$			-	22	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	19	-	
Fall Time	$t_f$			-	13	-	
<b>Dynamic</b>							
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	
Internal Source Inductance	$L_S$			-	7.5	-	nH
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.2	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	18	A
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8 V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 4.8\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	150	300	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.91	1.8	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

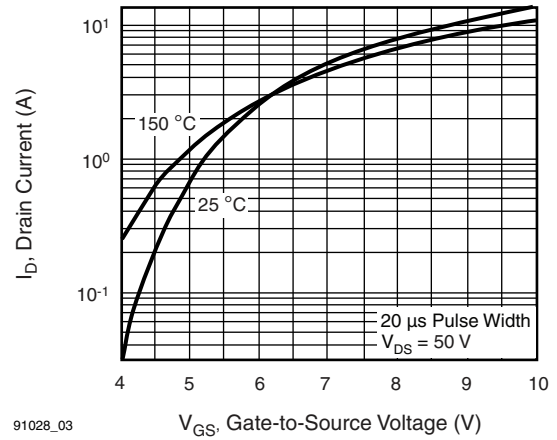
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



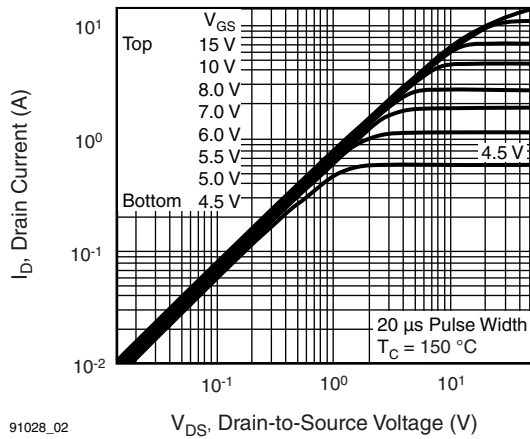
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**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



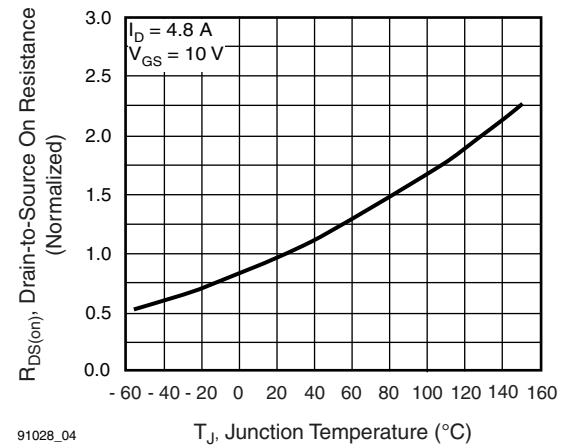
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**Fig. 3 - Typical Transfer Characteristics**



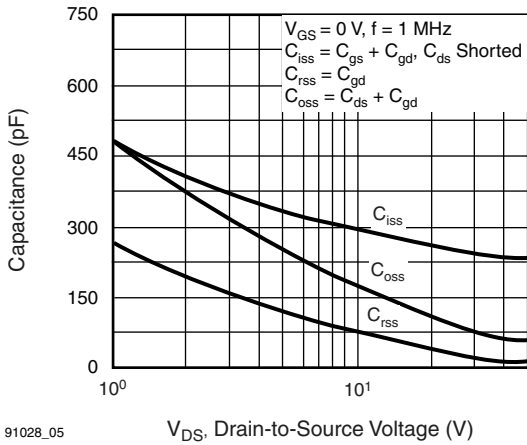
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**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



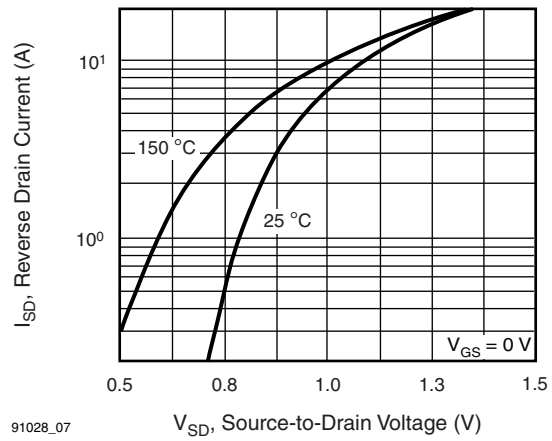
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**Fig. 4 - Normalized On-Resistance vs. Temperature**



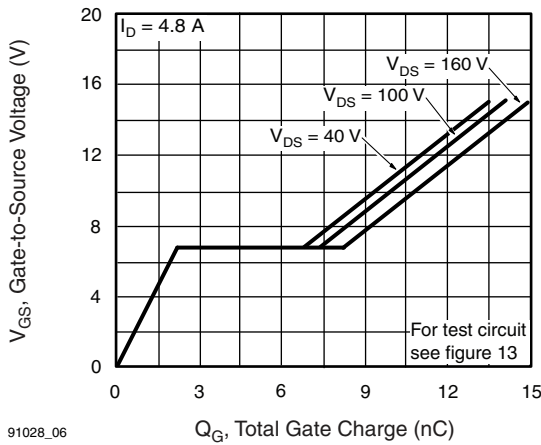
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**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



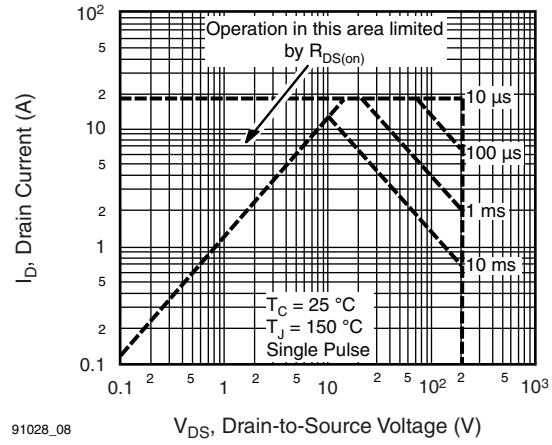
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



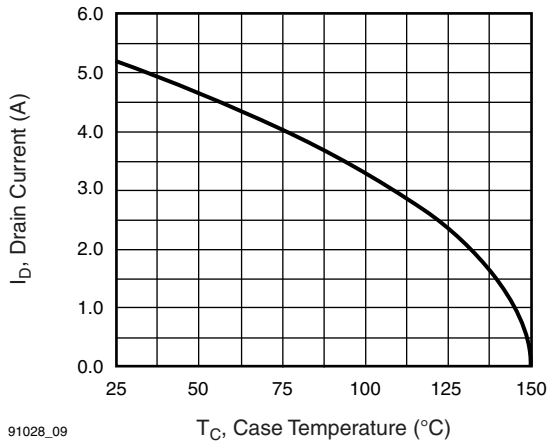
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**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

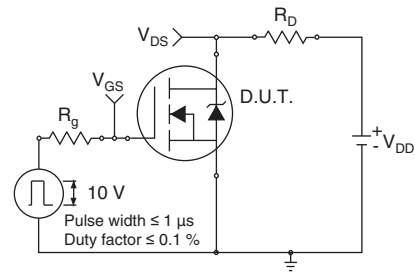


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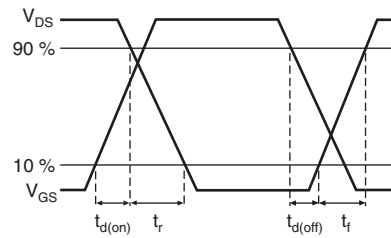
**Fig. 8 - Maximum Safe Operating Area**



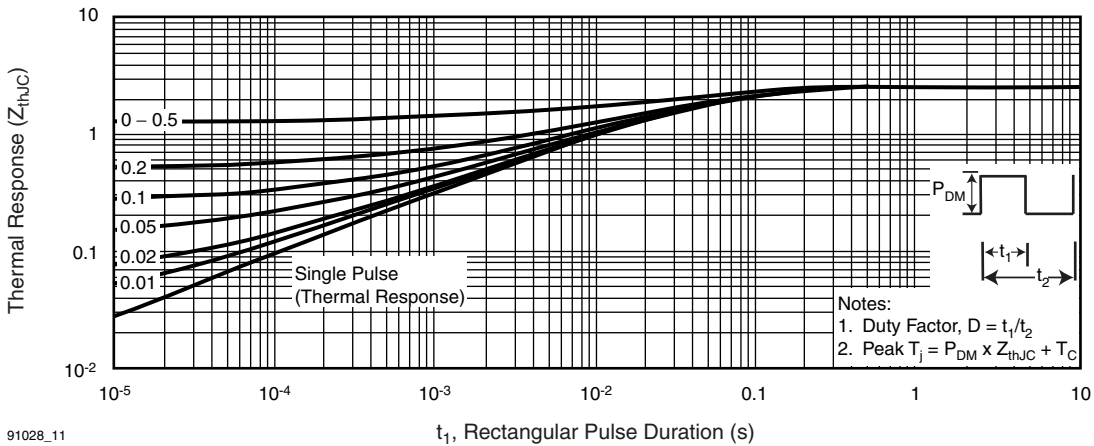
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

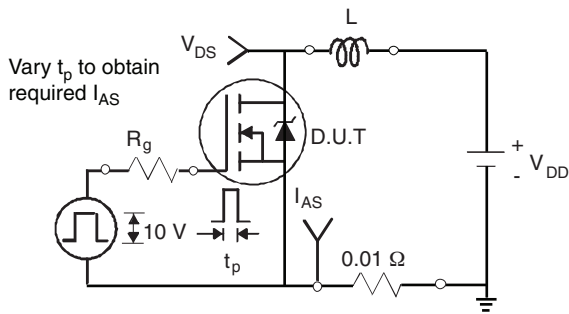


Fig. 12a - Unclamped Inductive Test Circuit

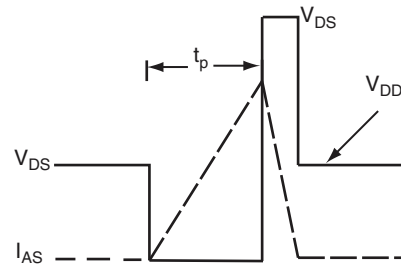


Fig. 12b - Unclamped Inductive Waveforms

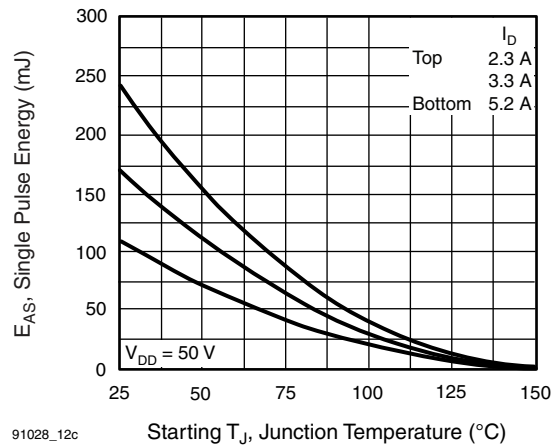


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

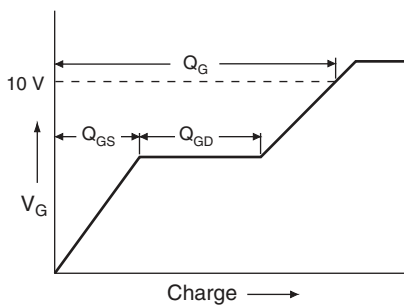


Fig. 13a - Basic Gate Charge Waveform

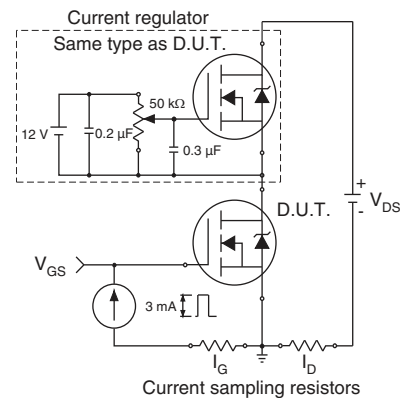
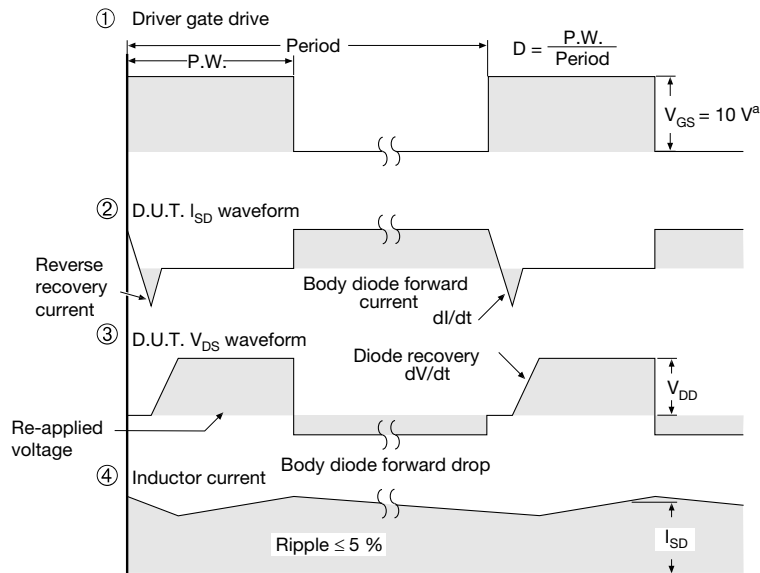
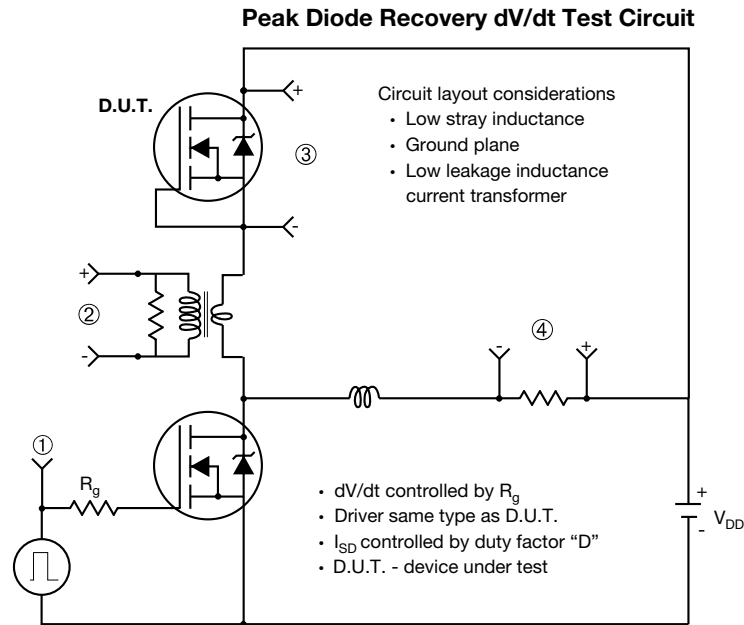


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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