

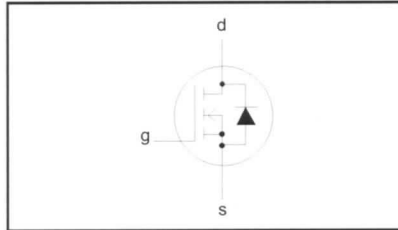
N-channel TrenchMOS transistor

IRF630, IRF630S

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 200\text{ V}$
$I_D = 9\text{ A}$
$R_{DS(ON)} \leq 400\text{ m}\Omega$

GENERAL DESCRIPTION

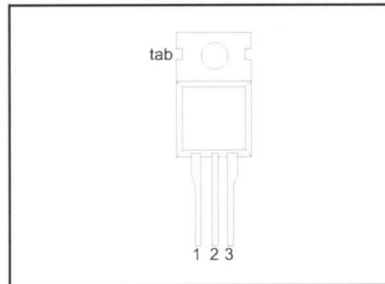
N-channel, enhancement mode field-effect power transistor using **Trench** technology, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The IRF630 is supplied in the SOT78 (TO220AB) conventional leaded package
The IRF630S is supplied in the SOT404 (D²PAK) surface mounting package

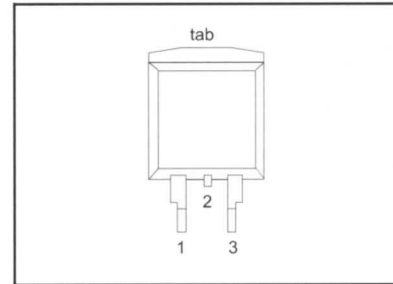
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

SOT78 (TO220AB)



SOT404 (D²PAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	200	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	9	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	6.3	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	36	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	88	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 5$ A; $t_p = 380$ μ s; T_j prior to avalanche = 25° C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig;14	-	250	mJ
I_{AS}	Peak non-repetitive avalanche current		-	9	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ$ C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ$ C	200 178	-	-	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ$ C $T_j = -55^\circ$ C	2 1	3	4	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 5.4$ A $T_j = 175^\circ$ C	-	300	400	m Ω Ω
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 5.4$ A	3.8	9	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V $V_{DS} = 160$ V; $V_{GS} = 0$ V; $T_j = 175^\circ$ C	-	0.05	10	μ A μ A
$Q_{g(tot)}$	Total gate charge	$I_D = 5.9$ A; $V_{DD} = 160$ V; $V_{GS} = 10$ V	-	-	39	nC
Q_{gs}	Gate-source charge		-	-	6.3	nC
Q_{gd}	Gate-drain (Miller) charge		-	-	21	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 100$ V; $R_D = 10$ Ω ;	-	8	-	ns
t_r	Turn-on rise time	$V_{GS} = 10$ V; $R_G = 5.6$ Ω	-	19	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	25	-	ns
t_f	Turn-off fall time		-	15	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	959	-	pF
C_{oss}	Output capacitance		-	93	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	9	A
I_{SM}	Pulsed source current (body diode)		-	-	36	A
V_{SD}	Diode forward voltage	$I_F = 9\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
t_{rr}	Reverse recovery time	$I_F = 9\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	92	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	-	0.5	-	μC