

IRFB13N50APbF

HEXFET® Power MOSFET

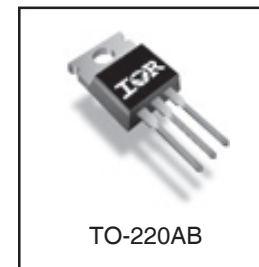
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Lead-Free

| V _{DSS} | R _{DS(on)} max | I _D |
|------------------|-------------------------|----------------|
| 500V | 0.450 Ω | 14A |

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|--------------|-------|
| I _D @ T _C = 25°C | Continuous Drain Current, V _{GS} @ 10V | 14 | A |
| I _D @ T _C = 100°C | Continuous Drain Current, V _{GS} @ 10V | 9.1 | |
| I _{DM} | Pulsed Drain Current ① | 56 | |
| P _D @ T _C = 25°C | Power Dissipation | 250 | W |
| | Linear Derating Factor | 2.0 | W/°C |
| V _{GS} | Gate-to-Source Voltage | ± 30 | V |
| dv/dt | Peak Diode Recovery dv/dt ③ | 9.2 | V/ns |
| T _J T _{STG} | Operating Junction and Storage Temperature Range | -55 to + 150 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10 | |

Avalanche Characteristics

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|--------------------------------|------|------|-------|
| E _{AS} | Single Pulse Avalanche Energy② | — | 560 | mJ |
| I _{AR} | Avalanche Current① | — | 14 | A |
| E _{AR} | Repetitive Avalanche Energy① | — | 25 | mJ |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|------------------|-------------------------------------|------|------|-------|
| R _{θJC} | Junction-to-Case | — | 0.50 | °C/W |
| R _{θCS} | Case-to-Sink, Flat, Greased Surface | 0.50 | — | |
| R _{θJA} | Junction-to-Ambient | — | 62 | |

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International
IR Rectifier

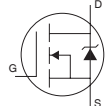
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 500 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.55 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.450 | Ω | $V_{GS} = 10V, I_D = 8.4A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 500V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 30V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -30V$ |

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------------|---------------------------------|------|------|------|-------|---|
| g_{fs} | Forward Transconductance | 8.1 | — | — | S | $V_{DS} = 50V, I_D = 8.4A$ |
| Q_g | Total Gate Charge | — | — | 81 | nC | $I_D = 14A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 20 | | $V_{DS} = 400V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 36 | | $V_{GS} = 10V, \text{See Fig. 6 and 13 } \textcircled{4}$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 15 | — | ns | $V_{DD} = 250V$ |
| t_r | Rise Time | — | 39 | — | | $I_D = 14A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 39 | — | | $R_G = 7.5\Omega$ |
| t_f | Fall Time | — | 31 | — | | $V_{GS} = 10V, \text{See Fig. 10 } \textcircled{4}$ |
| C_{iss} | Input Capacitance | — | 1910 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 290 | — | | $V_{DS} = 25V$ |
| C_{riss} | Reverse Transfer Capacitance | — | 11 | — | | $f = 1.0\text{MHz}, \text{See Fig. 5}$ |
| C_{oss} | Output Capacitance | — | 2730 | — | | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 82 | — | | $V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$ |
| $C_{oss \text{ eff.}}$ | Effective Output Capacitance | — | 160 | — | | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V \textcircled{5}$ |

Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------|---|---|------|------|---------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 14 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 56 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.5 | V | $T_J = 25^\circ\text{C}, I_S = 14A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 370 | 550 | ns | $T_J = 125^\circ\text{C}, I_F = 14A$ |
| Q_{rr} | Reverse Recovery Charge | — | 4.4 | 6.5 | μC | $di/dt = 100A/\mu s$ ④ |
| i_{RRM} | Reverse Recovery Current | — | 21 | 31 | A | |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 5.7\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 14A$, $dv/dt = 7.6V/ns$. (See Figure 12a)
- ③ $I_{SD} \leq 14A$, $di/dt \leq 250A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

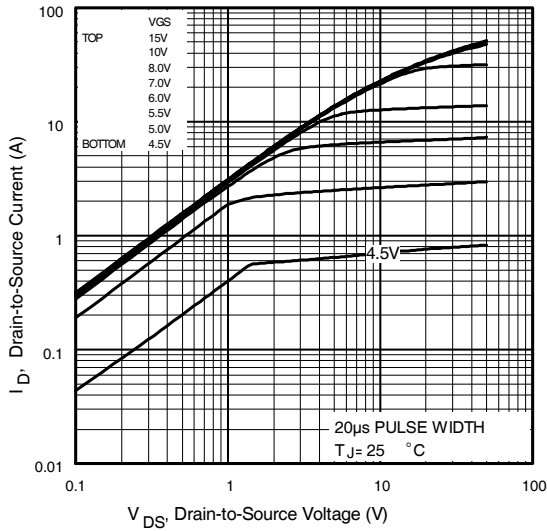


Fig 1. Typical Output Characteristics

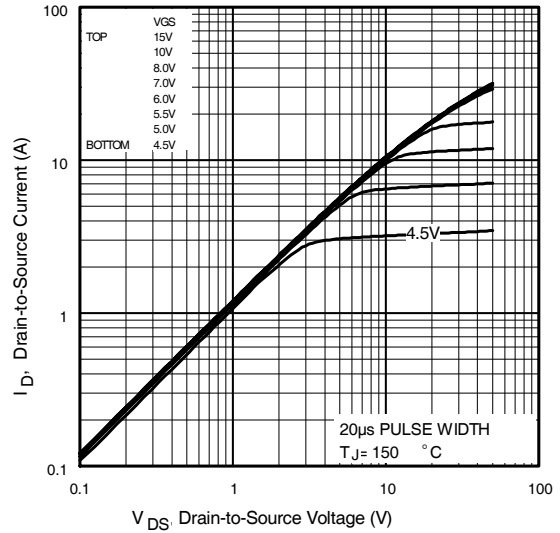


Fig 2. Typical Output Characteristics

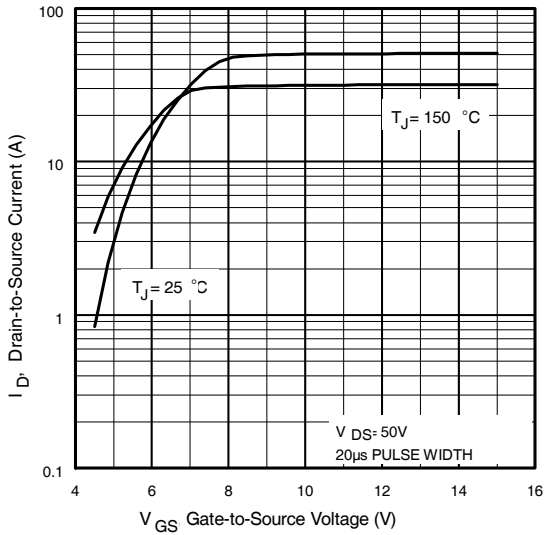


Fig 3. Typical Transfer Characteristics

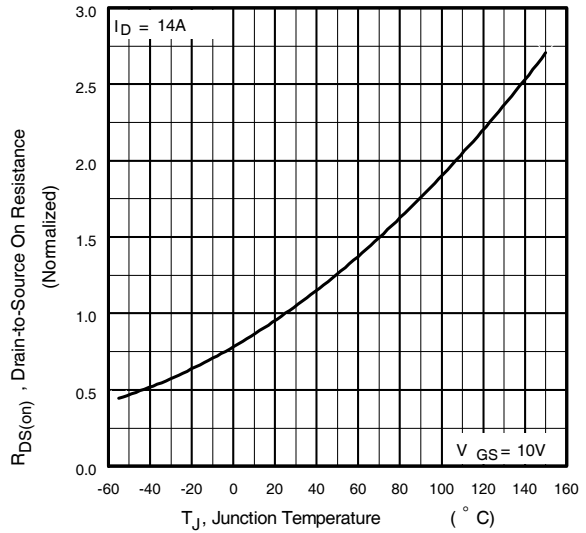


Fig 4. Normalized On-Resistance vs. Temperature

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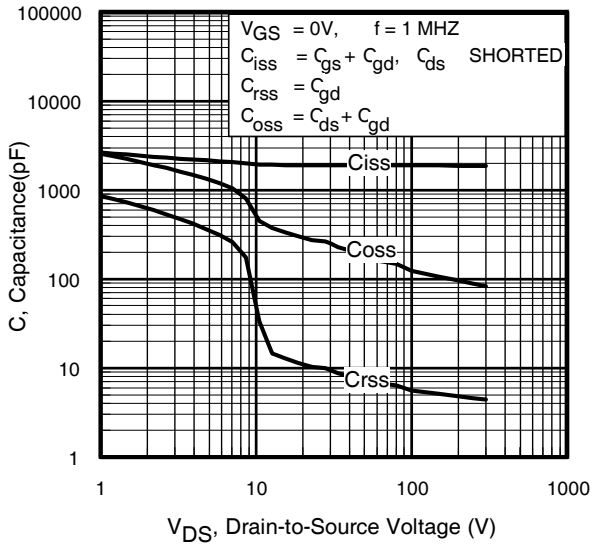


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

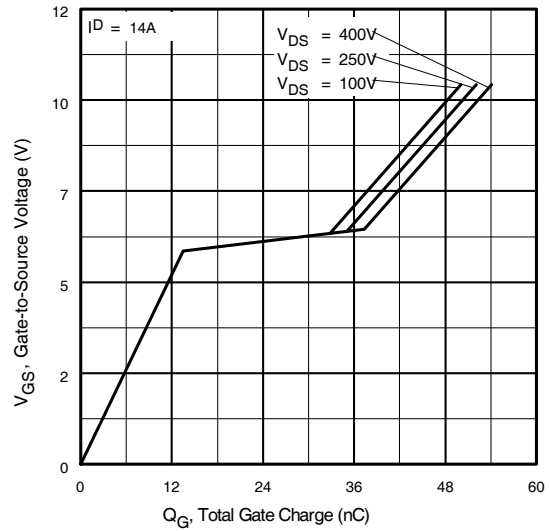


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

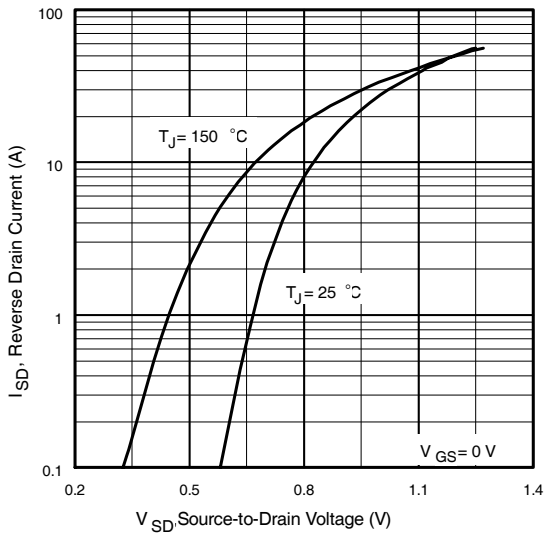


Fig 7. Typical Source-Drain Diode Forward Voltage

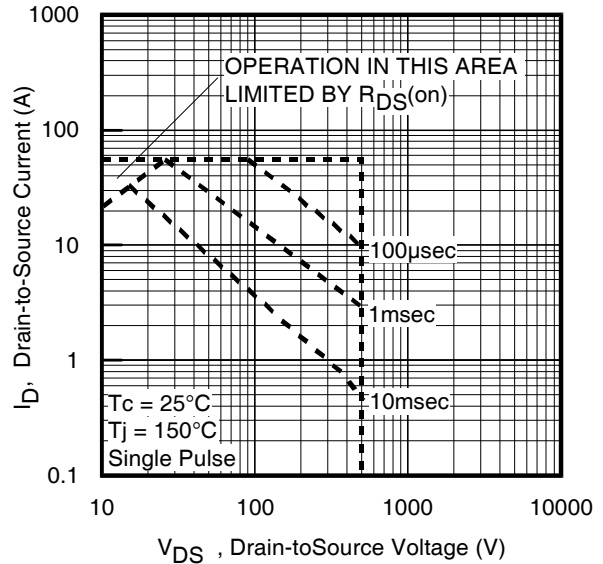


Fig 8. Maximum Safe Operating Area

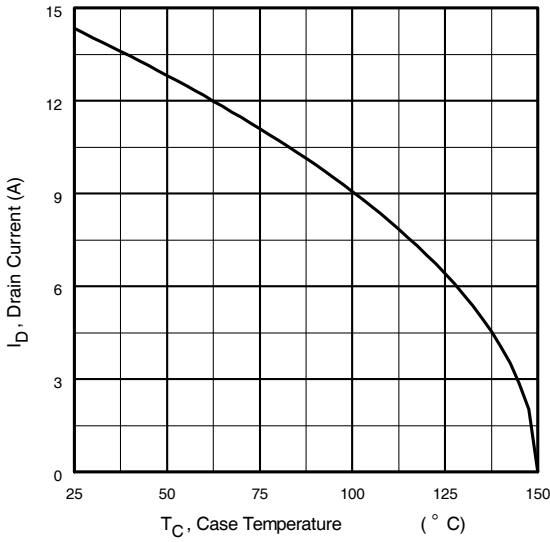


Fig 9. Maximum Drain Current vs. Case Temperature

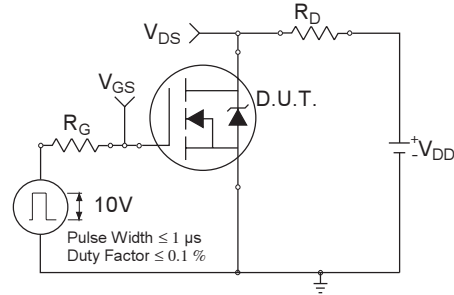


Fig 10a. Switching Time Test Circuit

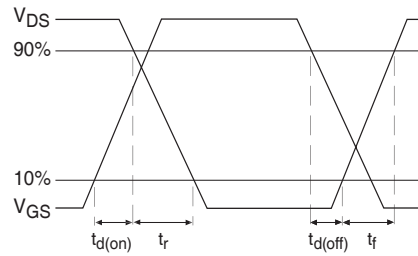


Fig 10b. Switching Time Waveforms

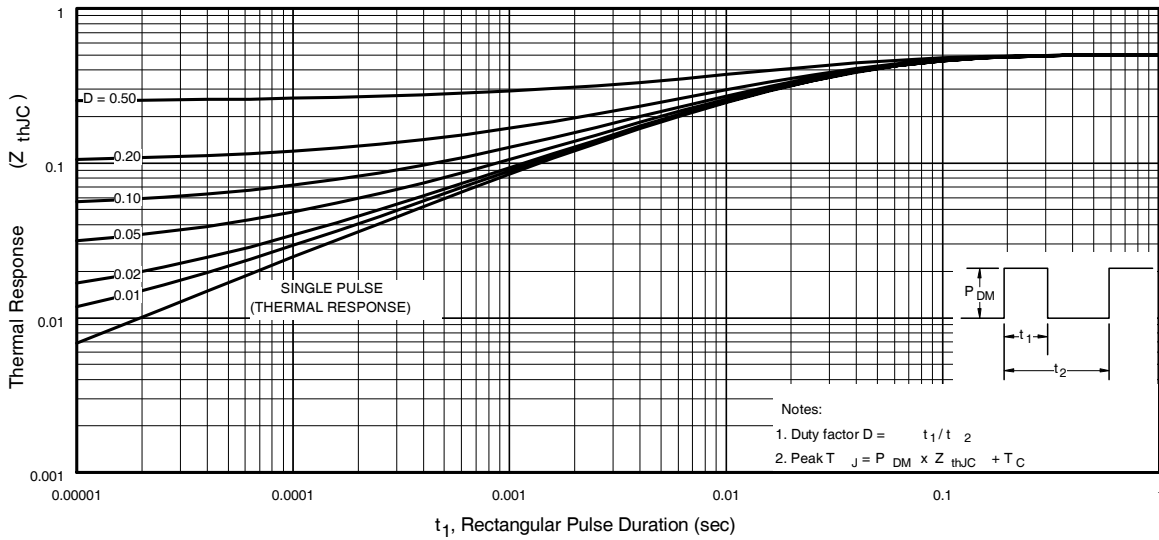


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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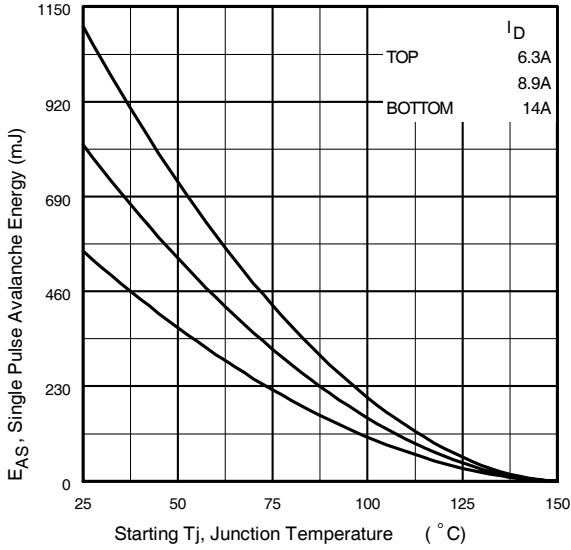


Fig 12a. Maximum Avalanche Energy vs. Drain Current

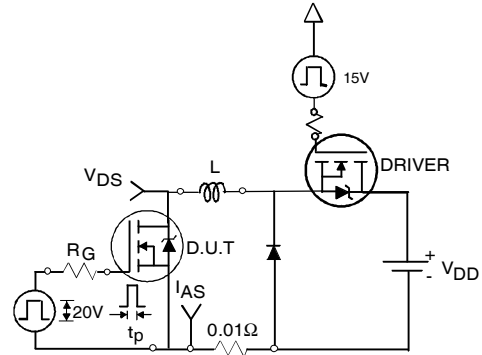


Fig 12c. Unclamped Inductive Test Circuit

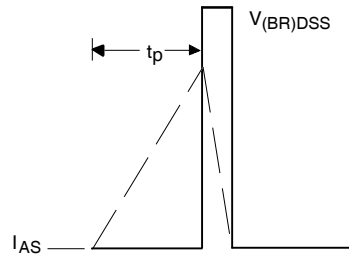


Fig 12d. Unclamped Inductive Waveforms

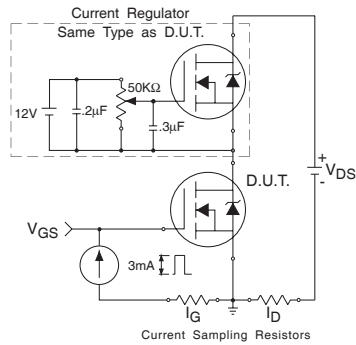


Fig 13a. Gate Charge Test Circuit

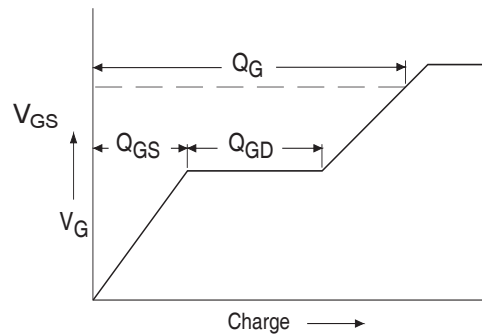
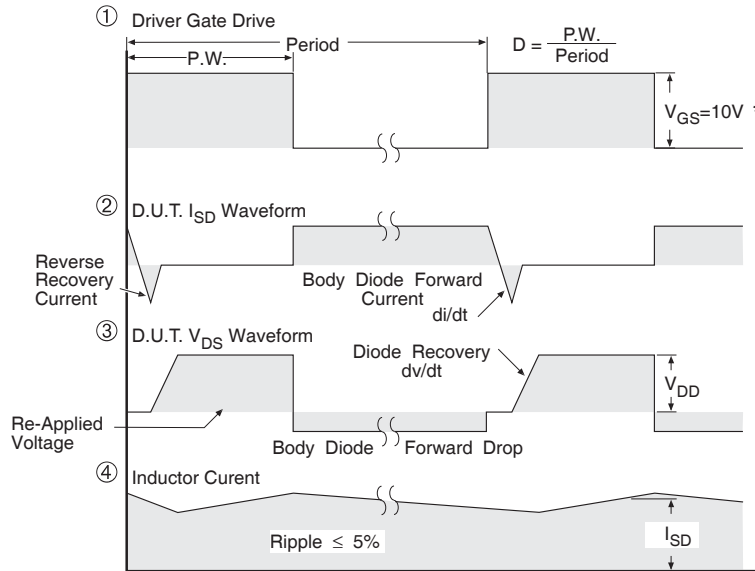
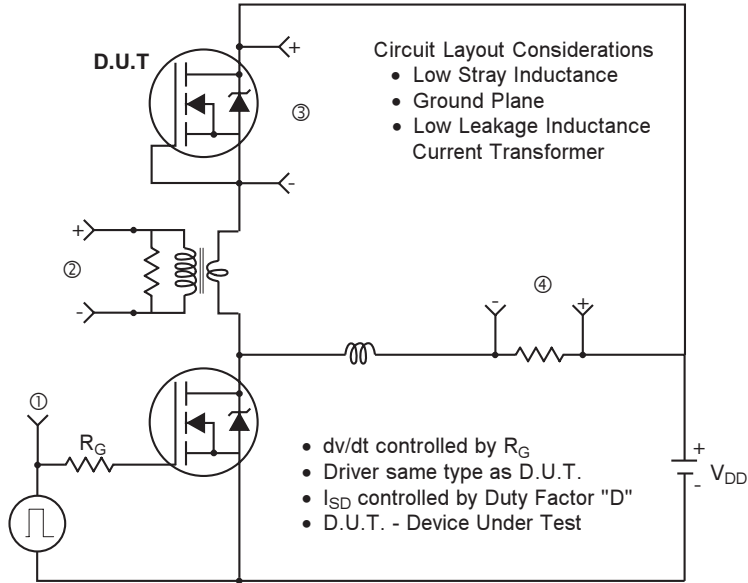


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

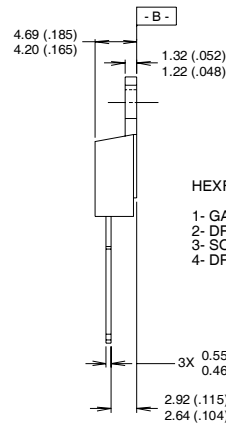
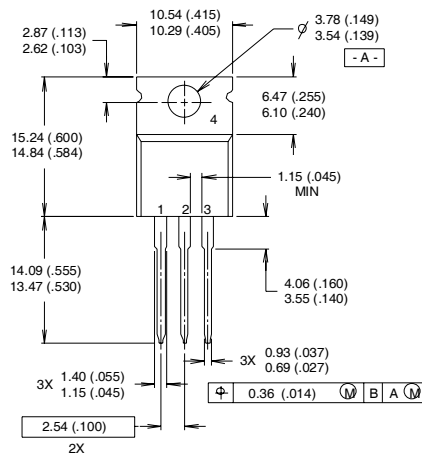
Fig 14. For N-Channel HEXFET[®] Power MOSFETs

IRFB13N50APbF



TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

| HEXFET | IGBTs, CoPACK |
|-----------|---------------|
| 1- GATE | 1- GATE |
| 2- DRAIN | 2- COLLECTOR |
| 3- SOURCE | 3- EMITTER |
| 4- DRAIN | 4- COLLECTOR |

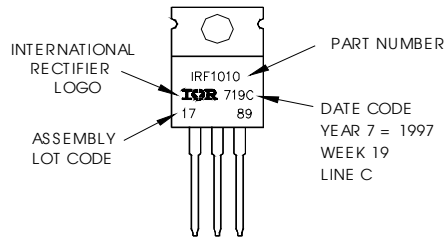
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
 position indicates "Lead-Free"



Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.



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 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.03/04

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