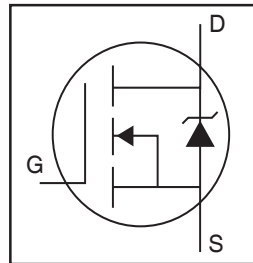


TO-247AC
Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits


Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}		100V
$R_{DS(on)}$	typ.	2.0mΩ
	max.	2.6mΩ
I_D (Silicon Limited)		290A ①
I_D (Package Limited)		195A

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	290①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	200	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	1120	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	520	W
	Linear Derating Factor	3.4	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	10	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	740	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.29	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧⑨	—	40	

Static @ T_J = 25°C (unless otherwise specified)

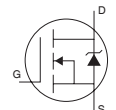
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to 25°C, I _D = 5mA ^②
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	2.0	2.6	mΩ	V _{GS} = 10V, I _D = 180A ^⑤
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Internal Gate Resistance	—	0.8	—	Ω	

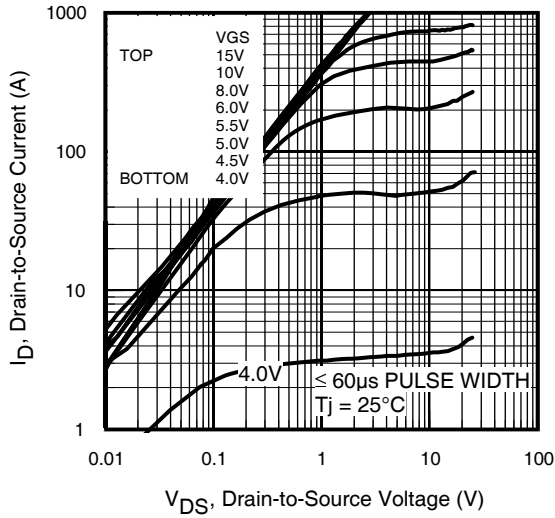
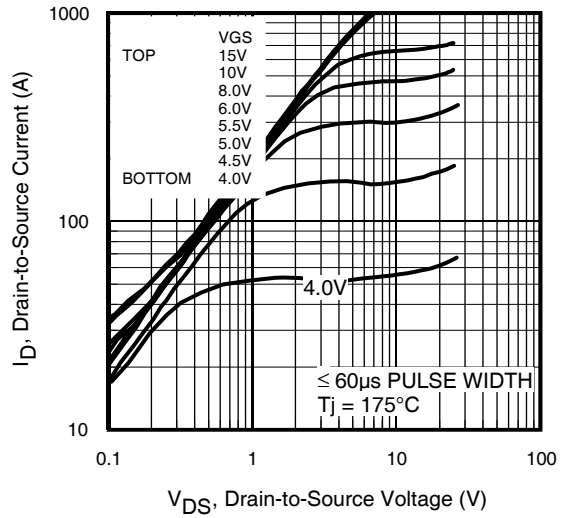
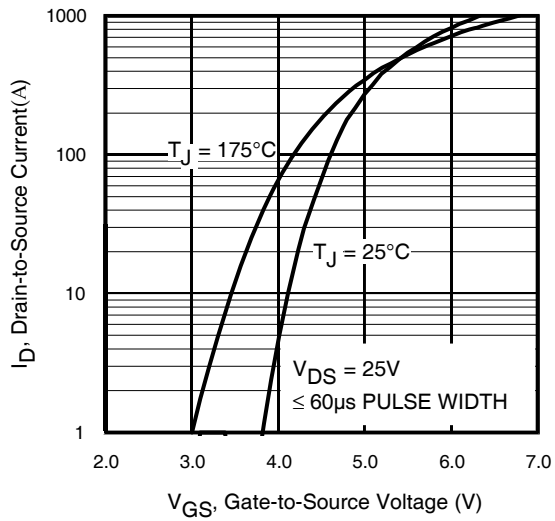
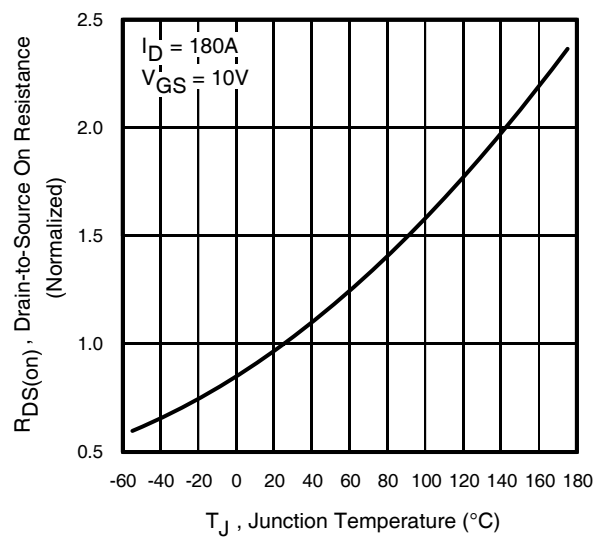
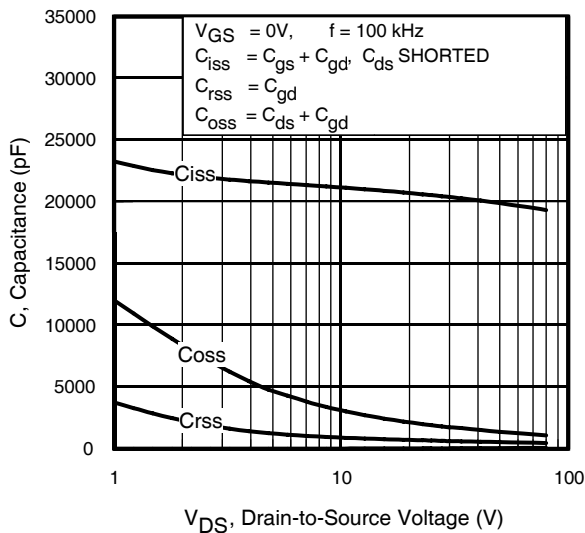
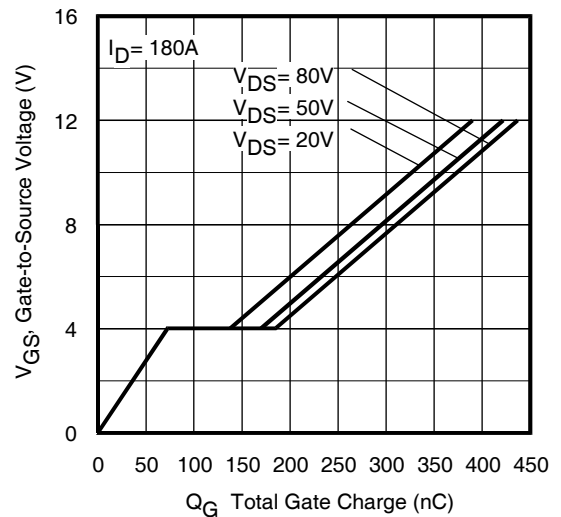
Dynamic @ T_J = 25°C (unless otherwise specified)

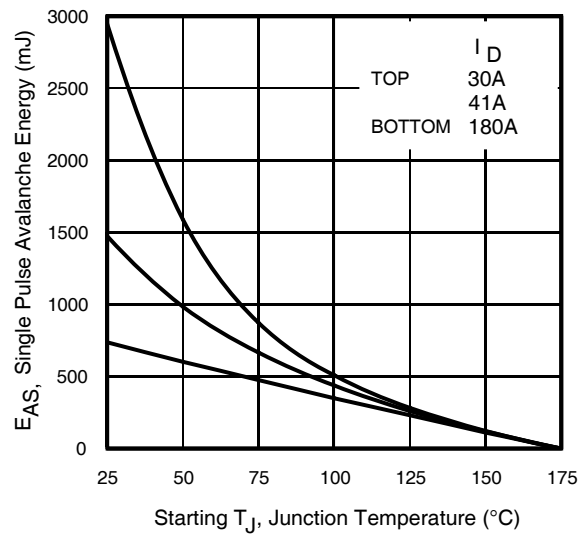
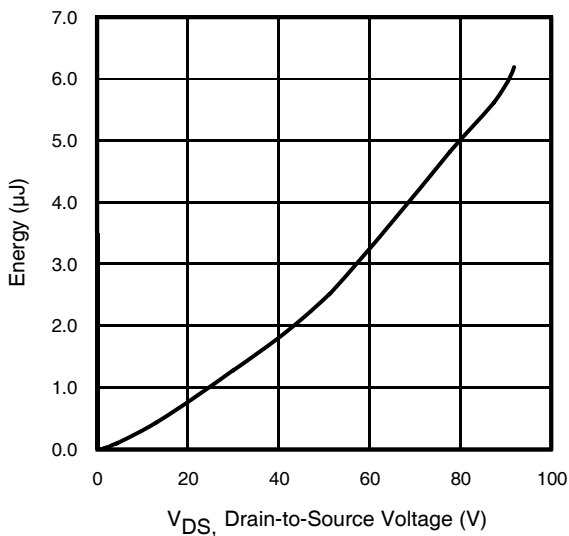
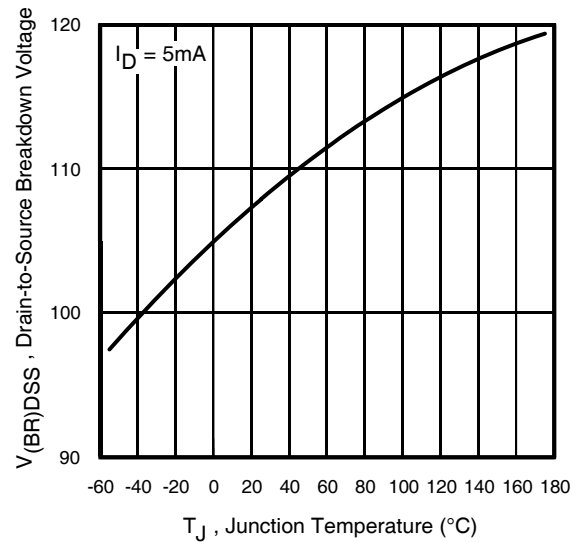
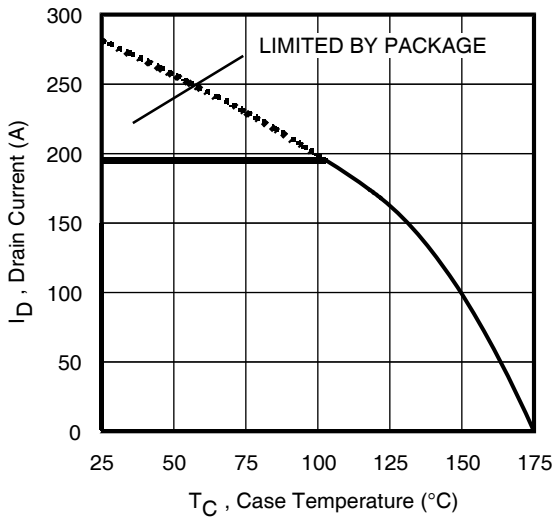
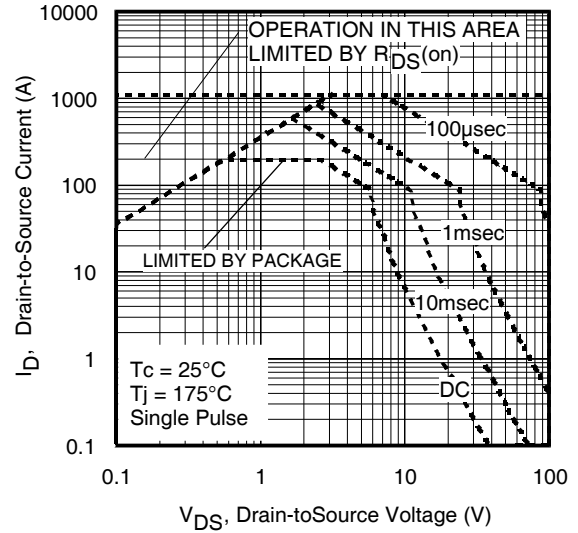
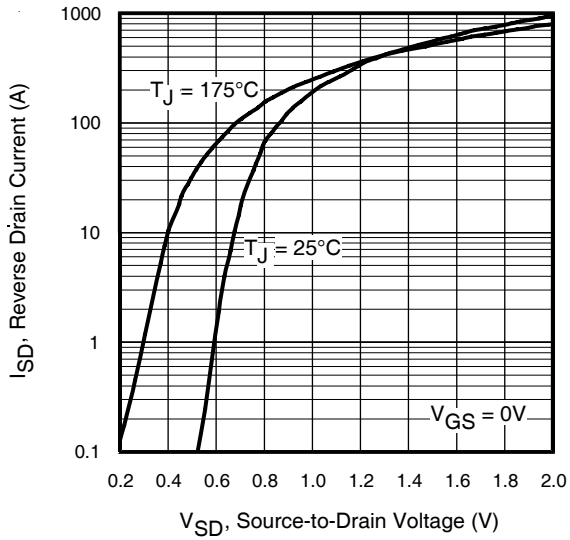
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	310	—	—	S	V _{DS} = 50V, I _D = 180A
Q _g	Total Gate Charge	—	360	540	nC	I _D = 180A
Q _{gs}	Gate-to-Source Charge	—	81	—		V _{DS} = 50V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	89	—		V _{GS} = 10V ^⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	270	—		I _D = 180A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	52	—	ns	V _{DD} = 65V
t _r	Rise Time	—	230	—		I _D = 180A
t _{d(off)}	Turn-Off Delay Time	—	160	—		R _G = 2.7Ω
t _f	Fall Time	—	260	—		V _{GS} = 10V ^⑤
C _{iss}	Input Capacitance	—	19860	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1360	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	540	—		f = 100 kHz, See Fig. 5
C _{oss eff. (ER)}	Effective Output Capacitance (Energy Related)	—	1550	—		V _{GS} = 0V, V _{DS} = 0V to 80V ^⑦ , See Fig. 11
C _{oss eff. (TR)}	Effective Output Capacitance (Time Related) ^⑧	—	900	—		V _{GS} = 0V, V _{DS} = 0V to 80V ^⑧

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	290 ^①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^②	—	—	1120	A	
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 180A, V _{GS} = 0V ^⑤
t _{rr}	Reverse Recovery Time	—	100	—	ns	T _J = 25°C V _R = 85V, T _J = 125°C I _F = 180A
Q _{rr}	Reverse Recovery Charge	—	370	—	nC	T _J = 25°C di/dt = 100A/μs ^⑤ T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	6.9	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				




Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



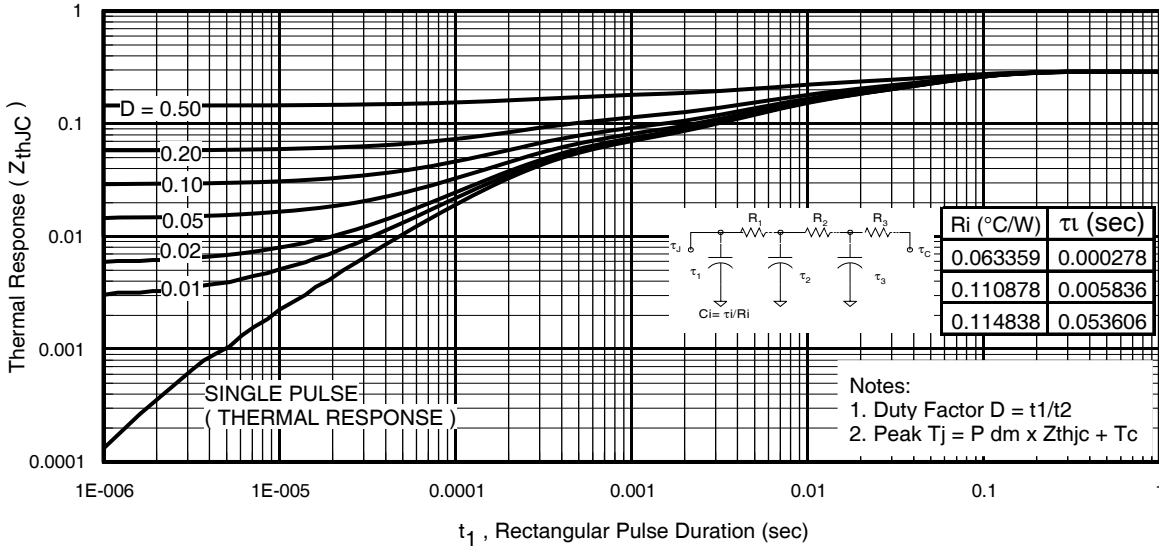


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

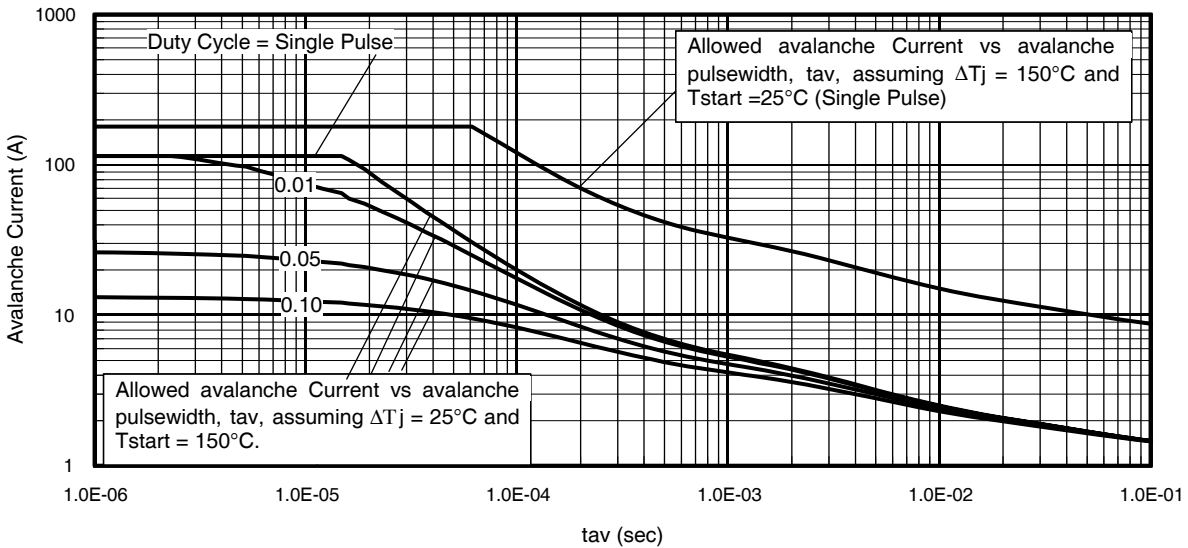
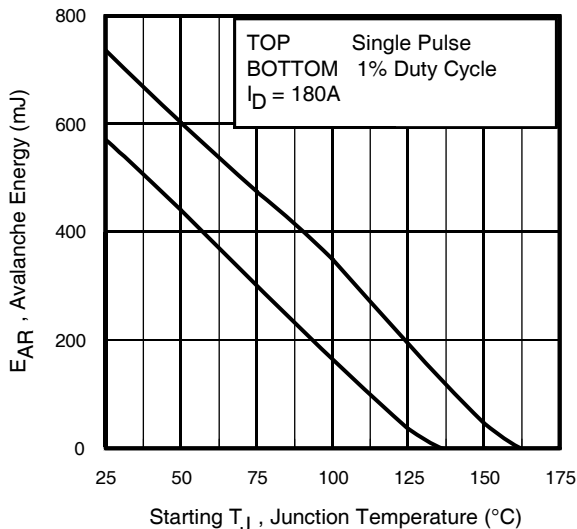


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^{\circ}C$ in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

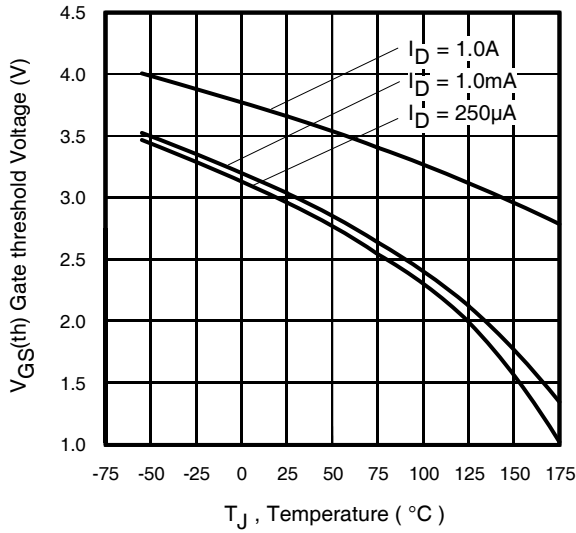


Fig 16. Threshold Voltage Vs. Temperature

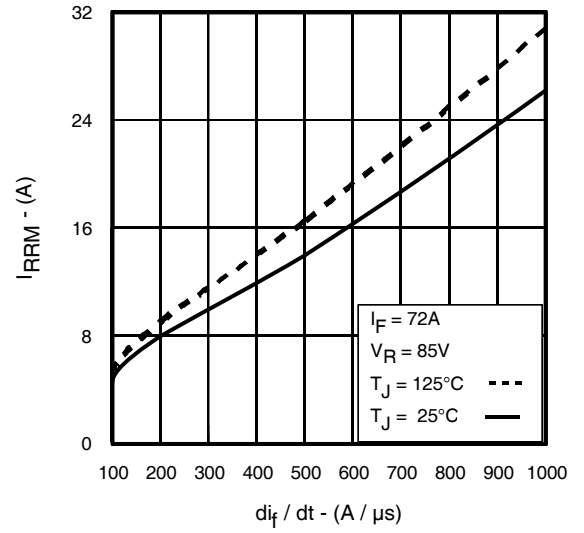


Fig. 17 - Typical Recovery Current vs. di_f/dt

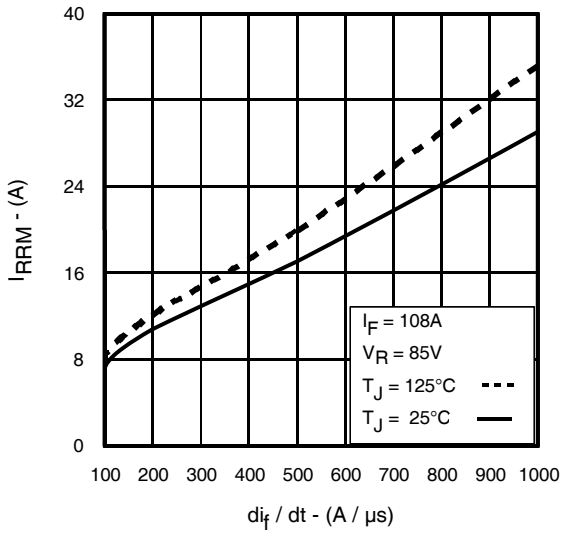


Fig. 18 - Typical Recovery Current vs. di_f/dt

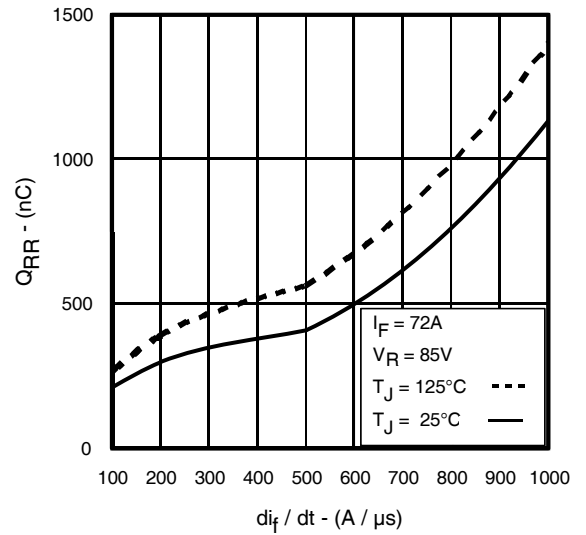


Fig. 19 - Typical Stored Charge vs. di_f/dt

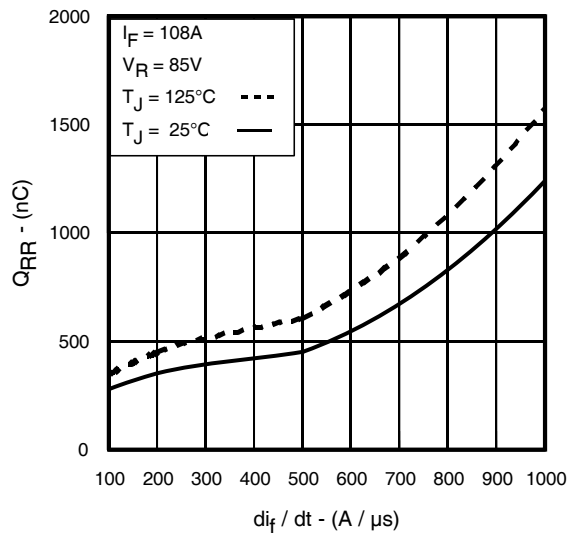
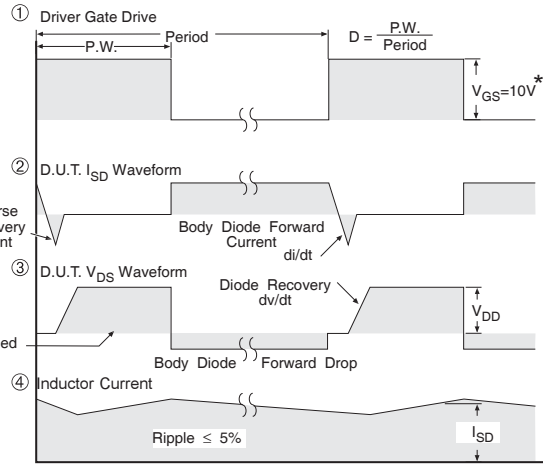
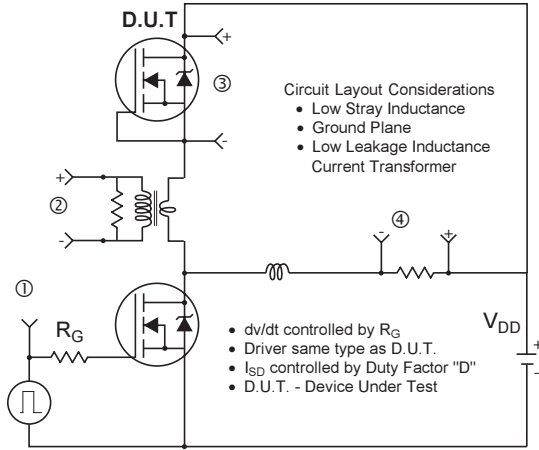


Fig. 20 - Typical Stored Charge vs. di_f/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

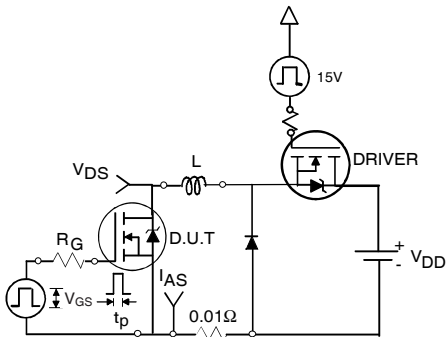


Fig 22a. Unclamped Inductive Test Circuit

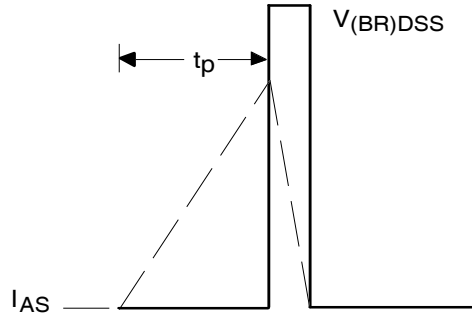


Fig 22b. Unclamped Inductive Waveforms

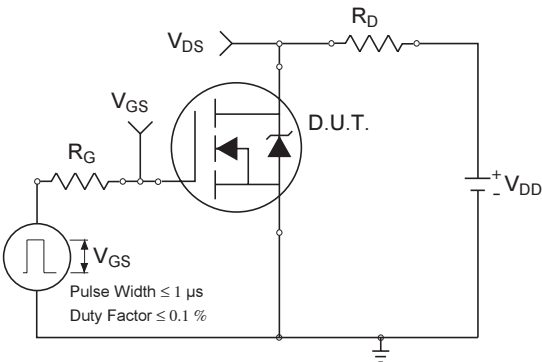


Fig 23a. Switching Time Test Circuit

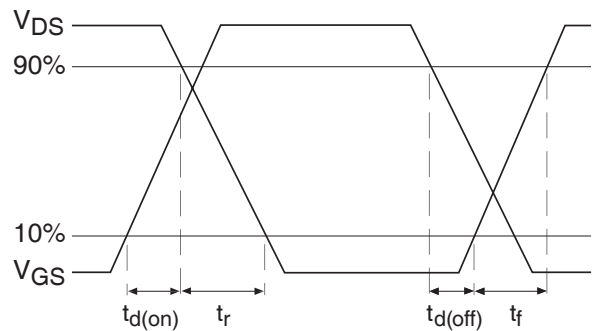


Fig 23b. Switching Time Waveforms

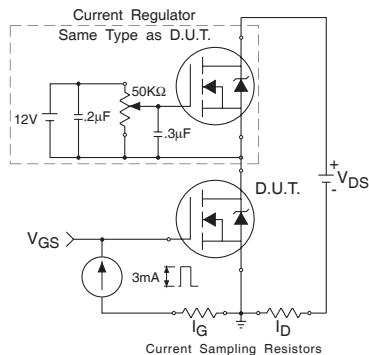


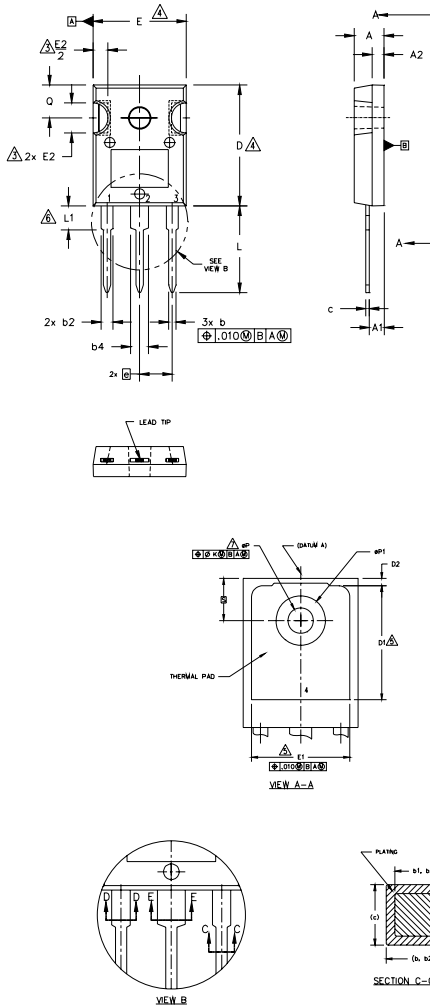
Fig 24a. Gate Charge Test Circuit



Fig 24b. Gate Charge Waveform

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

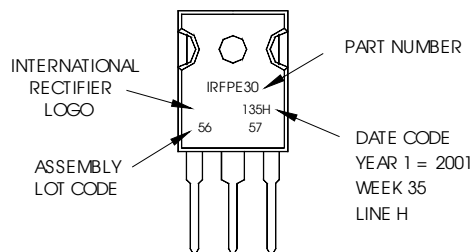
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC packages are not recommended for Surface Mount Application.