SMPS MOSFET

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	I_D
150V	0.18Ω	14A

Applications
- High frequency DC-DC converters

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

D-Pak
IRFR13N15D

I-Pak
IRFU13N15D

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	9.8	
I_{DM}	Pulsed Drain Current ①	56	
P_D @T_C = 25°C	Power Dissipation	86	W
	Linear Derating Factor	0.57	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input Active Clamp Forward Converter

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	V_{GS} = 10V, I_D = 8.3A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	5.0	—	—	S	V_{DS} = 50V, I_D = 8.3A
Q_g	Total Gate Charge	—	19	29	nC	I_D = 8.3A
Q_{gs}	Gate-to-Source Charge	—	5.5	8.2		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.4	14		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	V_{DD} = 75V
t_r	Rise Time	—	26	—		I_D = 8.3A
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		R_G = 11Ω
t_f	Fall Time	—	11	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	620	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	130	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	38	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	780	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	62	—		V_{GS} = 0V, V_{DS} = 120V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	110	—		V_{GS} = 0V, V_{DS} = 0V to 120V ⑤

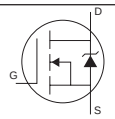
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	130	mJ
I_{AR}	Avalanche Current①	—	8.3	A
E_{AR}	Repetitive Avalanche Energy①	—	8.6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 8.3A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	110	—	ns	T_J = 25°C, I_F = 8.3A
Q_{rr}	Reverse RecoveryCharge	—	520	—	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

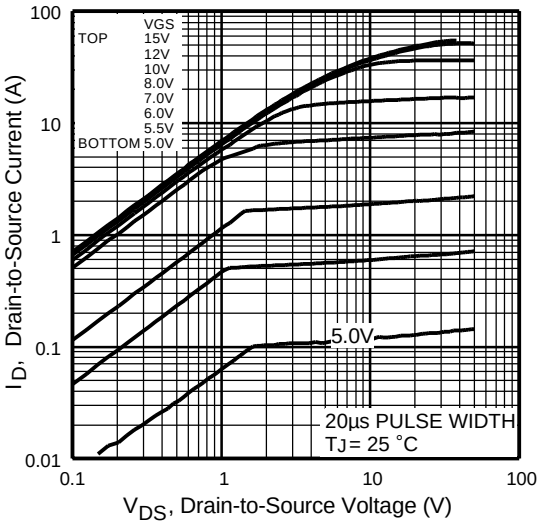


Fig 1. Typical Output Characteristics

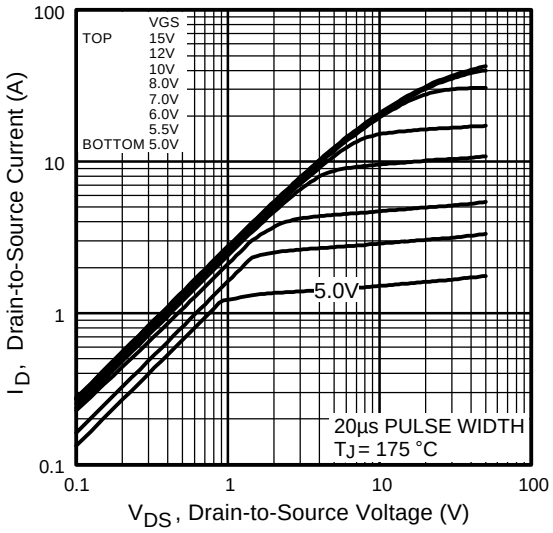


Fig 2. Typical Output Characteristics

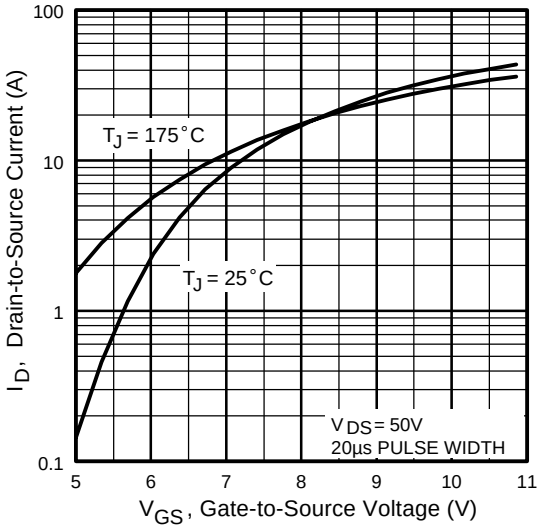


Fig 3. Typical Transfer Characteristics

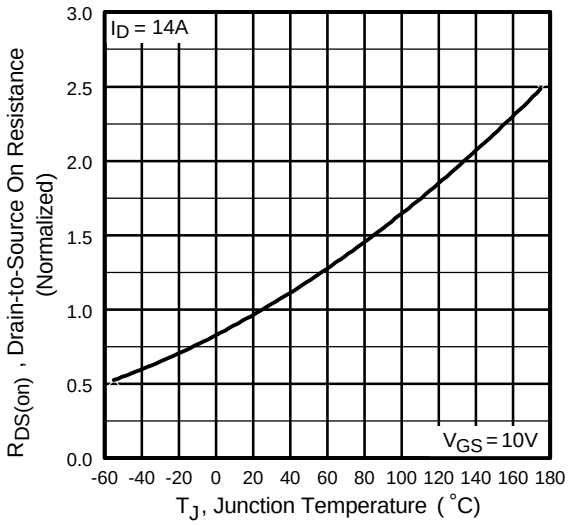


Fig 4. Normalized On-Resistance Vs. Temperature

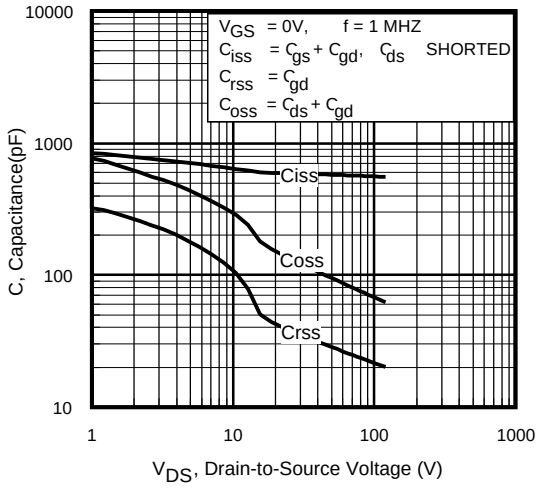


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

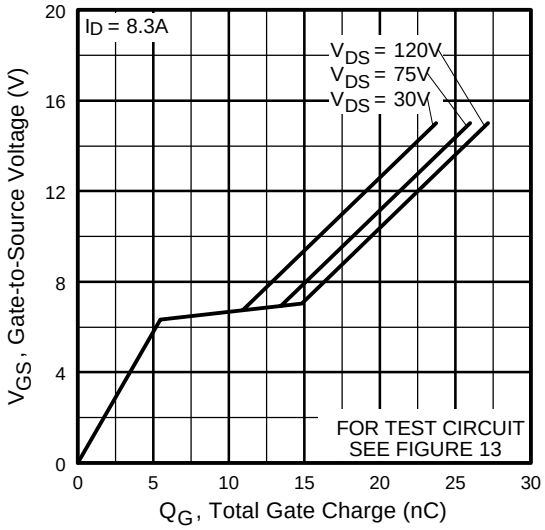


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

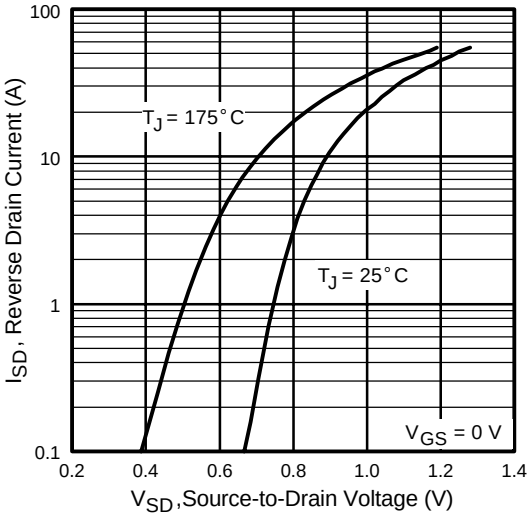


Fig 7. Typical Source-Drain Diode Forward Voltage

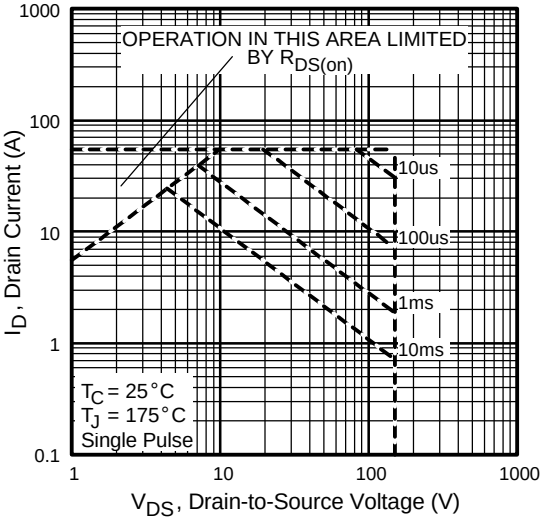


Fig 8. Maximum Safe Operating Area

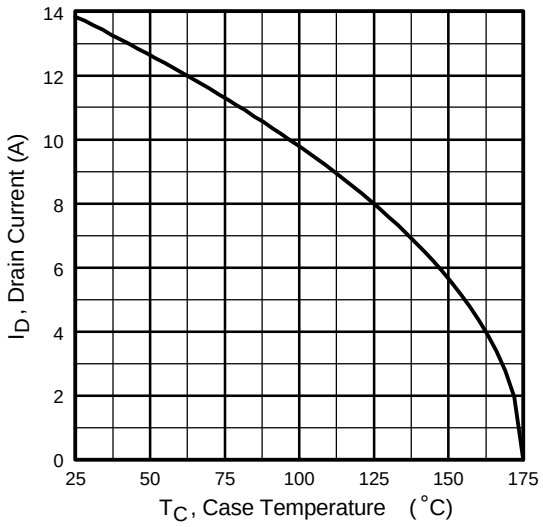


Fig 9. Maximum Drain Current Vs. Case Temperature

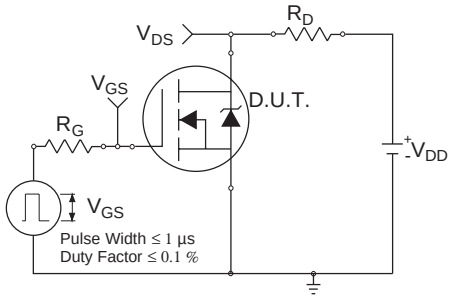


Fig 10a. Switching Time Test Circuit

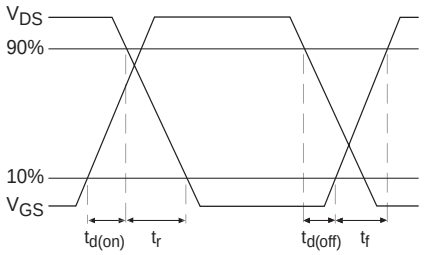


Fig 10b. Switching Time Waveforms

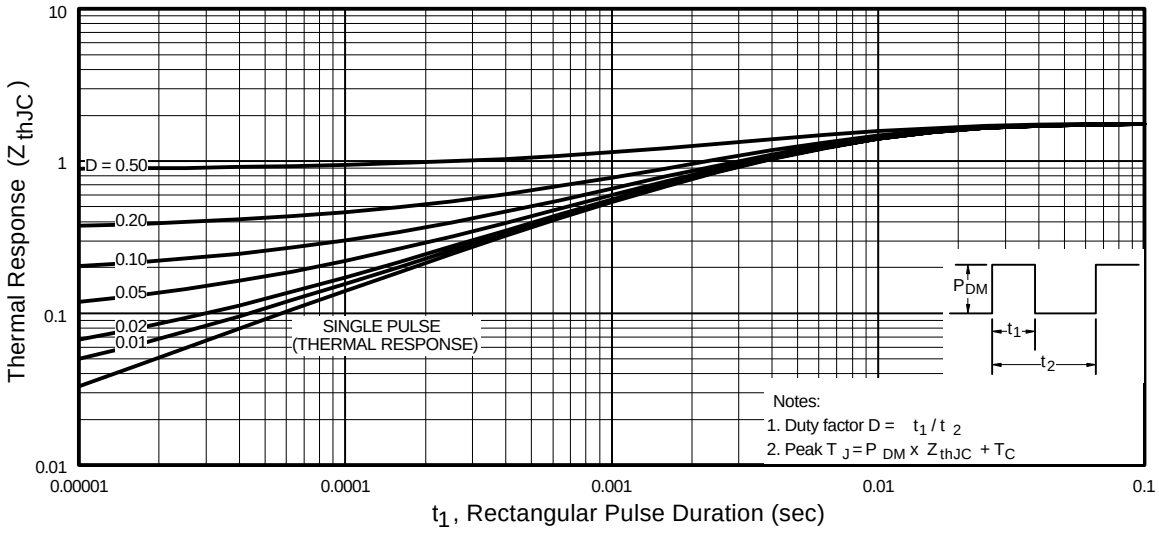


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

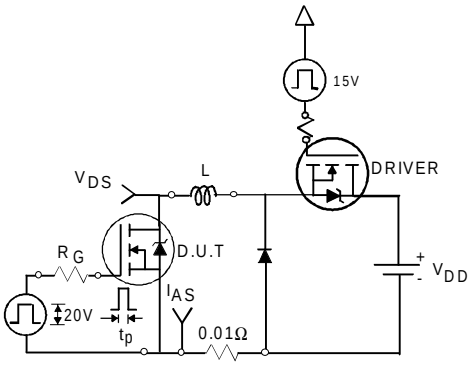


Fig 12a. Unclamped Inductive Test Circuit

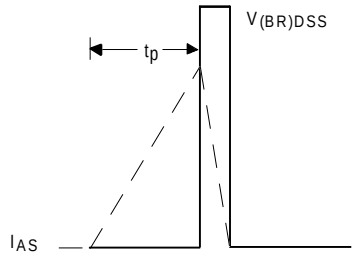


Fig 12b. Unclamped Inductive Waveforms

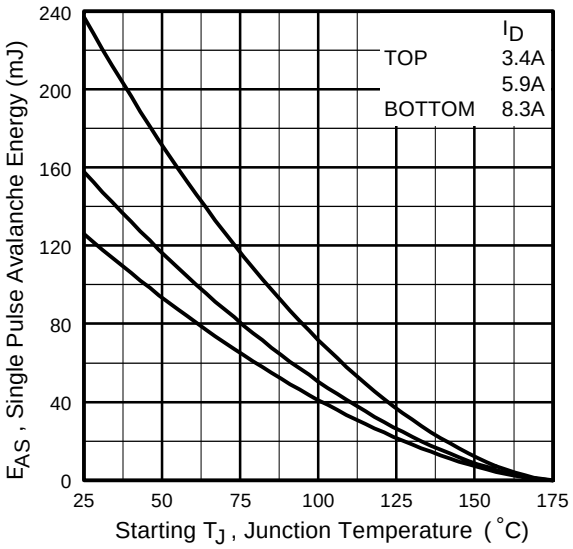


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

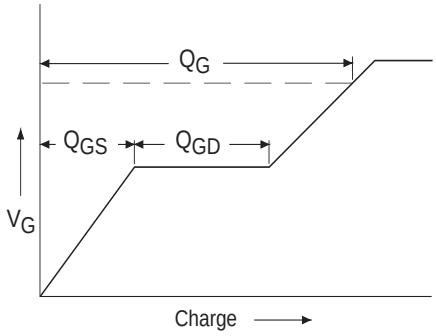


Fig 13a. Basic Gate Charge Waveform

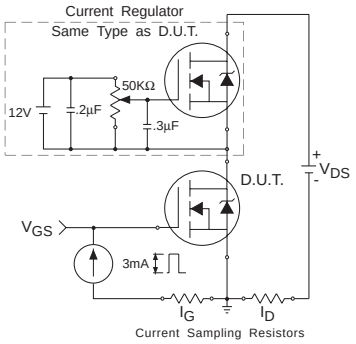
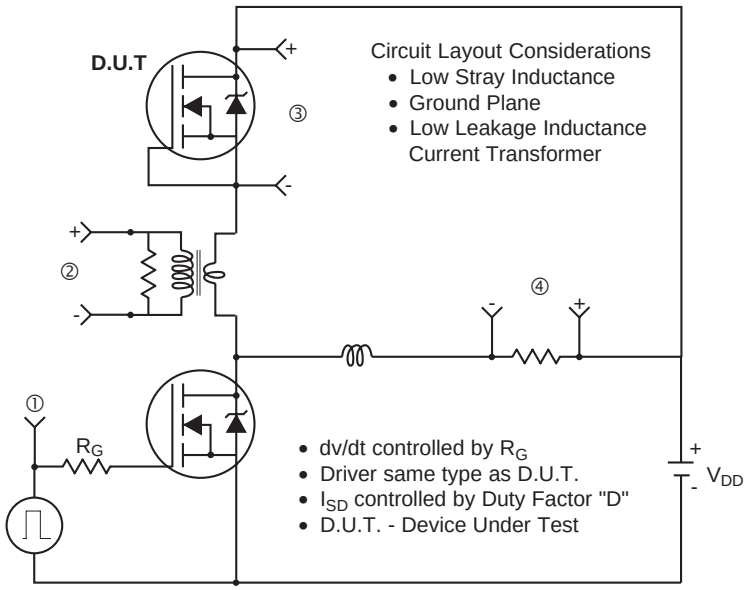
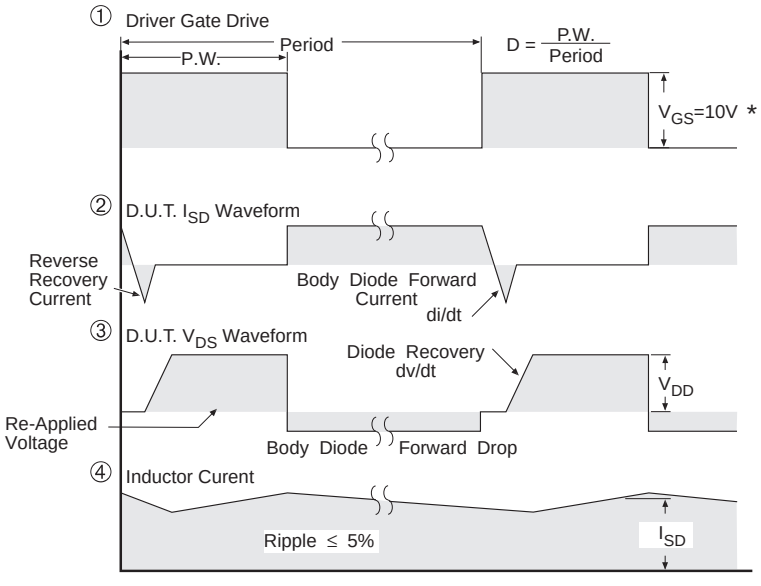


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



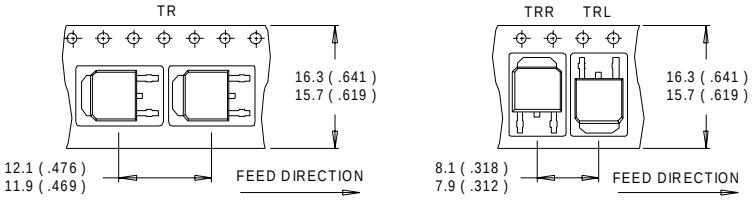


* V_{GS} = 5V for Logic Level Devices

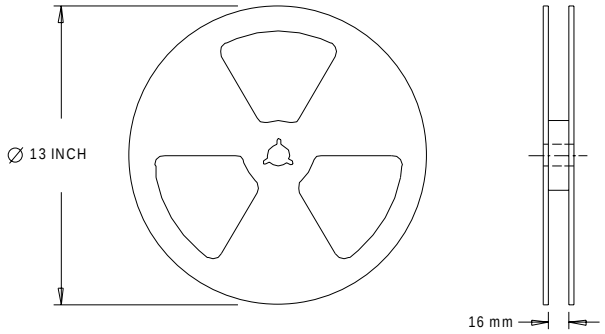
Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 3.8mH R_G = 25Ω, I_{AS} = 8.3A.

③ $I_{SD} \leq$ 8.3A, di/dt ≤ 280A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}